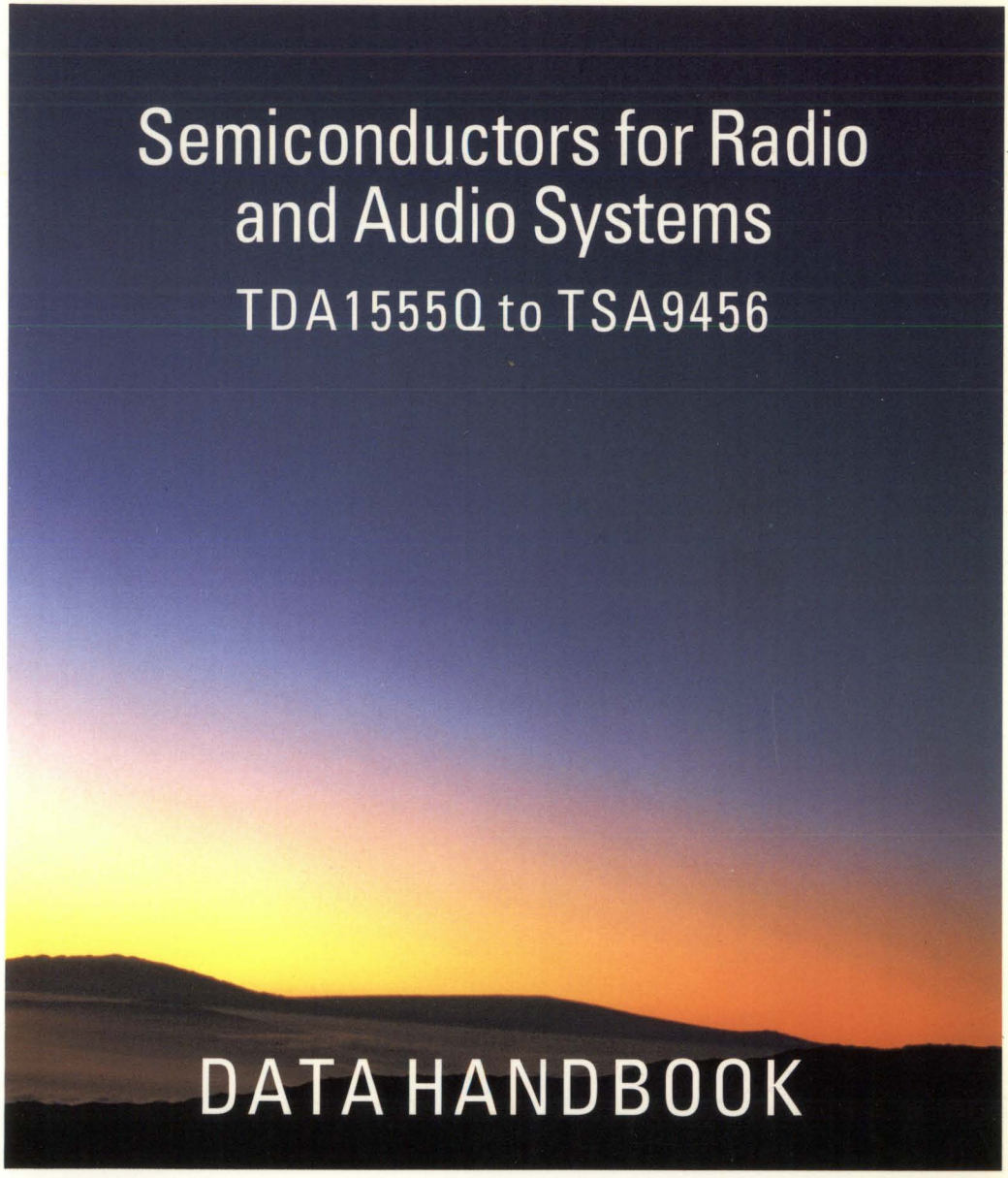
INTEGRATED CIRCUITS

Semiconductors for Radio and Audio Systems

TDA1555Q to TSA9456



DATA HANDBOOK

Philips Semiconductors

PHILIPS

BOOK IC01b 1992

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Radio and Audio Systems

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SEMICONDUCTORS

INTEGRATED CIRCUITS

MAINTAINANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA3028	high performance transcoder (RC5) for infrared rermote control; I²C-bus
SAA7210	decoder for Compact Disc digital audio system
TDA1512A	12 to 20 W hi-fi audio power amplifier
TDA1512AQ	12 to 20 W hi-fi audio power amplifier
TDA1520B	20 W hi-fi audio power amplifier; complete SOAR protection
TDA1520BQ	20 W hi-fi audio power amplifier; complete SOAR protection
TDA1576T	FM/IF amplifier/demodulator circuit

DEVICE DATA

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER WITH DISTORTION DETECTOR

GENERAL DESCRIPTION

The TDA1555Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads
- Distortion detector

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R).

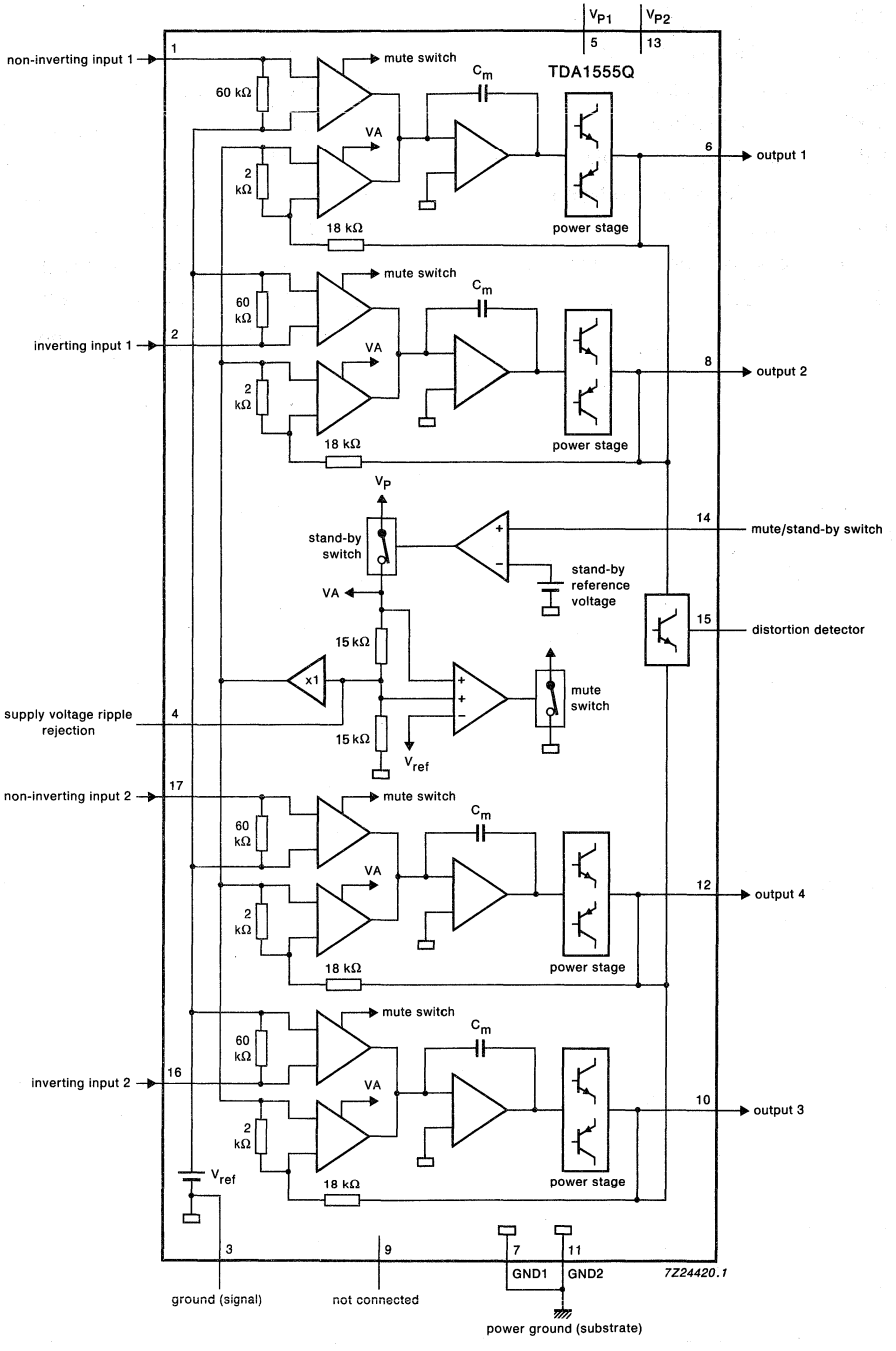


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (signal)
4	RR	supply voltage ripple rejection
5	V_{P1}	positive supply voltage 1
6	OUT1	output 1
7	GND1	power ground 1 (substrate)
8	OUT2	output 2
9	n.c.	not connected
10	OUT3	output 3
11	GND2	power ground 2 (substrate)
12	OUT4	output 4
13	V_{P2}	positive supply voltage 2
14	M/SS	mute/stand-by switch
15	DD	distortion detector
16	INV2	inverting input 2
17	NINV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1555Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of this device are:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Distortion detector

- At onset of clipping of one or more channels the distortion detector (pin 15) becomes active. This information can be used to drive a sound processor or DC volume control to decrease the input signal and so limit distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

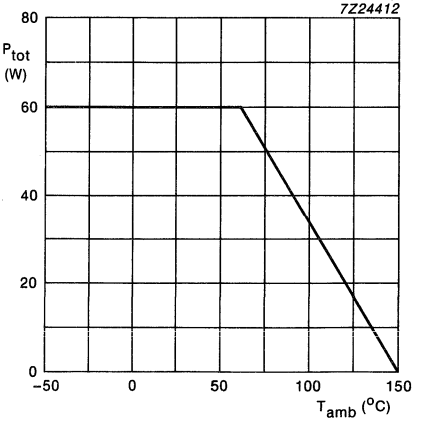


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

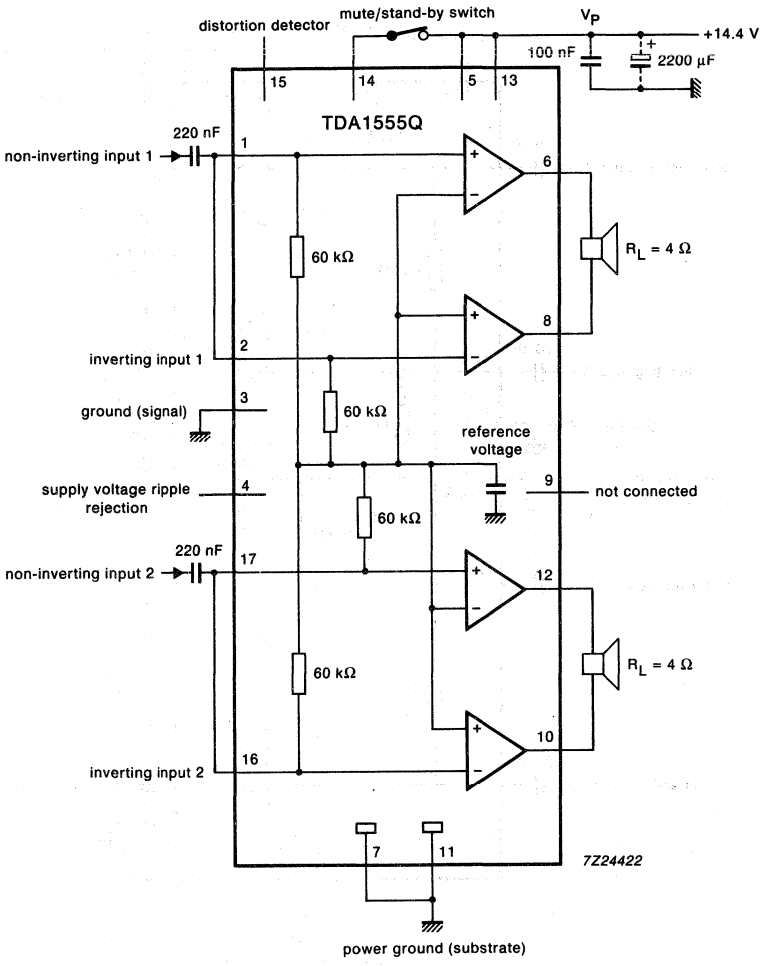


Fig.3 Stereo BTL application circuit diagram.

DEVELOPMENT DATA

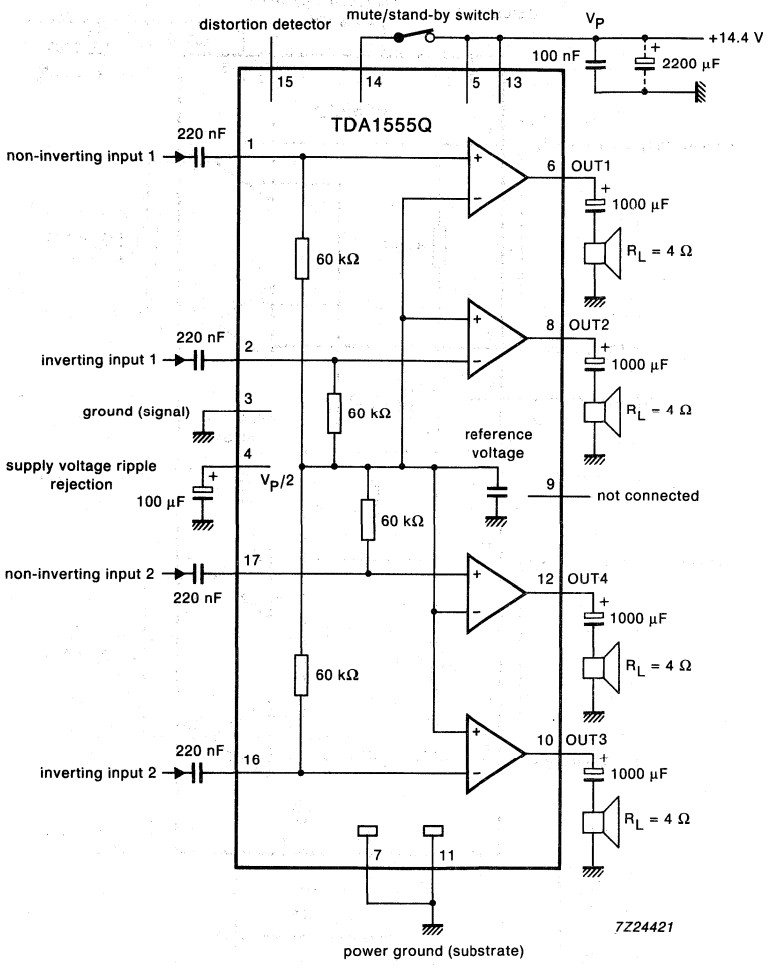


Fig.4 Quad single-ended application circuit diagram.

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

FEATURES

- Few peripheral components
- High output power
- Low output offset voltage
- Fixed gain
- Loudspeaker protection (with diagnostic facility)
- Differential inputs
- Dynamic Distortion Detector (DDD)
- High common mode input signal
- Very high CMRR
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- Short-circuit safe
- Thermally protected
- Reverse polarity safe
- High energy handling capability at the outputs (V_P = 0 V)
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance

GENERAL DESCRIPTION

TDA1556Q is a monolithic integrated class-B output amplifier containing two 22 Watt amplifiers in a BTL configuration. The device is contained in a 17-lead single-in-line (SIL) plastic power package. It has two differential inputs and is primarily intended for car booster applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	µA
I_{sw}	switch-on current		–	–	60	µA
$\|Z_I\|$	input impedance		50	–	–	kΩ
T_{vj}	virtual junction temperature		–	–	150	°C
P_O	output power	4 Ω; THD = 10%	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	48	–	–	dB
V_{os}	DC output offset voltage		–	–	100	mV
α	channel separation		40	–	–	dB
ΔG_v	channel unbalance		–	–	1	dB
CMRR	rejection ratio		–	72	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1556Q	17	SIL	plastic	SOT243R

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

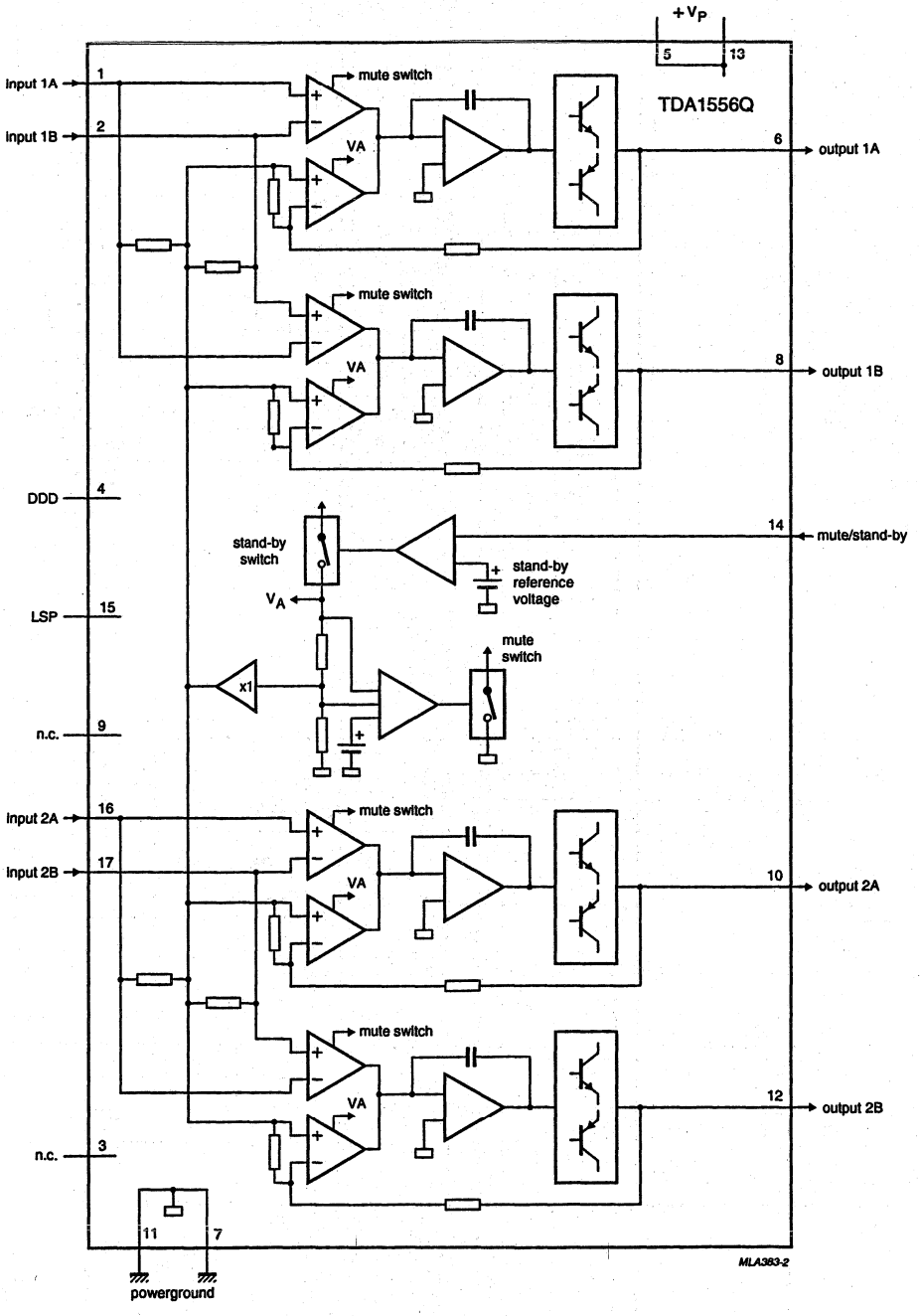


Fig.1 Block diagram.

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

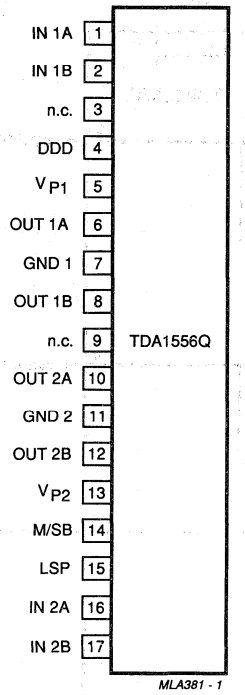


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1A	1	input signal 1A
IN1B	2	input signal 1B
n.c.	3	not connected
DDD	4	dynamic distortion detector
V_{P1}	5	positive supply voltage 1
OUT1A	6	output signal 1A
GND1	7	power ground 1
OUT1B	8	output signal 1B
n.c.	9	not connected
OUT2A	10	output signal 2A
GND2	11	power ground 2
OUT2B	12	output signal 2B
V_{P2}	13	positive supply voltage 2
M/SB	14	mute/stand-by switch
LSP	15	loudspeaker protection
IN2A	16	input signal 2B
IN2B	17	input signal 2A

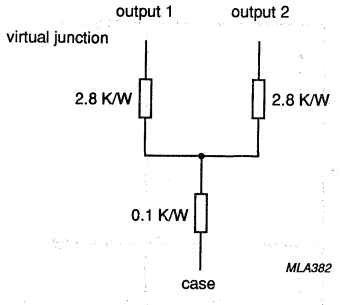


Fig.3 Thermal resistance.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Figs 3 and 4)	1.5 K/W

2 x 22 W stereo BTL differential amplifier with speaker protection and dynamic distortion detector

TDA1556Q

FUNCTIONAL DESCRIPTION

The TDA1556Q contains two identical amplifiers each with a fixed gain of 26 dB and differential input stages. The device can be used for bridge-tied-load applications. The circuit has the following features:

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Loudspeaker protection

Should a short circuit to ground occur, thereby forcing a DC voltage ≥ 1 V across the loudspeaker, a built-in protection circuit is activated to limit the DC voltage across the speaker to ≤ 1 V. The delay time of the protection circuit can be influenced by an external capacitor connected to pin 15.

A dynamic distortion detector (DDD) is activated when clipping occurs at one or both output stages. Its information may be used to operate a sound processor or DC volume control to attenuate the input signal, thereby minimizing the distortion.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		during 50 ms (load dump protection); rise time ≥ 2.5 ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature range		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
V_{os}	DC output offset voltage	operating	–	–	100	mV
Mute/stand-by						
V_{ON}	switch-on voltage level		8.5	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	$V_{I\ max}$ = 1 V; f = 1 kHz	–	–	2	mV
V_{os}	DC output offset voltage		–	–	100	mV
STANDBY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC standby current	V_{14} < 0.5 V	–	–	100	µA
		0.5 V ≤ V_{14} ≤ 2.0 V	–	–	500	µA
I_{sw}	switch-on current		–	25	60	µA
I_{PSC}	supply current	short-circuit to ground; note 3	–	10	–	mA
Loudspeaker protection						
$\lvert\Delta V_{6\text{-}8,\ 10\text{-}12}\rvert$	DC voltage across R_L		–	–	1.0	V
t_d	delay time		–	0.5	–	s
Protection active ($\lvert\Delta V_{4\text{-}6}\rvert$ or $\lvert\Delta V_{7\text{-}9}\rvert \leq 1.0$ V						
I_{15}	current information		–	25	–	µA
V_{15}	voltage information		3.6	–	–	V
Protection inactive ($\lvert\Delta V_{6\text{-}8}\rvert$ and $\lvert\Delta V_{10\text{-}12}\rvert \leq 0.1$ V)						
V_{15}	voltage information		–	–	0.3	V

Notes to the DC characteristics

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$
3. Conditions: V_{14} = 0 V; short-circuit to ground; switch V_{14} to MUTE or ON condition, rise time at V_{14} = ≥ 10 µs
4. Frequency response externally fixed
5. Ripple rejection measured at the output with a source-impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz
6. Mismatching is given by the following equation:

$$|\Delta Z_i| = \frac{Z_{i1} - Z_{i2}}{Z_{i1}} \times 100\%$$

$$|\Delta Z_i| = \frac{Z_{i3} - Z_{i4}}{Z_{i3}} \times 100\%$$

7. Noise measured in a bandwidth of 20 Hz to 20 kHz
8. Noise output voltage independent of R_S (V_I = 0 V)
9. Common mode rejection ratio measured at the output with both inputs tied together. $V_{I(RMS)}$ < 3.5 V; f = 100 Hz - 10 kHz

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		THD = 0.5%; V_p = 13.2 V	–	12	–	W
		THD = 10%; V_p = 13.2 V	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	−1 dB; note 4	–	25	–	Hz
f_h	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 5				
		ON condition	48	–	–	dB
		MUTE condition	48	–	–	dB
		stand-by condition	80	–	–	dB
$\|Z_I\|$	input impedance		100	120	150	kΩ
$\|\Delta Z_I\|$	input impedance	note 6	–	4	–	%
V_{no}	noise output voltage	ON: R_S = 0 Ω; note 7	–	70	120	μV
		ON: R_S = 10 kΩ; note 7	–	100	–	μV
		MUTE: R_S = 10 kΩ; notes 7 and 8	–	60	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
ΔG_v	channel unbalance		–	–	1	dB
CMRR	common mode rejection ratio	note 9	66	72	–	dB
THD	total harmonic distortion	I_{DDD} = 50 μA (peak)	–	3.5	–	%

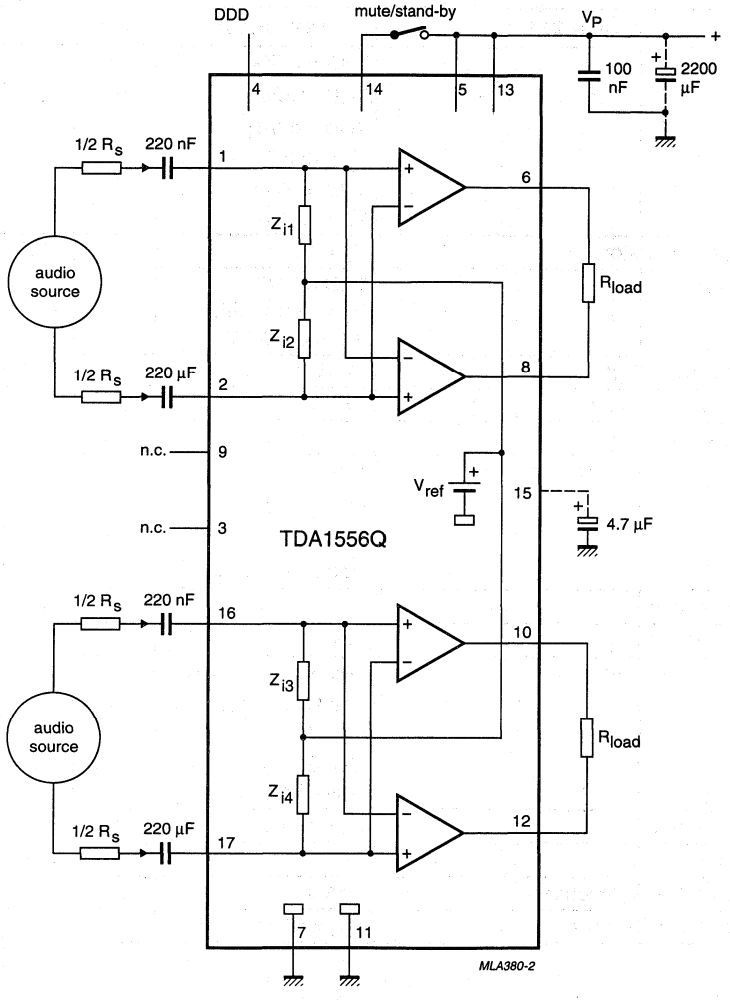


Fig.4 Stereo BTL test diagram.

2 x 22 W BTL stereo car radio power amplifier with speaker protection

TDA1557Q

FEATURES

- Requires very few external components
- High output power
- Low offset voltage at output
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA1557Q is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device contains 2 x 22 W amplifiers in BTL configuration and has been primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
IORM	repetitive peak output current		–	–	4	A
I_{tot}	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	µA
I_{sw}	switch-on current		–	–	60	µA
$\|Z_I\|$	input impedance		25	–	–	kΩ
T_{XTAL}	crystal temperature		–	–	+150	°C
Stereo application						
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0; f = 100 Hz to 10 kHz	45	–	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
α	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
G_v	closed loop voltage gain		45	46	47	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1557Q	13	DIL	plastic	SOT141R

2 x 22 W BTL stereo car radio power amplifier with speaker protection

TDA1557Q

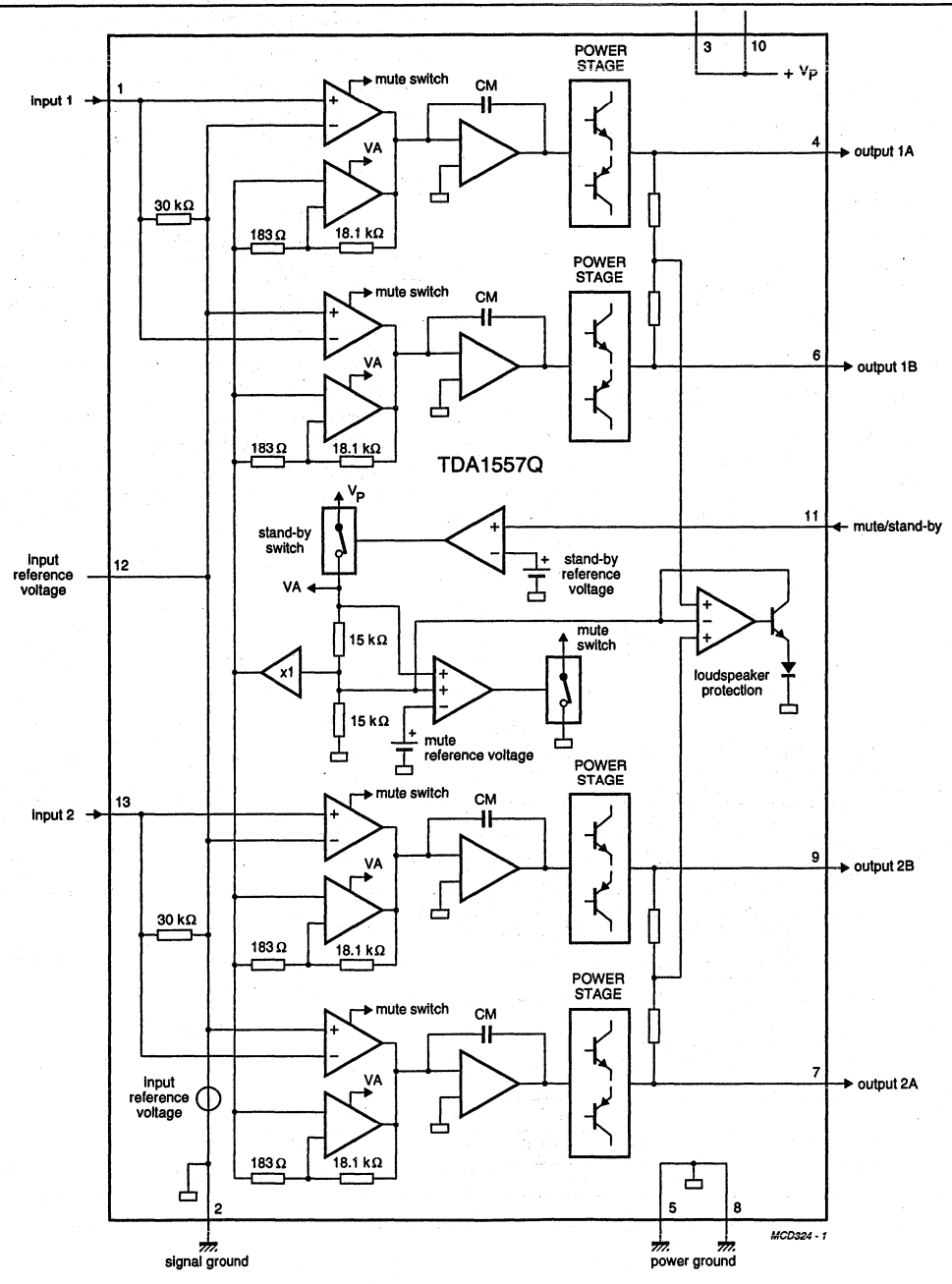


Fig.1 Block diagram.

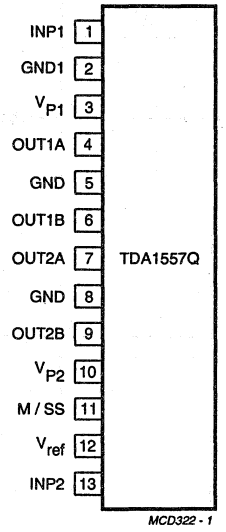


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
INP1	1	input 1
GND1	2	ground (signal)
V_{P1}	3	supply voltage 1
OUT1A	4	output 1A
GND	5	power ground 1
OUT1B	6	output 1B
OUT2A	7	output 2A
GND	8	power ground 2
OUT2B	9	output 2B
V_{P2}	10	supply voltage 2
M/SS	11	mute/stand-by switch
V_{ref}	12	input reference voltage
INP2	13	input 2

FUNCTIONAL DESCRIPTION

The TDA1557Q contains two identical amplifiers with differential input stages, and can be used for bridge applications. The gain of each amplifier is fixed at 46 dB. Special features of this device are:

a. mute/stand-by switch

low stand-by current

low mute/stand-by switching current (low cost supply switch)

mute facility

b. loudspeaker protection

when a short circuit to ground is made, which forces a DC voltage of ≥ 1 V across the loudspeaker, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to ≤ 1 V

c. the harmonic distortion at low frequencies can be decreased by connecting two diodes to ground at pin 12.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6.0	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
IOSM	non-repetitive peak output current		–	6	A
IORM	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature range		–55	+150	°C
Tj	junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ vj\text{-}a}$	from virtual junction to ambient in free air	40 K/W
$R_{th\ vj\text{-}c}$	from virtual junction to case (see Fig.3)	1.5 K/W

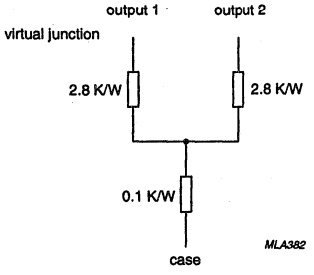


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
Mute/stand-by switch						
V_{sw}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V max; f = 1 kHz	–	–	20	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2.0	V
I_{sb}	DC current in stand-by condition	$V_{11} \leq 0.5$ V $0.5 < V_{11} \leq 2$ V	– –	– –	100 500	µA µA
I_{sw}	switch-on current		–	30	60	µA
I_P	positive supply current	short-circuit to GND; note 4	–	5.5	–	mA
Loudspeaker protection						
$\lvert\Delta V_{4\text{-}6,\ 7\text{-}9}\rvert$	DC voltage across R_L		–	–	1.0	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power					
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		V_P = 13.2 V; THD = 0.5%	–	12	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = –1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	–1 dB; note 5	–	25	–	Hz
f_{high}	high frequency roll-off	–1 dB	20	–	–	kHz
G_v	closed loop voltage gain		45	46	47	dB
SVRR	supply voltage ripple rejection					
		ON; note 6	34	–	–	dB
		ON; note 7	38	–	–	dB
		ON; note 8	45	–	–	dB
		MUTE; notes 6 and 7	45	–	–	dB
		stand-by; notes 6 and 7	80	–	–	dB
$\|Z_i\|$	input impedance		25	30	36	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 9	–	325	500	μV
		R_S = 10 kΩ; note 9	–	350	–	μV
		MUTE; notes 9 & 10	–	180	–	μV
α	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
3. At 18 V < V_P < 30 V, the DC output voltage ≤ $V_P/2$
4. Conditions: V_{11} = 0; short-circuit output to GND; switch V_{11} to MUTE or ON condition (rise time V_{11} > 10 μs).
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency of 100 Hz.
7. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 1 and 10 kHz.
8. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz. Pin 12 is decoupled with two diodes to ground.
9. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
10. Noise output voltage independent of R_S (V_{in} = 0).

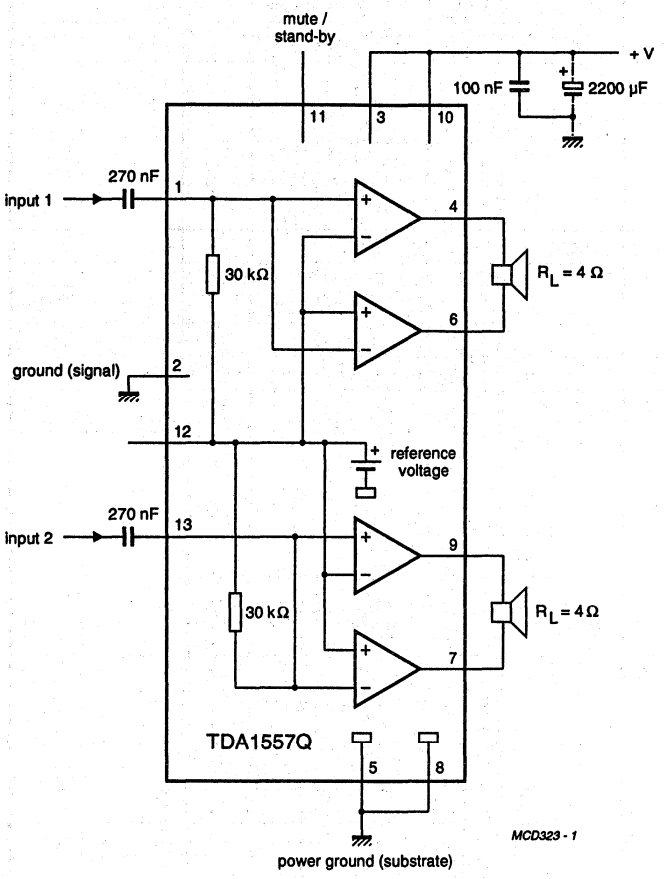


Fig.4 Stereo BTL application.

2 x 22 W or 4 x 11 W single-ended car radio power amplifier

TDA1558Q

FEATURES

- Requires very few external components
- Flexibility in use Quad single-ended or stereo BTL
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA1558Q is a monolithic integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The device contains 4 x 11 W single-ended or 2 x 22 W BTL amplifiers and has been primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range	operating	6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_{tot}	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
Stereo BTL application						
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection		45	–	–	dB
V_{no}	noise output voltage	R_S = 0	–	200	–	μV
$\|Z_i\|$	input impedance		25	–	–	kΩ
$\|\Delta V_{os}\|$	DC output offset voltage		–	–	250	mV
G_v	closed loop voltage gain		45	46	47	dB
Quad single-ended application						
P_O	output power	THD = 10%; 4 Ω	–	6	–	W
		THD = 10%; 2 Ω	–	11	–	W
SVRR	supply voltage ripple rejection		44	–	–	dB
V_{no}	noise output voltage	R_S = 0	–	150	–	μV
$\|Z_i\|$	input impedance		50	–	–	kΩ
G_v	closed loop voltage gain		39	40	41	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1558Q	17	DIL	plastic	SOT243R

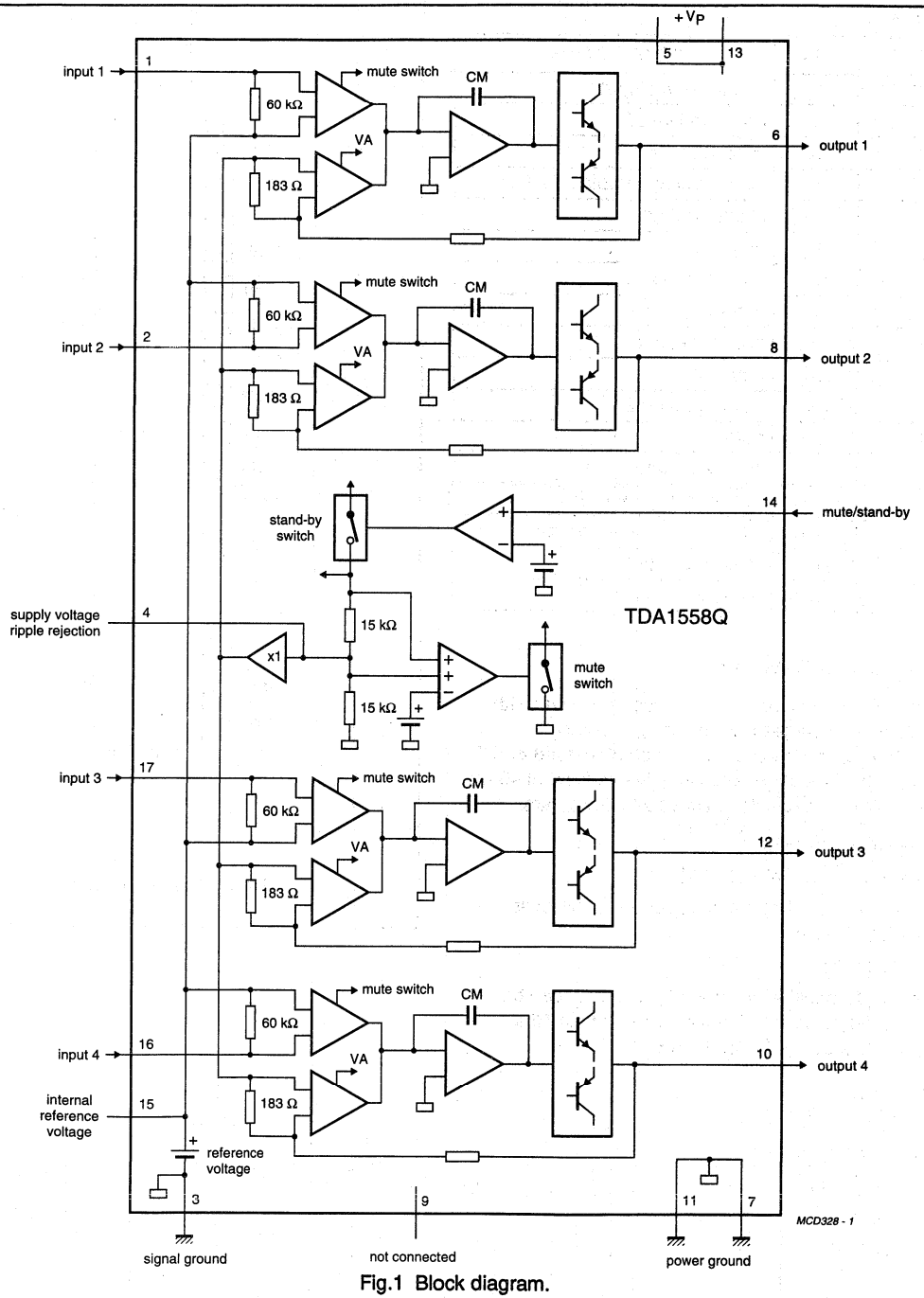


Fig.1 Block diagram.

2 x 22 W or 4 x 11 W single-ended car radio power amplifier

TDA1558Q

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
INV2	2	inverting input 2
GND	3	ground (signal)
SVRR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
n.c.	9	not connected
OUT4	10	output 4
GND2	11	power ground 2
OUT3	12	output 3
V_{P2}	13	supply voltage
M/SS	14	mute/stand-by switch
V_{ref}	15	internal reference voltage
INV3	16	inverting input 3
–INV4	17	non-inverting input 4

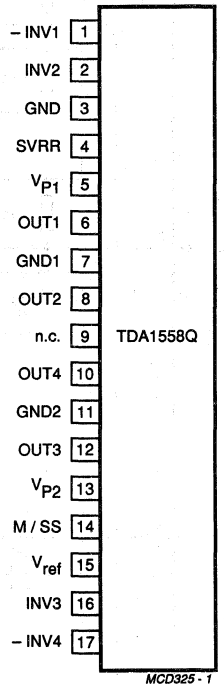


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1558Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting), and can be used for single-ended or BTL applications. The gain of each amplifier is fixed at 40 dB (46 dB in BTL). Special features of this device are:

a. mute/stand-by switch

   low stand-by current (< 100 μA)

   low mute/stand-by switching current (low cost supply switch)

   mute facility.

b. the harmonic distortion at low frequencies can be decreased by connecting two diodes at pin 15 to ground or a zener diode of 1.5 V.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		–	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ vj\text{-}a}$	from virtual junction to ambient in free air	40 K/W
$R_{th\ vj\text{-}c}$	from virtual junction to case (see Fig.3)	1.5 K/W

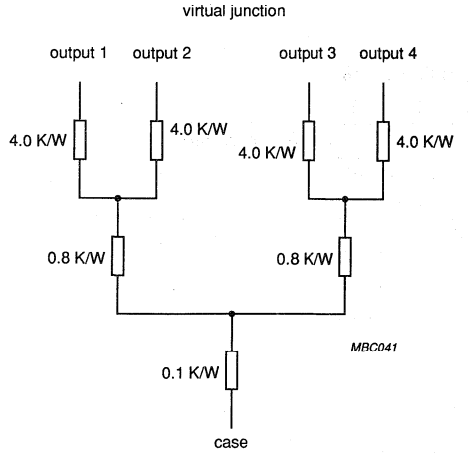


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage		–	–	250	mV
Mute/stand-by switch						
V_{ON}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max); f = 1 kHz	–	–	20	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage	between pins 6-8 and pins 10-12	–	–	250	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC current in stand-by condition		–	–	100	µA
I_{sw}	switch-on current		–	12	40	µA

AC CHARACTERISTICS

V_P = 14.4 V, R_L = 4 Ω, f = 1 kHz, T_{amb} = 25 °C, unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		V_P = 13.2 V; THD = 0.5%	–	12	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
B	power bandwidth	THD = 0.5%; P_O = –1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	–1 dB; note 4	–	45	–	Hz
f_{high}	high frequency roll-off	–1 dB	20	–	–	kHz
G_v	closed loop voltage gain		45	46	47	dB
SVRR	supply voltage ripple rejection					
		ON; note 5	45	–	–	dB
		MUTE; note 5	45	–	–	dB
		stand-by; note 5	80	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Z_i\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 6	–	200	300	μV
		R_S = 10 kΩ; note 6	–	350	–	μV
		MUTE; notes 6 and 7	–	180	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
Quad single-ended application (see Fig.5)						
P_O	output power	note 8				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	6	–	W
		R_L = 2 Ω; THD = 0.5%	7.5	8.5	–	W
		R_L = 2 Ω; THD = 10%	10	11	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
f_{low}	low frequency roll-off	–3 dB; note 4	–	45	–	Hz
f_{high}	high frequency roll-off	–1 dB	20	–	–	kHz
G_v	closed loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection	note 5				
		ON	44	–	–	dB
		MUTE	44	–	–	dB
		stand-by	80	–	–	dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 6	–	150	230	μV
		R_S = 10 kΩ; note 6	–	250	–	μV
		MUTE; notes 6 and 7	–	120	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
3. At 18 V < V_P < 30 V, the DC output voltage ≤ V_P/2.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
6. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage independent of R_S (V_{in} = 0).
8. Output power is measured directly at the output pins of the IC.

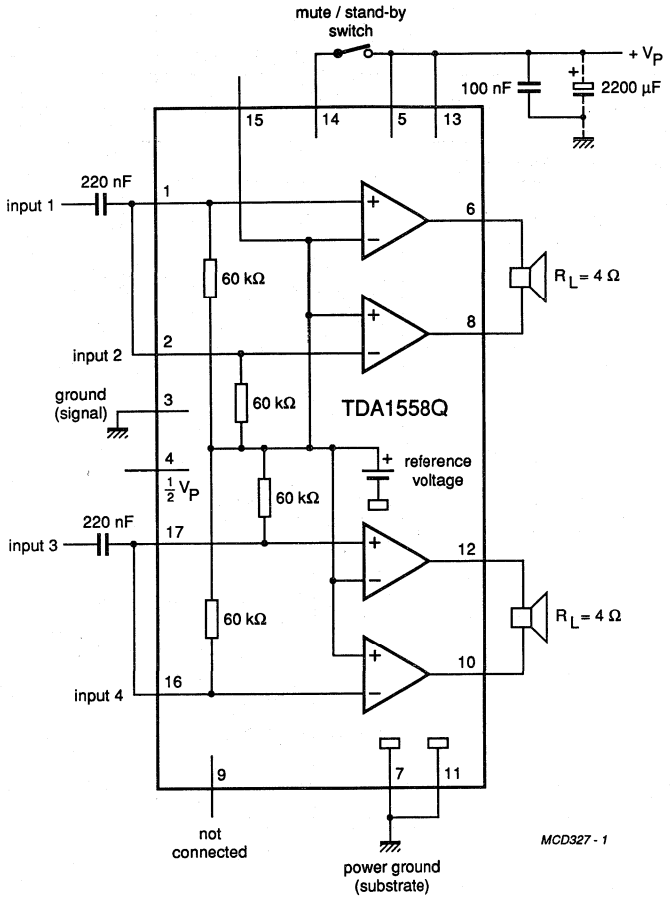


Fig.4 Stereo BTL application.

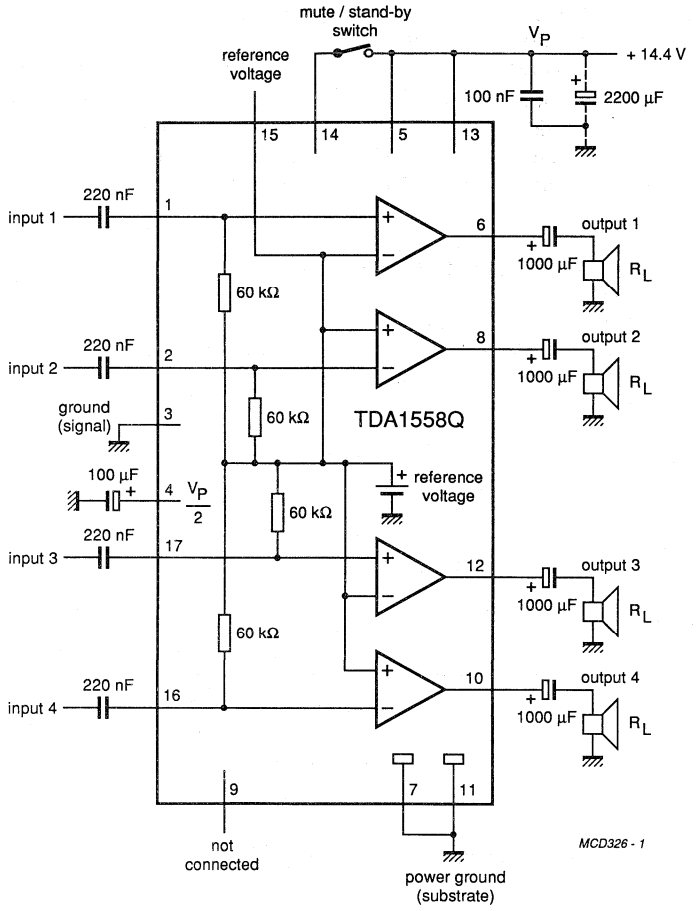


Fig.5 Quad single-ended application.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1572 integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

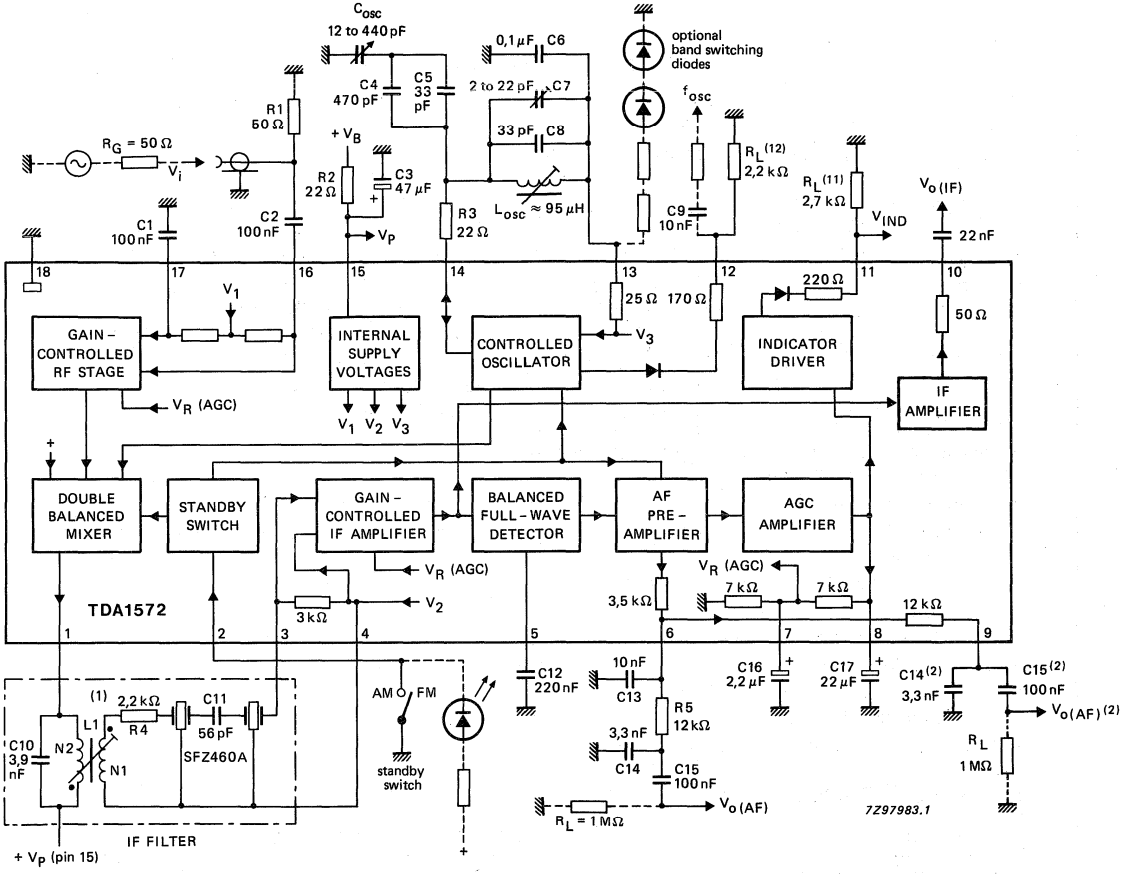
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7,5	–	18,0	V
Supply current range	I_P	15	–	30	mA
RF input voltage for (S+N)/N = 6 dB at m = 30%	$V_{i(RF)}$	–	1,5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%	$V_{i(RF)}$	–	500	–	mV
IF output voltage with V_i = 2 mV	$V_{o(IF)}$	–	230	–	mV
AF output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{o(AF)}$	–	310	–	mV
AGC range: change of V_i for 1 dB change of $V_{o(AF)}$		–	86	–	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(11)}$ = 2,7 kΩ	V_{IND}	–	2,8	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

(2) AF output is pin 6 is not used.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S+N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{13\text{-}18}$. An extra buffered oscillator putput (pin 12) is available for driving a synthesizer. If this is not needed, resistor $R_{L(12)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 10.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(11)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{15-18}$	–	20	V
Total power dissipation	P_{tot}	–	875	mW
Input voltage	$\|V_{16-17}\|$	–	12	V
	$-V_{16-18}$, $-V_{17-18}$	–	0,6	V
	V_{16-18}, V_{17-18}	–	V_P	V
Input current	$\|I_{16}\|$, $\|I_{18}\|$	–	200	mA
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C
Junction temperature	T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$		80	K/W

CHARACTERISTICS

$V_P = V_{15-18} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 15)	V_P	7,5	8,5	18,0	V
Supply current (pin 15)	I_P	15	23	30	mA
RF stage and mixer (pins 16 and 17)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$	Z_i	–	5,5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6,5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-15(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1,2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability: (r.m.s. value): input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,1	–	60	MHz
Oscillator amplitude (pins 13 to 14)	V	–	130	150	mV
External load impedance (pins 14 to 13)	$R_{(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation (pins 14 to 13)	$R_{(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_p = 100 Hz (SVRR = 20 log [V_{15}/V_{13}])	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 13)	V	–	4,2	–	V
DC output current (for switching diodes) (pin 13)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{13} = 20 mA (switch to maximum load) (pin 13)	ΔV_I	–	0,3	–	V
Buffered oscillator output (pin 12)					
DC output voltage	V_O	–	0,8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p-p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2,0	–	V
IF input impedance (pins 3 to 4)	Z_i	2,4	3,0	3,9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4)	V_i	–	90	–	mV
IF output impedance (pin 10)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 10)	V_o	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 18)	G_v	–	68	–	dB
AGC range of IF stages: change of V_{3-4} for 1 dB change of $V_{o(AF)}$; $V_{3-4(ref)}$ = 75 mV	ΔV_v	–	55	–	dB
AF output voltage at $V_{3-4(IF)}$ = 50 μV	$V_{o(AF)}$	–	130	–	mV
AF output voltage at $V_{3-4(IF)}$ = 1 mV	$V_{o(AF)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2,8	3,5	4,2	kΩ

parameter	symbol	min.	typ.	max.	unit
Indicator driver (pin 11)					
Output voltage at V_i = 0 mV; R_L = 2,7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV; R_L = 2,7 kΩ	V_o	2,5	2,8	3,1	V
Load resistance	R_L	1,5	–	–	kΩ
Standby switch					
Switching threshold at; V_P = 7,5 to 18 V; T_{amb} = −40 to +80 °C					
ON-voltage	V_{2-1}	0	–	2,0	V
OFF-voltage	V_{2-1}	3,5	–	20,0	V
ON-current at V_{2-1} = 0 V	$-I_2$	–	100	200	μA
OFF-current at V_{2-1} = 20 V	$\|I_2\|$	–	–	10	μA

OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

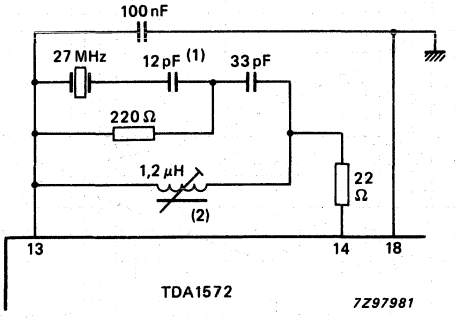
parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input required for (S+N)/N = 6 dB	V_i	–	1,5	–	μV
RF input required for (S+N)/N = 26 dB	V_i	–	15	–	μV
RF input required for (S+N)/N = 46 dB	V_i	–	150	–	μV
RF input at start of AGC	V_i	–	30	–	μV
RF large signal handling					
RF input at THD = 3%; m = 80%	V_i	–	500	–	mV
RF input at THD = 3%; m = 30%	V_i	–	700	–	mV
RF input at THD = 10%; m = 30%	V_i	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
IF output voltage at V_i = 2 mV	$V_{o(IF)}$	180	230	290	mV
AF output voltage at V_i = 4 μV; m = 80%	$V_{o(AF)}$	–	130	–	mV
AF output voltage at V_i = 2 mV	$V_{o(AF)}$	240	310	390	mV
THD at V_i = 1 mV	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV	d_{tot}	–	1	–	%
Signal plus noise-to-noise ratio at V_i = 100 mV	(S+N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_P/V_{o(AF)}]$)	RR	–	38	–	dB
a) additional AF signal at IF output	RR	–	0*	–	dB
b) add modulation at IF output (m_{ref} = 30%)	RR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	*	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	*	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

* Value to be fixed.

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

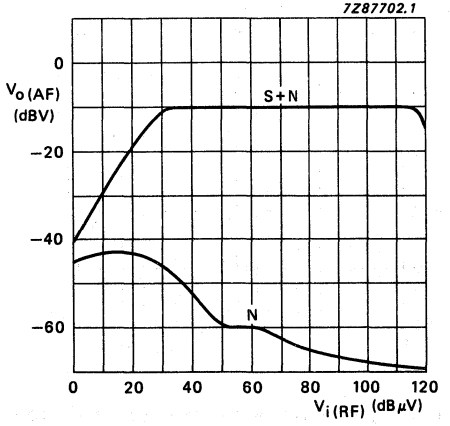


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

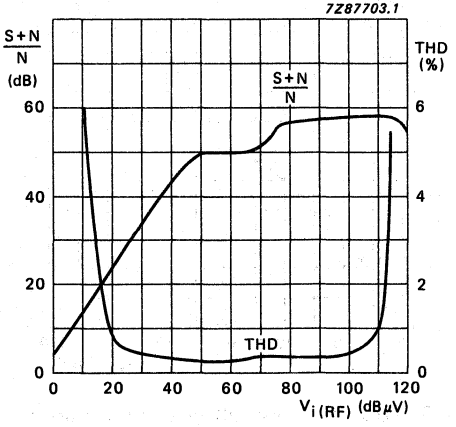


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

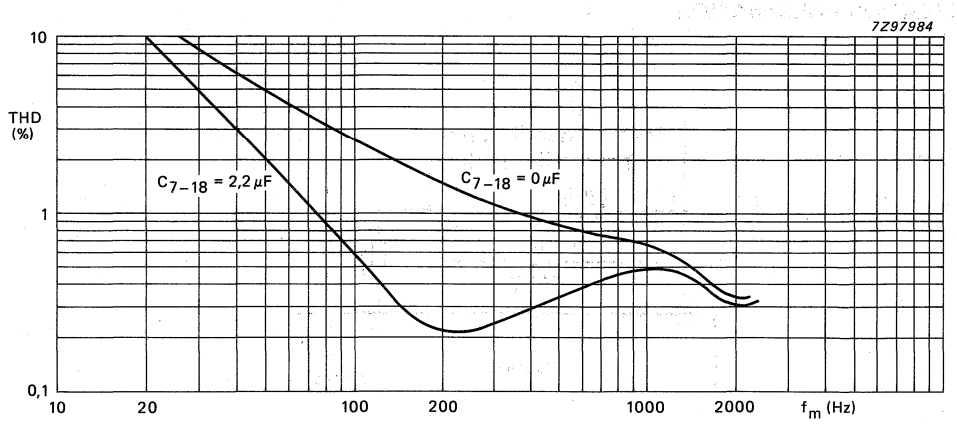


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-18(ext)}$ = 0 μF and 2,2 μF.

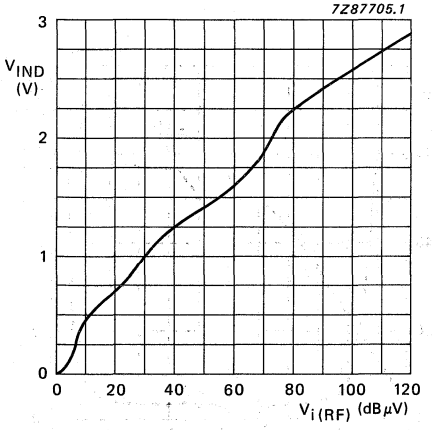


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.

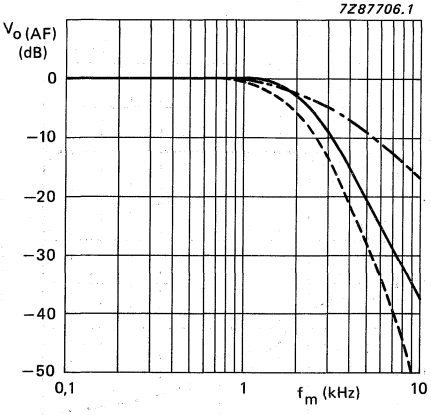


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:

——— with IF filter;
—·—·— with AF filter;
– – – – – – with IF and AF filters.

APPLICATION INFORMATION (continued)

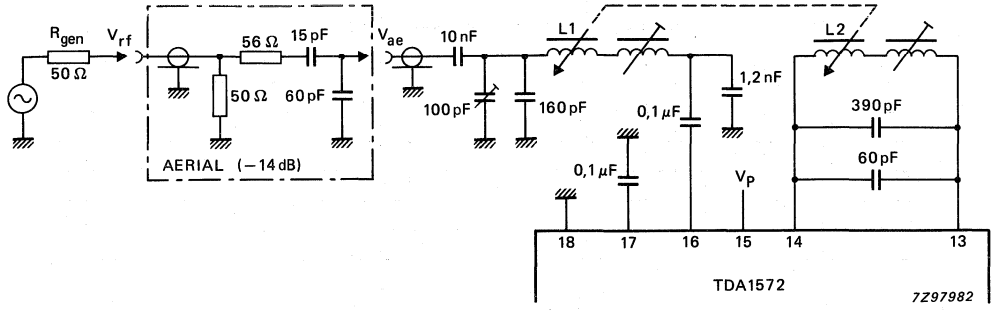


Fig. 8 Car radio application with inductive tuning.

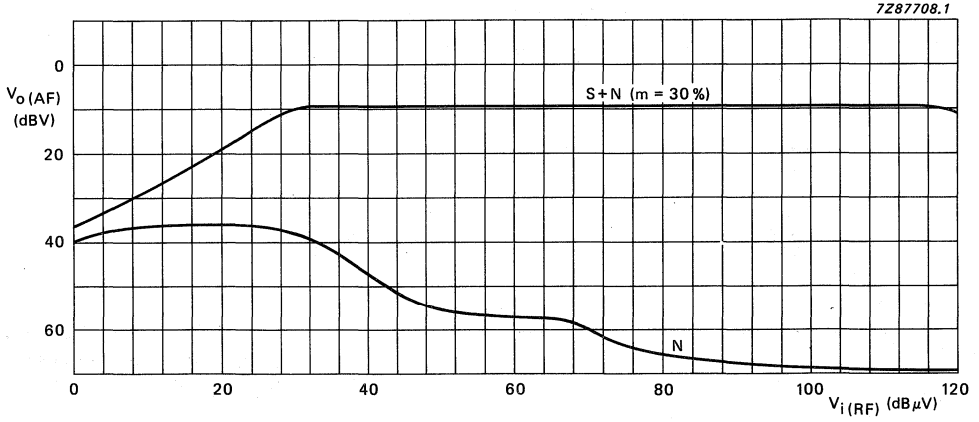


Fig. 9 AF output as a function of RF input using the circuit of Fig. 8 with that of Fig. 1.

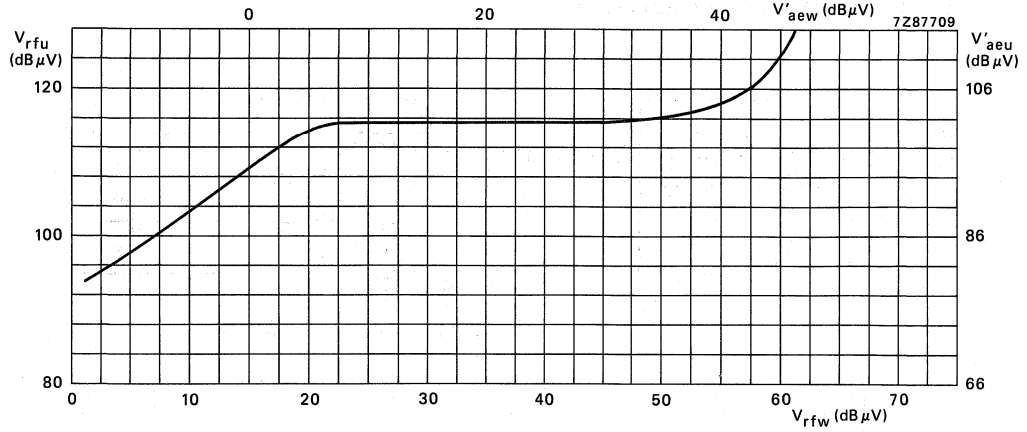


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(AF)}$/Unwanted $V_{o(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

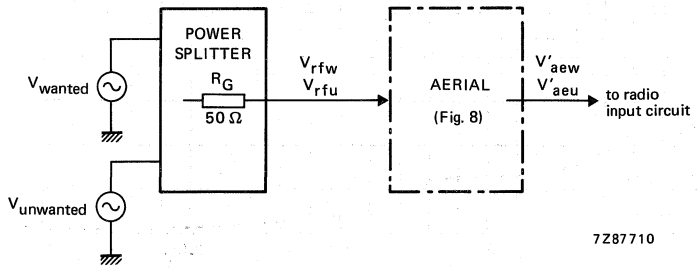


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

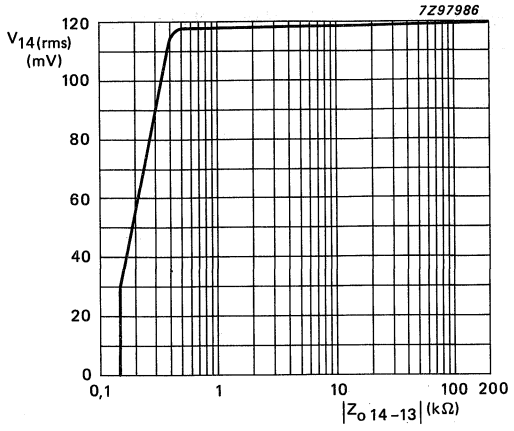


Fig. 12 Oscillator amplitude as a function of pin 13, 14 impedance in the circuit of Fig. 8.

APPLICATION INFORMATION (continued)

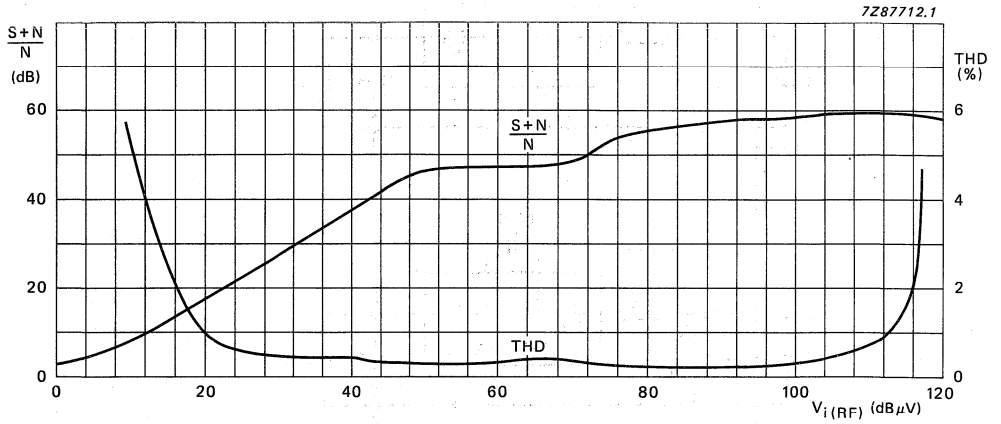


Fig. 13 Total harmonic distortion and (S + N)/N as functions of RF input using the circuit of Fig. 8 with that of Fig. 1.

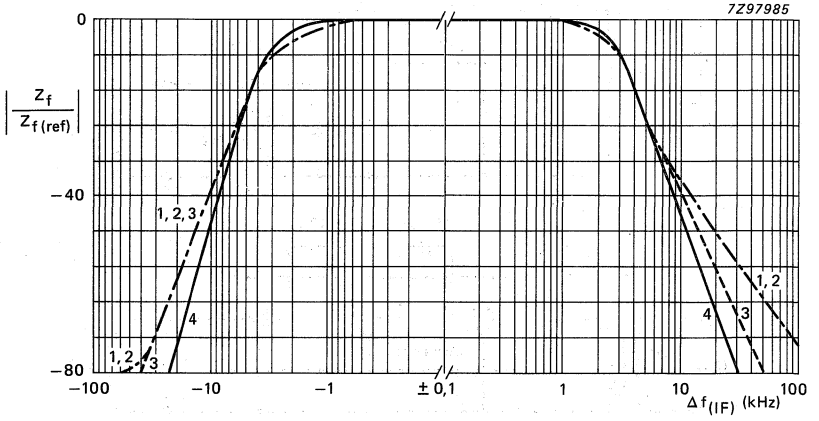


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

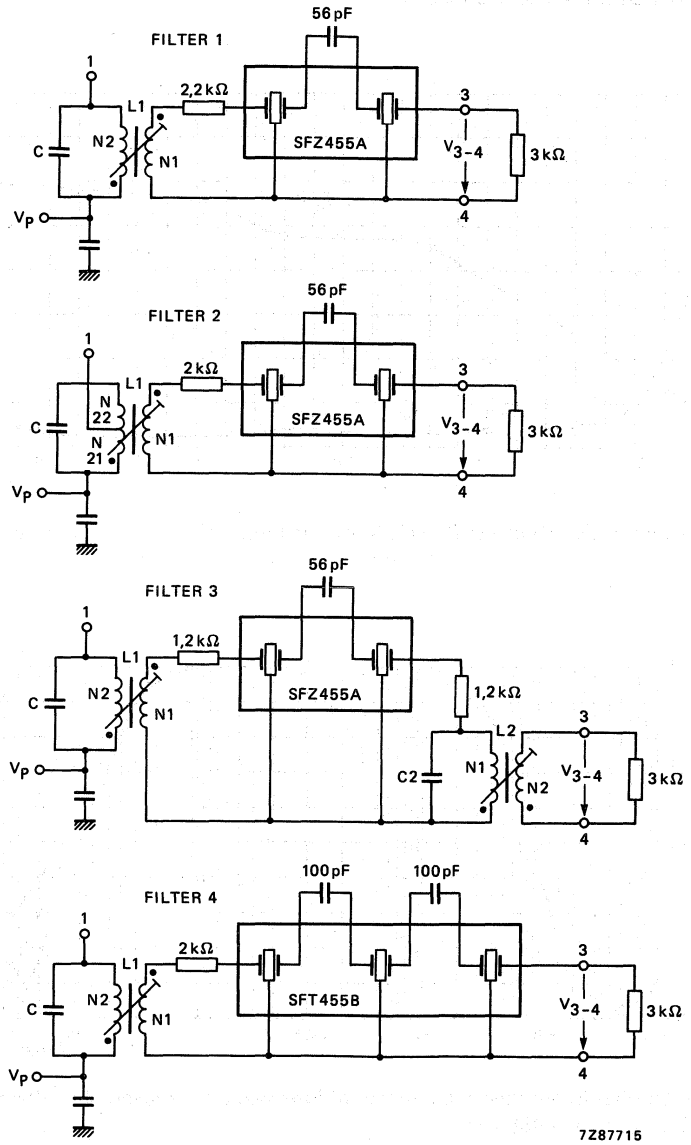


Fig. 15 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

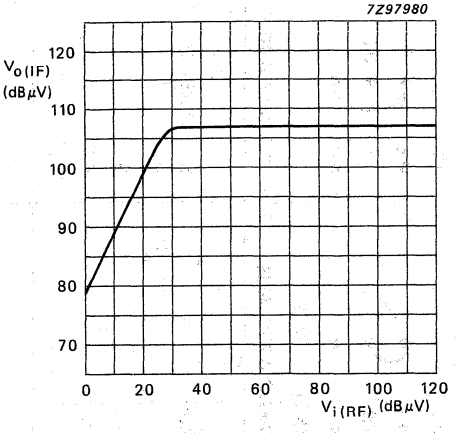
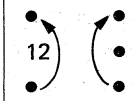
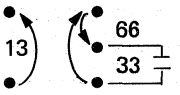
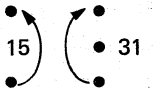
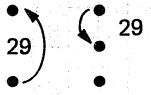
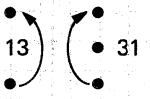


Fig. 16 IF output voltage as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz.

Table 1 Data for IF filters shown in Fig. 15. Criteria for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

AM RECEIVER

GENERAL DESCRIPTION

The TDA1572T integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

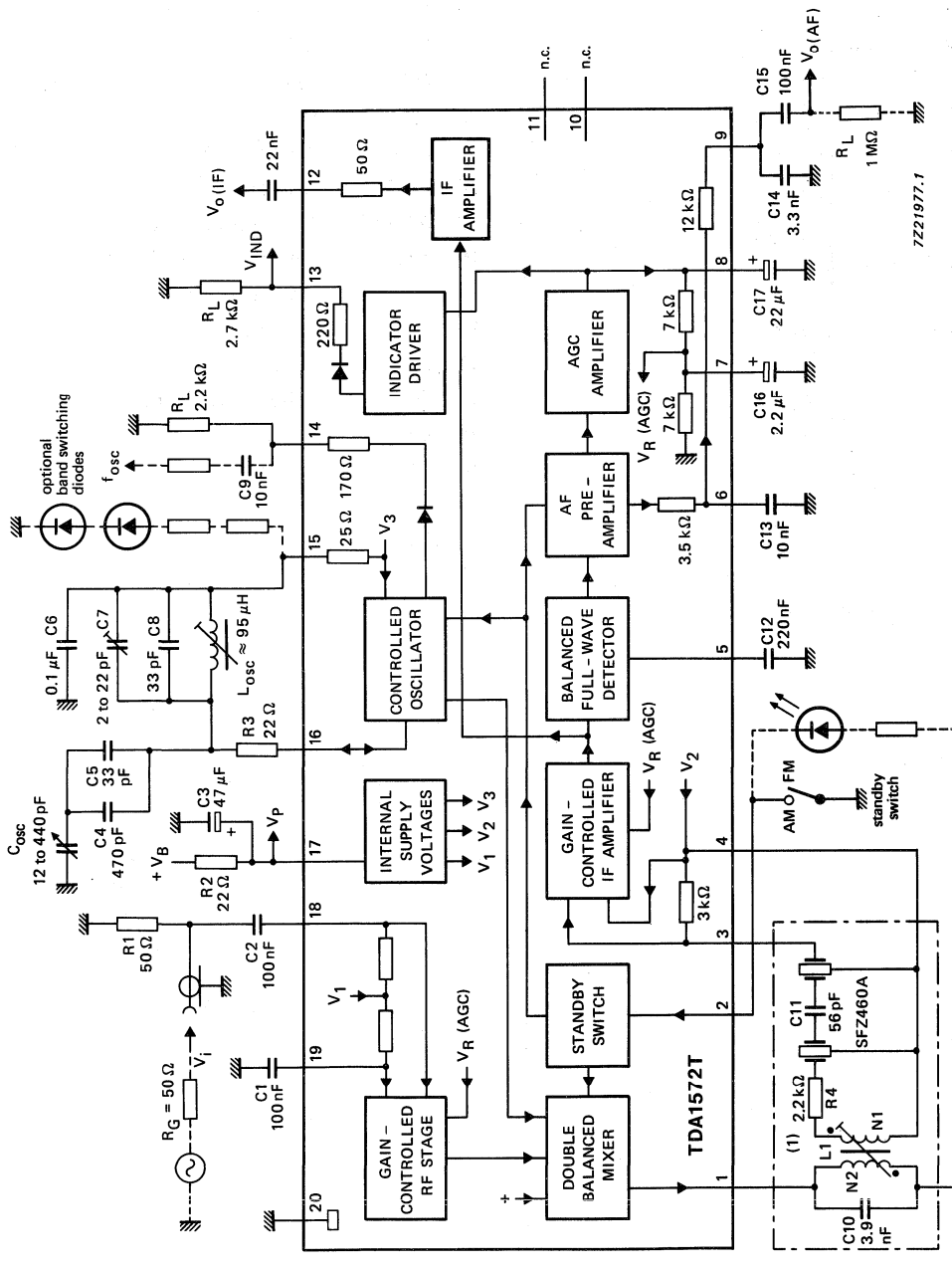
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	8.5	14.0	V
Supply current range	V_P = 8.5 V	I_P	15	25	28	mA
RF input voltage (RMS value)						
for (S + N)/N = 6 dB	m = 30%	$V_{iFR(rms)}$	–	1.5	–	μV
for THD = 3%	m = 80%	$V_{iRF(rms)}$	–	500	–	mV
IF output voltage (RMS value)	V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage (RMS value)	V_i = 2 mV(rms); f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{oAF(rms)}$	240	310	390	mV
AGC range						
Change of V_i for 1 dB change of V_{oAF}		ΔV_i	–	86	–	dB
Indicator driver (pin 13)						
Output voltage	V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_O = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4.8 kΩ.

Fig. 1 Block diagram and test circuits (connections shown in broken lines are not part of the test circuits).

PINNING

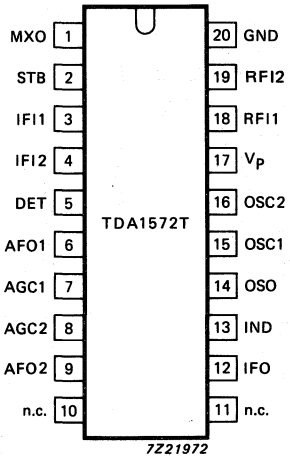


Fig.2 Pinning diagram.

1	MXO	mixer output
2	STB	standby switch
3	IFI1	IF input 1
4	IFI2	IF input 2
5	DET	detector
6	AFO1	AF output 1
7	AGC1	AGC stage 1
8	AGC2	AGC stage 2
9	AFO2	AF output 2
10	n.c.	not connected
11	n.c.	not connected
12	IFO	IF output
13	IND	indicator output
14	OSO	buffered oscillator output
15	OSC1	oscillator 1
16	OSC2	oscillator 2
17	V_P	supply voltage
18	RFI1	RF input 1
19	RFI2	RF input 2
20	GND	ground

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S + N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{15\text{-}20}$. An extra buffered oscillator putput (pin 14) is available for driving a synthesizer. If this is not needed, resistor $R_{L(14)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 12.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(13)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-20}$	–	16	V
Input voltage	$\|V_{18-19}\|$	–	12	V
	$-V_{18-19}$; $-V_{19-20}$	–	0.6	V
	V_{18-19}; V_{19-20}	–	V_P	V
Input current (pins 18 and 20)	$\|I_{18}\|$; $\|I_{20}\|$	–	200	mA
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Junction temperature	T_j	–	+125	°C
Electrostatic handling*				
all pins except pins 3, 6, 9, 14	V_{es}	−2000	+2000	V
pins 3, 6, 14	V_{es}	−1500	+2000	V
pin 9	V_{es}	−1000	+2000	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; (5 pulses, both polarities).

CHARACTERISTICS

$V_P = V_{17-20} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 17)	V_P	7.5	8.5	14.0	V
Supply current (pin 17)	I_P	15	25	28	mA
RF stage and mixer (pins 18 and 19)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$ (rms)	Z_i	–	5.5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV (rms)	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-17(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1.2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability					
Input voltage (RMS value) for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ	max.	unit
Oscillator					
Frequency range	f_{osc}	0.1	–	60	MHz
Voltage amplitude (pins 15 to 16) (RMS value)	$V_{(rms)}$	80	130	150	mV
External load impedance (pins 16 to 15)	$R_{(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation (pins 16 to 15)	$R_{(ext)}$	–	–	60	Ω
Supply voltage ripple rejection at V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log [V_{17}/V_{15}]$)	SVRR	–	55	–	dB
Source voltage for switching diodes ($6 \times V_{BE}$) (pin 15)	$V_{15\text{-}20}$	–	4.2	–	V
DC output current (for switching diodes) (pin 15)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{15} = 20 mA (switch to maximum load) (pin 15)	ΔV_I	–	0.3	–	V
Buffered oscillator output (pin 14)					
DC output voltage	V_O	–	0.8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p\text{-}p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current (peak value)	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2.0	–	V
IF input impedance (pins 3 to 4)	Z_i	2.4	3.0	3.9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4) (RMS value)	$V_{iIF(rms)}$	–	90	–	mV
IF output impedance (pin 12)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 12) (RMS value)	$V_{oIF(rms)}$	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 20)	G_v	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV(rms)	ΔV_v	–	55	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
IF, AGC and AF stages (continued)					
AF output voltage (RMS value)					
at $V_{3-4(IF)}$ = 50 μV(rms)	$V_{oAF(rms)}$	–	130	–	mV
at $V_{3-4(IF)}$ = 1 mV(rms)	$V_{oAF(rms)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2.8	3.5	4.2	kΩ
AF output impedance (pin 9)	$\|Z_o\|$	12.4	15.5	18.6	kΩ
Indicator driver (pin 13)					
Output voltage at V_i = 0 mV(rms); R_L = 2.7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V
Load resistance	R_L	1.5	–	–	kΩ
Output current at V_i = 500 mV(rms)	$-I_o$	–	–	2.0	mA
Output impedance at $-I_o$ = 0.5 mA	Z_o	–	220	–	Ω
Reverse output voltage at AM off	V_o	–	6	–	V
Standby switch					
Switching threshold at; V_P = 7.5 to 14 V; T_{amb} = −40 to +80 °C					
ON-voltage	V_{2-20}	0	–	2.0	V
OFF-voltage	V_{2-20}	3.5	–	20.0	V
ON-current at V_{2-20} = 0 V	$-I_2$	–	100	200	μA
OFF-current at V_{2-20} = 14 V	$\|I_2\|$	–	–	10	μA

OPERATING CHARACTERISTICS

V_P = 8.5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input voltage (RMS value)					
for (S + N)/N = 6 dB	$V_{iRF(rms)}$	–	1.5	–	μV
for (S + N)/N = 26 dB	$V_{iRF(rms)}$	–	15	–	μV
for (S + N)/N = 46 dB	$V_{iRF(rms)}$	–	150	–	μV
at start of AGC	$V_{iRF(rms)}$	–	30	–	μV
RF large signal handling					
RF input voltage (RMS value)					
at THD = 3%; m = 80%	$V_{iRF(rms)}$	–	500	–	mV
at THD = 3%; m = 30%	$V_{iRF(rms)}$	–	700	–	mV
at THD = 10%; m = 30%	$V_{iRF(rms)}$	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	91	–	dB
Output signal (RMS value)					
IF output voltage at V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage					
at V_i = 4 μV(rms); m = 80%	$V_{oAF(rms)}$	–	130	–	mV
at V_i = 2 mV(rms)	$V_{oAF(rms)}$	240	310	390	mV
Total harmonic distortion					
at V_i = 2 mV(rms); m = 30%	THD	–	0.5	–	%
at V_i = 2 mV(rms); m = 80%	THD	–	1.0	–	%
at V_i = 500 mV(rms); m = 30%	THD	–	1.0	–	%
Signal-to-noise ratio at V_i = 100 mV(rms)	(S+ N)/N	–	58	–	dB
Supply voltage ripple rejection at V_i = 2 mV(rms) V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log[V_P/V_{oAF}]$)	SVRR	–	38	–	dB
(a) additional AF signal at IF output	SVRR	–	0*	–	dB
(b) add modulation at IF output (m_{ref} = 30%)	SVRR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

OPERATING CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	37	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	44	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1.1	–	μA

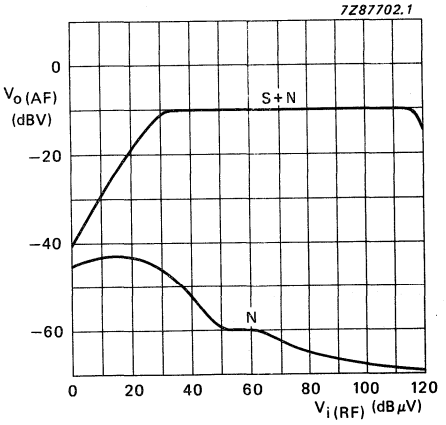


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

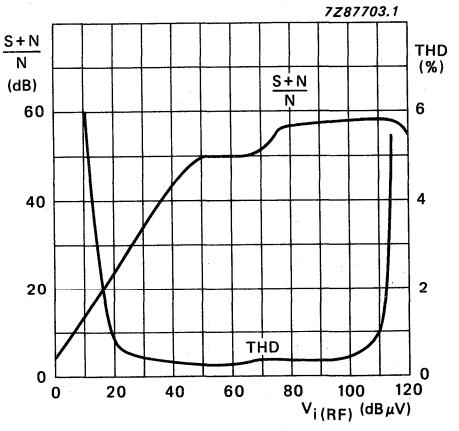


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

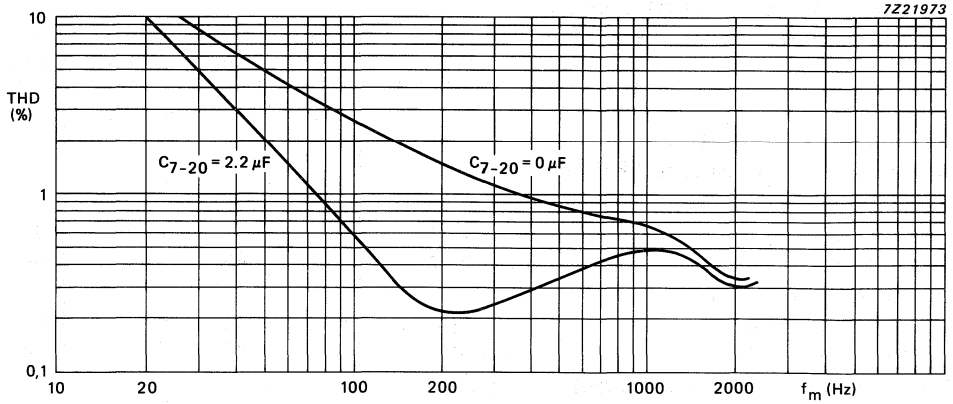


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-20(ext)}$ = 0 μF and 2.2 μF.

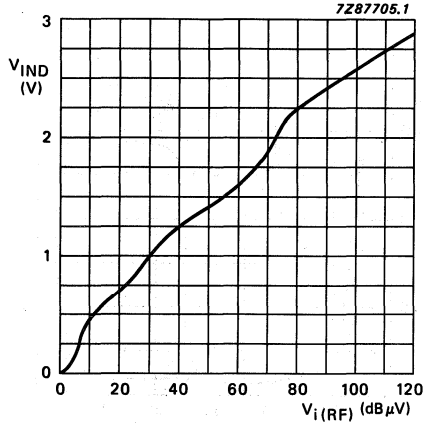
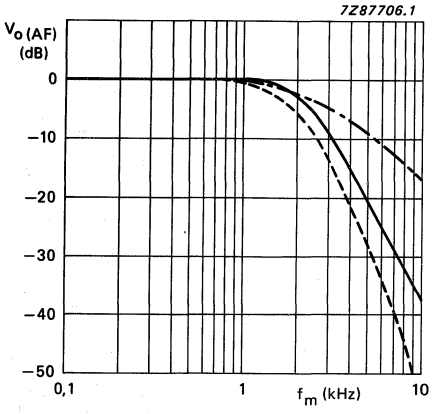


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.



——— with IF filter;
—·—·— with AF filter;
– – – – – – with IF and AF filters.

Fig.7 Typical frequency response curves from Fig.1 showing the effect of filtering.

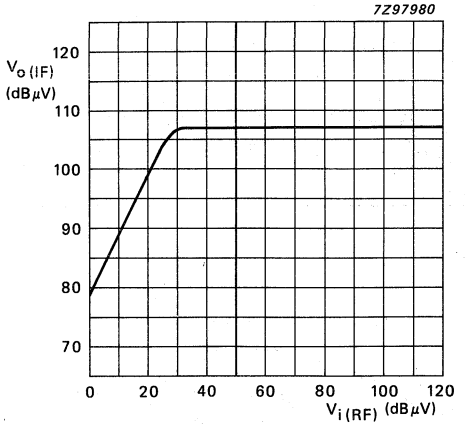


Fig.8 IF output voltage as a function of RF input in the circuit of Fig.1; f_i = 1 MHz.

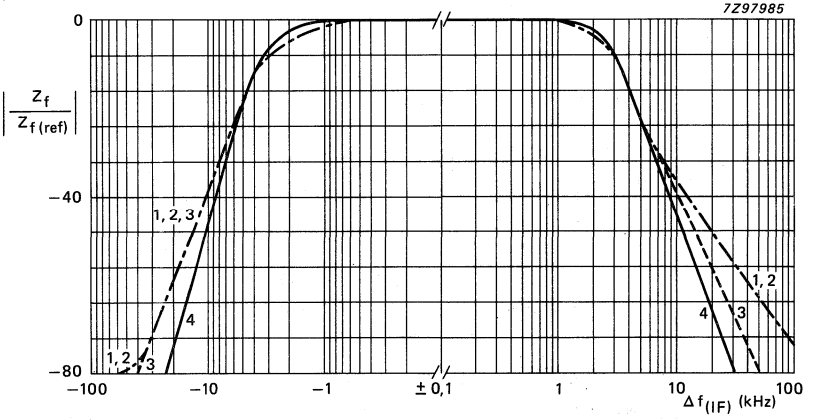


Fig.9 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.10; centre frequency = 455 kHz.

APPLICATION INFORMATION

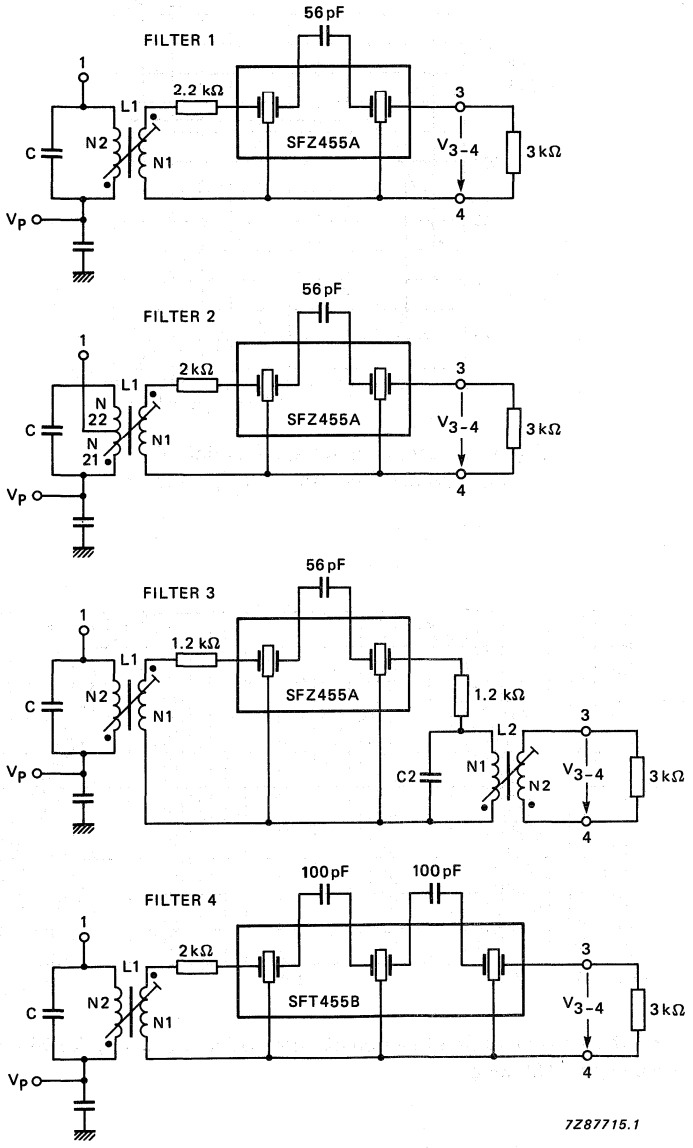


Fig. 10 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

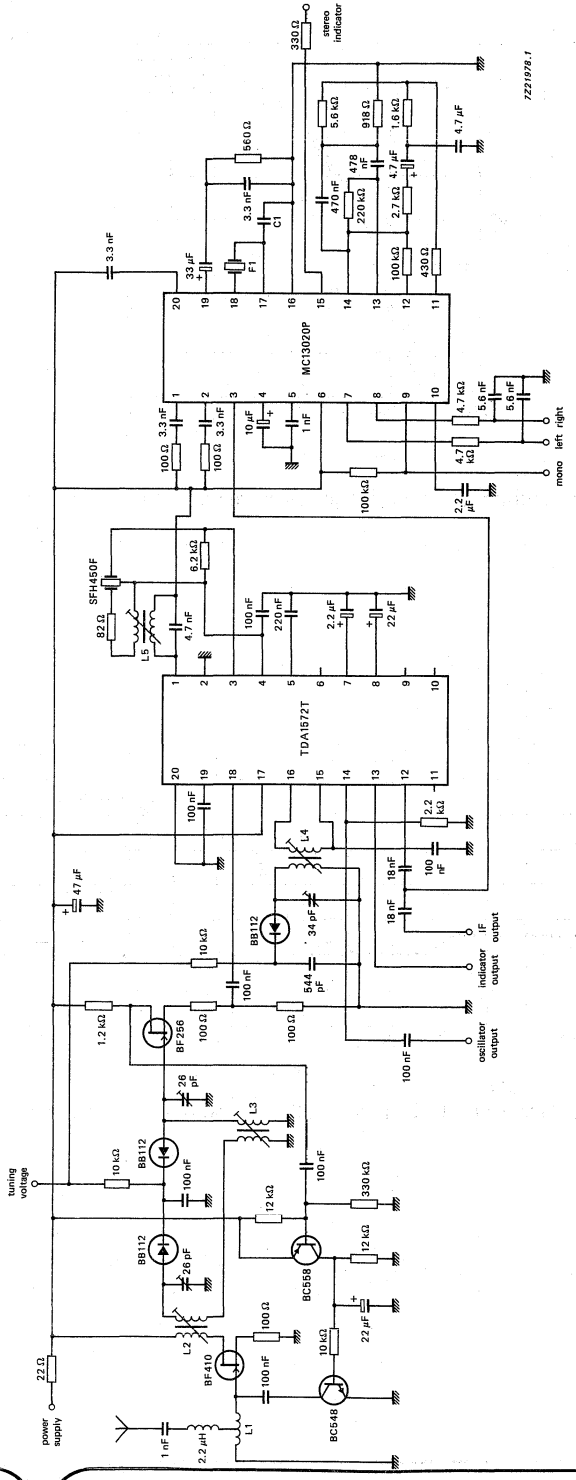


Fig.11 Application diagram.

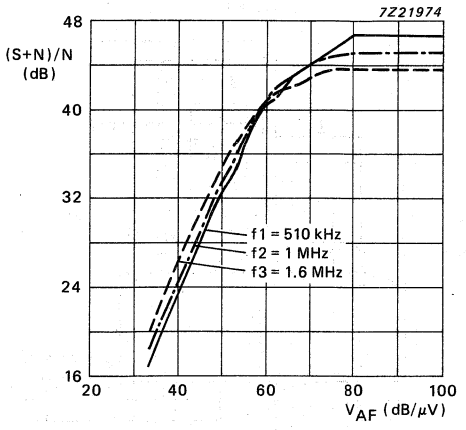


Fig.12 (S + N)/N as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

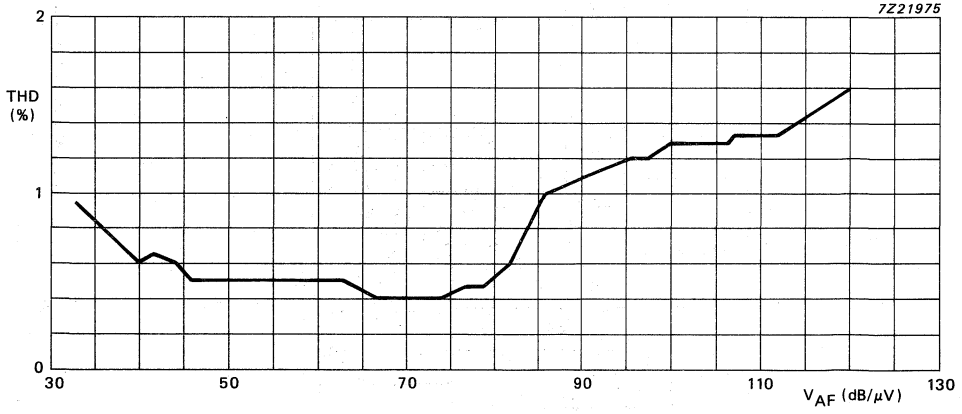


Fig.13 Total harmonic distortion (THD) as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

filter no.	1	2	3		4	5	unit
Coil data	L1	L1	L1	L2	L1	L1	
Value of C	3900	430	3900	4700	3900	4700	pF
N1 : N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	26 : 32	
Diameter of CU laminated wire	0.09	0.08	0.09	0.08	0.09	0.07	mm
Q_O	65 (typ.)	50	75	60	75	50	
Schematic* of windings	12 • • 32	13 • • 66 / 33	15 • • 31	29 • • 29 (N1) (N2)	13 • • 31	26 • • 32	
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY		
Resonators							
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	SFH450F	
D (typical value)	4	4	4		6	6	dB
R_G, R_L	3	3	3		3	2	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	10	kHz
S_{9kHz}	24	24	24		38		dB
Filter data							
Z_I	4.8	3.8	4.2		4.8	1.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	20	
Z_F	0.70	0.67	0.68		0.68	0.70	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	10	kHz
S_{9kHz}	35	31	36		42		dB
S_{18kHz}	52	49	54		64		dB
S_{27kHz}	63	58	66		74		dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

Table 1 Data for IF filters shown in Fig.10 (Filter 1 to 4) and Fig.11 (Filter 5). Criteria for adjustment is IF = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). Filter 5 is used for AM stereo application with centre frequency f_0 = 450 kHz.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16 V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2-4}$	typ.	1 V
noise figure	NF	typ.	9 dB
Oscillator output voltage (pin 6)	V_{6-4}	typ.	2 V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2 mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V_{9-4}	typ.	6 V
Total harmonic distortion	THD	typ.	−15 dBC
Linear i.f. amplifier output voltage (pin 10)	V_{10-4}	typ.	4,5 V
noise figure at R_S = 300 Ω	NF	typ.	6,5 dB
Keyed a.g.c. output voltage range (pin 18)	V_{18-4}		+ 0,5 to V_P−0,3 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

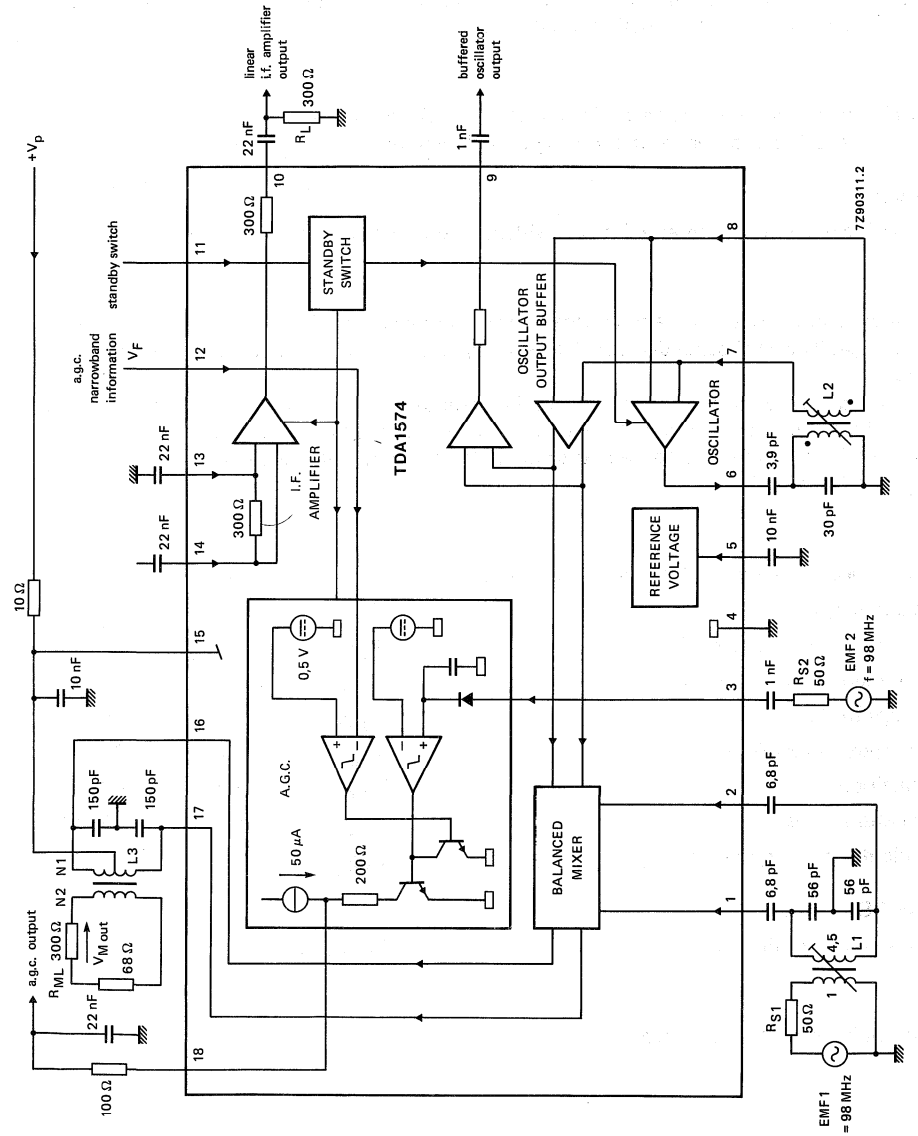


Fig. 1 Block diagram and test circuit.

Coil data

L1: TOKO MC-108, 514HNE-150014S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrowband AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\ 17-4}$	max.	35	V
Standby switch input voltage (pin 11)	V_{11-4}	max.	23	V
Reference voltage (pin 5)	V_{5-4}	max.	7	V
Field strength input voltage (pin 12)	V_{12-4}	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to +	85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15-4} = 8{,}5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	V_{5-4}	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain $10 \log \frac{4\,(V_{M(out)}\ 10{,}7\ \text{MHz})^2}{(EMF1\ 98\ \text{MHz})^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	–	1,3	–	V
Output voltage (pin 6)	V_{6-4}	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	V_{13-4}	–	1,2	–	V
Output voltage (pin 10)	V_{10-4}	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	R_{14-13}	240	300	360	Ω
	C_{14-13}	–	13	–	pF
Output impedance					
	R_{10-4}	240	300	360	Ω
	C_{10-4}	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10-4}}{V_{14-13}}$	G_{VIF}	27	30	–	dB
T_{amb} = –40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10-4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10-4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	V_{18-4}	0,5	–	V_P–0,3	V
A.G.C. output current					
at I_3 = ϕ or					
V_{12-4} = 450 mV; $V_{18-4} = V_P/2$	$-I_{18}$	25	50	100	μA
at V_{3-4} = 2 V and					
V_{12-4} = 1 V; $V_{18-4} = V_{15-4}$	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at V_{3-4} = 2 V; V_{12-4} = 550 mV	V_{18-4}	–	–	1	V
at V_{3-4} = 2 V; V_{12-4} = 450 mV	V_{18-4}	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	R_{3-4}	–	4	–	kΩ
	C_{3-4}	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at V_{12-4} = 0,7 V; $V_{18-4} = V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	V_{9-4}	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9-4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9-4(rms)}$	30	50	–	mV
D.C. output impedance	R_{9-15}	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18-4} = \geqslant V_P$–3 V	V_{11-4}	0	–	2,3	V
for threshold OFF; $V_{18-4} = \leqslant$ 0,5 V	V_{11-4}	3,3	–	23	V
Input current					
at ON condition; V_{11-4} = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; V_{11-4} = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	V_{11-4}	–	–	4,4	V

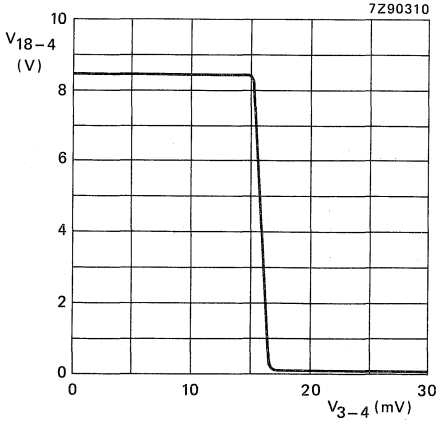


Fig. 2 Keyed a.g.c. output voltage V_{18-4} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $I_{18} = \phi$.

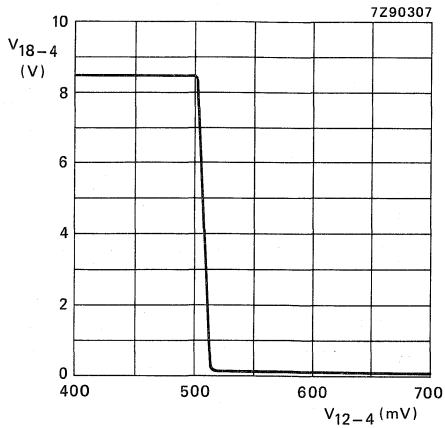


Fig. 3 Keyed a.g.c. output voltage V_{18-4} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $I_{18} = \phi$.

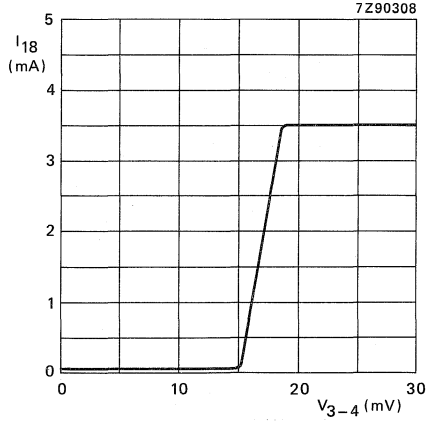


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $V_{18-4} = 8{,}5$ V.

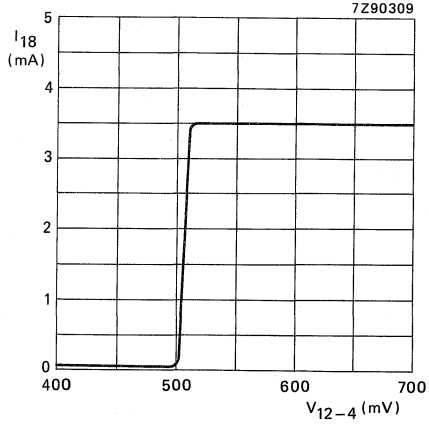


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $V_{18-4} = 8{,}5$ V.

APPLICATION INFORMATION

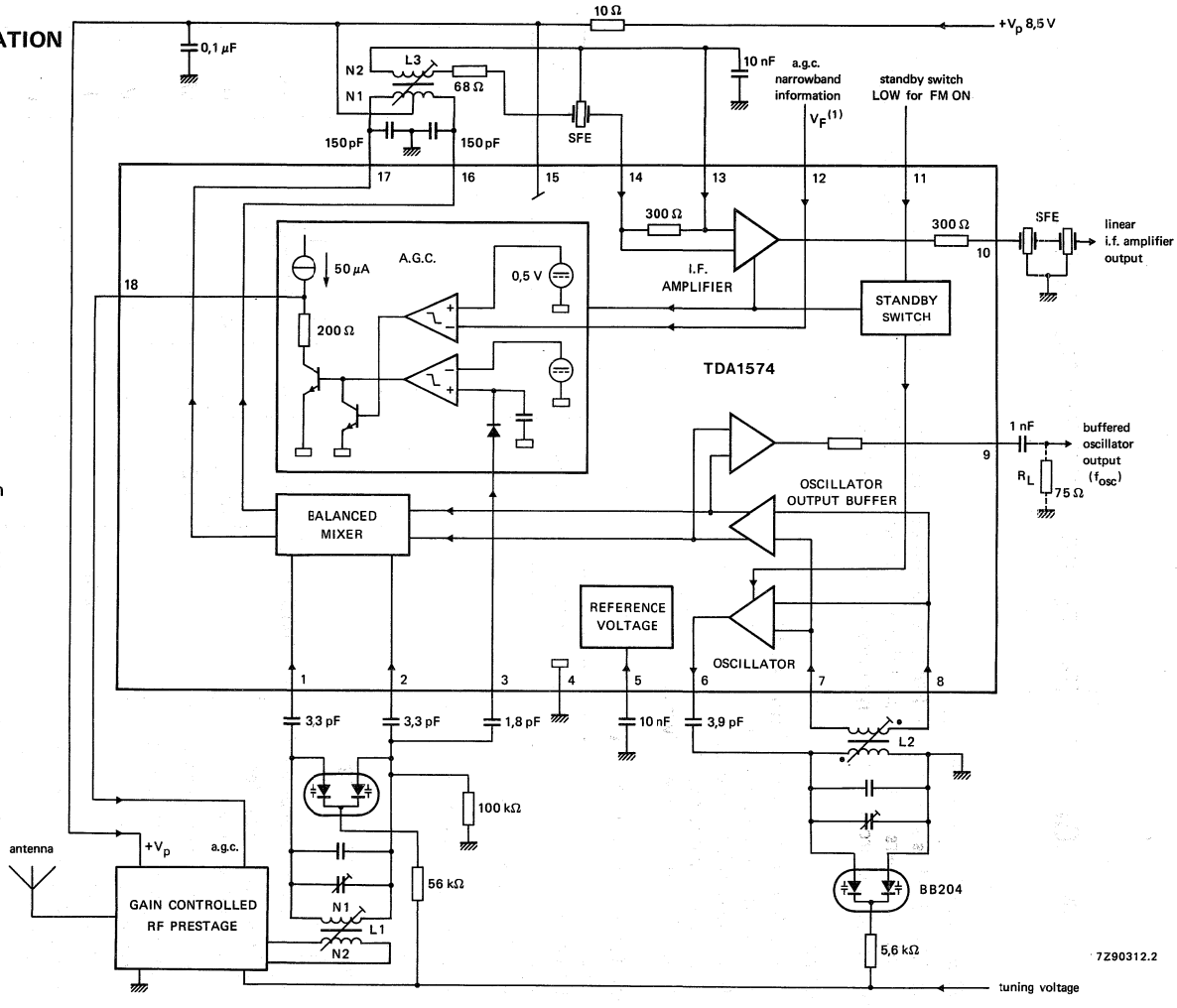


Fig. 6 TDA1574 application diagram.

Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2:
L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

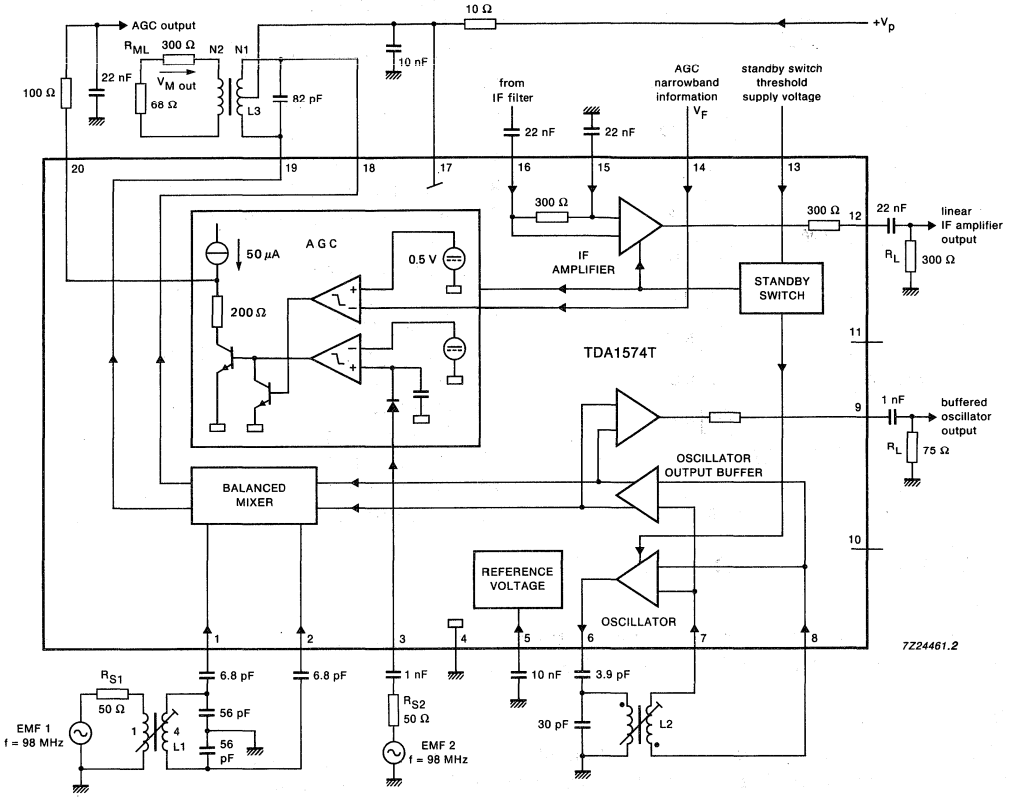
- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2-4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		V_{6-4}	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		V_{9-4}	–	6	–	V
Total harmonic distortion		THD	–	−15	–	dB
Linear IF amplifier output voltage (pin 12)		V_{12-4}	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		V_{20-4}	0.5	–	V_P−0.3	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0.08 μH
L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

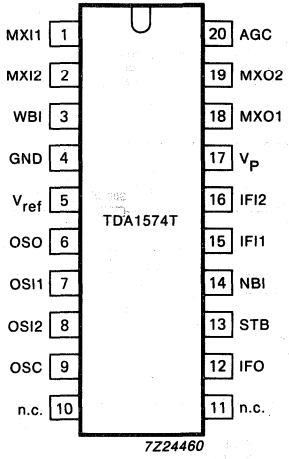


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.

The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		V_{17-4}	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19-4}$	–	35	V
Standby switch input voltage (pin 13)		V_{13-4}	–	23	V
Reference voltage (pin 5)		V_{5-4}	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 95 K/W

Note to the ratings

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{17-4} = 8.5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$	240	300	360	Ω
		$C_{16\text{-}15}$	–	13	–	pF
Output impedance		R_{12}	240	300	360	Ω
		C_{12}	–	3	–	pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = –40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P–0.3	V
AGC output current at I_3 = 0 or V_{14} = 450 mV; V_{20} = V_P/2		$-I_{20}$	25	50	100	μA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P–0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3	–	4	–	kΩ
		C_3	–	3	–	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at V_{14} = 0.7 V; $V_{20} = V_P/2$; $I_{20} = 0$		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at R_L = 75 Ω		$V_{9(rms)}$	30	50	–	mV
DC output resistance		R_{9-17}	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; R_{S1} = 50 Ω		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} = > V_P - 3$ V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} = < 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	V_{13} = 0 V	$-I_{13}$	–	–	150	μA
at OFF condition	V_{13} = 23 V	$-I_{13}$	–	–	10	μA
Input voltage	I_{13} = 0	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

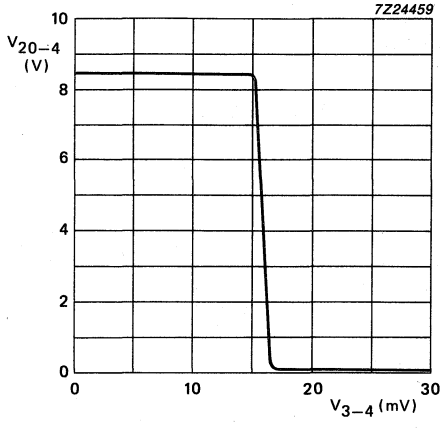


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

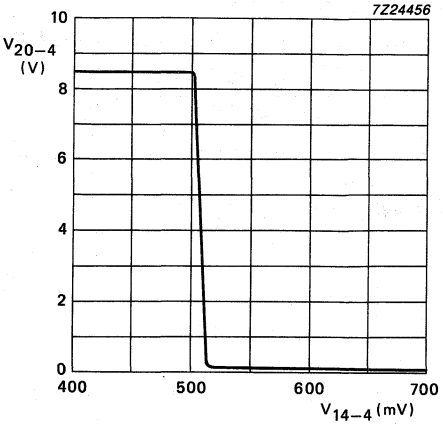


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

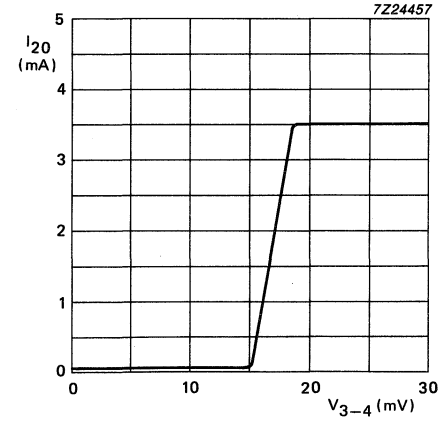


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

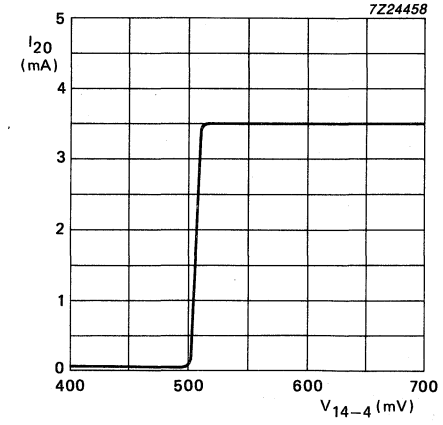
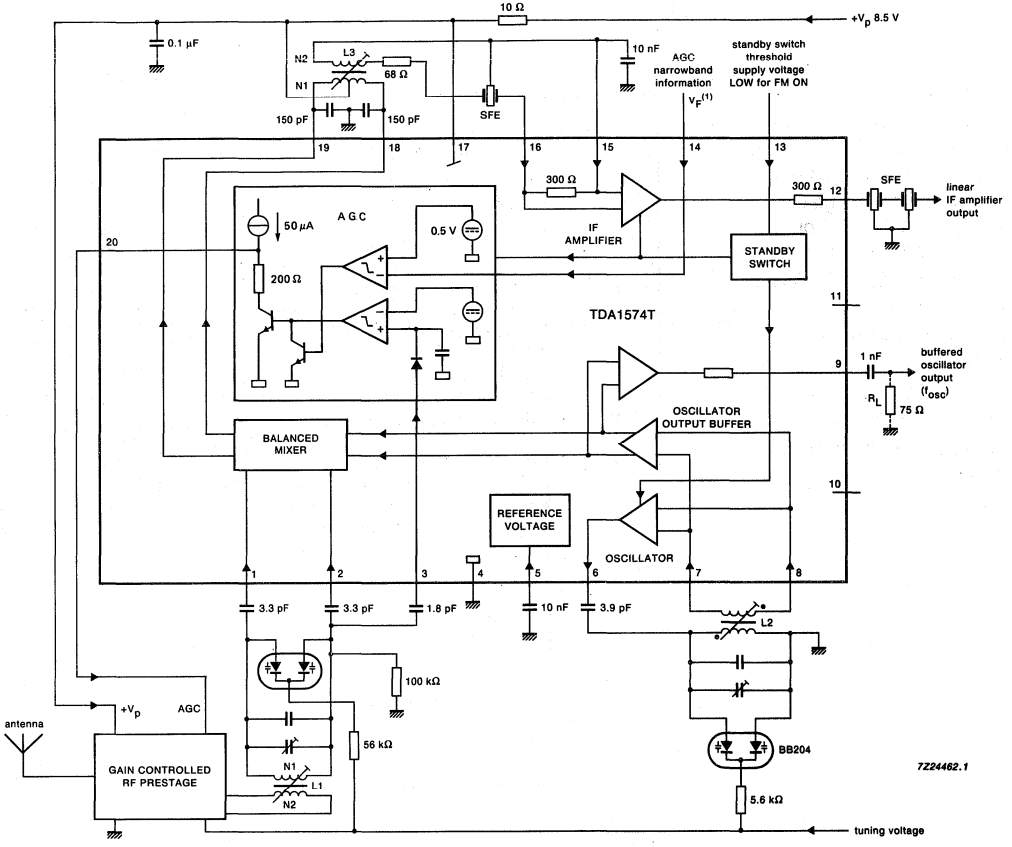


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn
L2: } see Fig.1
L3: }

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October, 1990

TDA1575T
FM tuner circuit

FEATURES

- Bipolar integrated FM tuner circuit, designed for use in car radios and home receivers
- Radio frequency range of 76 to 90 MHz (Japan) or 87.5 to 108 MHz (Europe, USA)
- Low noise oscillator, buffered oscillator output
- Double balanced mixer
- Internal buffered mixer driving
- Linear IF amplifier, suitable for ceramic IF filters
- Regulated reference voltage

QUICK REFERENCE DATA

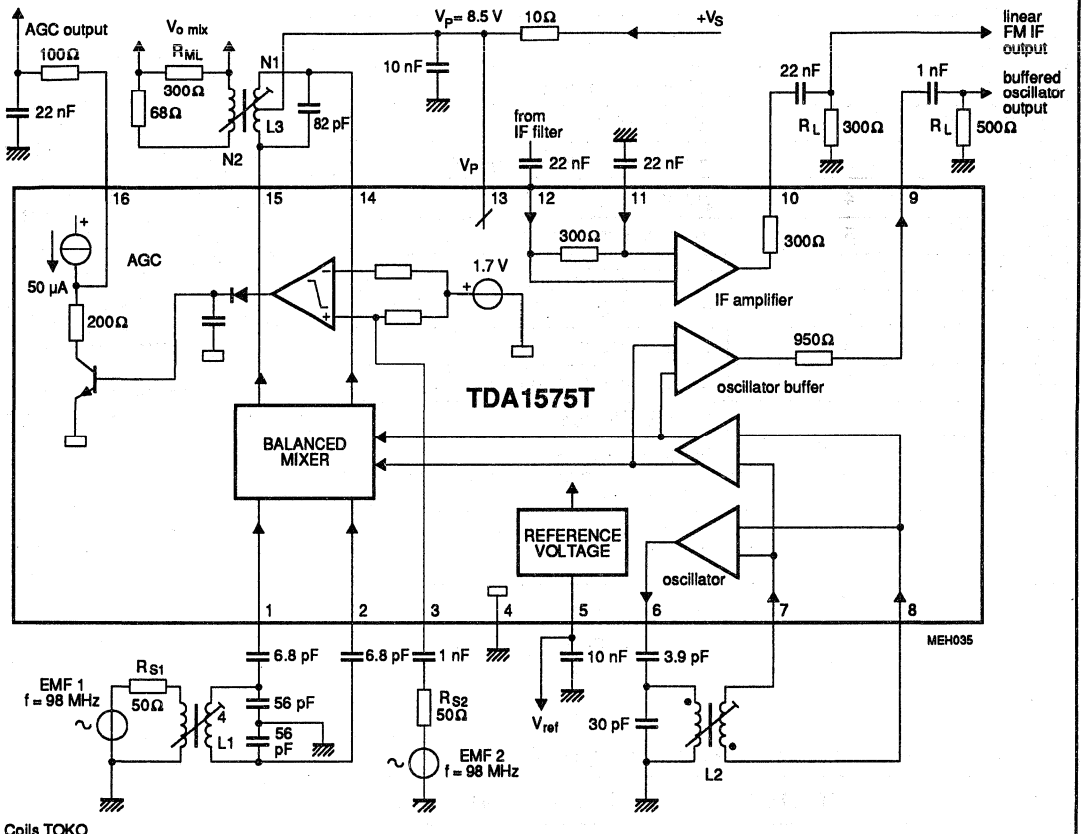
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	7	8.5	10	V
I_P	supply current, without mixer	-	23	-	mA
V_{ref}	reference voltage output	-	4.2	-	V
Z_I	mixer input impedance	-	14	-	Ω
NF	noise figure of mixer	-	9	-	dB
EMF1	3rd order intermodulation	-	115	-	dBμV
V_{osc}	oscillator buffer output signal (RMS value)	75	-	-	mV
THD	total harmonic distortion	-	–15	-	dBC
G_v	IF gain	-	30	-	dB
NF	IF noise figure	-	6.5	-	dB
Z_I	IF input impedance	-	300	-	Ω
Z_O	IF output impedance	-	300	-	Ω
EMF2	AGC wideband threshold (RMS value)	-	17	-	mV

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1575T	16	mini-pack	plastic	SOT109A

FM tuner circuit

TDA1575T



Coils TOKO
L1: MC-108 514 HNE-150023 S14; L = 78 nH, N = 4 turns
L2: MC-111 E516 HNS-200057; L = 80 nH
L3: coil set 7P; N1 = 5.5 + 5.5 turns; N2 = 4 turns

Fig.1 Block diagram and test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
MIXI1	1	RF input 1 to mixer
MIXI2	2	RF input 2 to mixer
AGCI	3	HF input to automatic gain control
GND	4	ground (0 V)
V_{ref}	5	reference voltage output
OSCO	6	oscillator output
OSCI1	7	oscillator input 1
OSCI2	8	oscillator input 2
LO	9	buffered oscillator output
IFO	10	linear FM IF output
IFI1	11	FM IF input 1
IFI2	12	FM IF input 2
V_P	13	supply voltage (+8.5 V)
MIXO1	14	mixer output 1
MIXO2	15	mixer output 2
AGCO	16	automatic gain control output

PIN CONFIGURATION

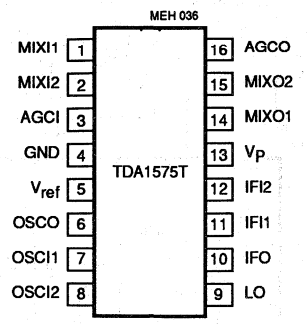


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13)	0	12	V
$V_{14, 15}$	voltage at mixer output	0	V_P	V
P_{tot}	total power dissipation	0	380	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{ESD}	electrostatic handling*			
	all pins except 3 and 10	-	±2000	V
	pin 3	-	+2000	V
		-	−1000	V
	pin 10	-	+1500	V
		-	−2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V and T_{amb} = 25 °C, measurements taken in Fig.1 with f_o = 98 MHz (EMF1) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 13)		7	8.5	10	V
I_P	supply current	without mixer	16	23	30	mA
V_{ref}	reference voltage (pin 5)	$I_5 \leq 3$ mA	3.9	4.2	4.4	V
Mixer		EMF1 = 98 MHz				
I_{14+15}	mixer supply current (pins 14 and 15)		-	4	-	mA
$V_{1,2}$	DC voltage input (pins 1 and 2)		-	1	-	V
$Z_{1,2}$	input impedance		-	14	-	Ω
$V_{14,15}$	DC output voltage (pins 14 and 15)		4	-	10	V
$C_{14,15}$	output capacitance		-	13	-	pF
G_P	conversion power gain	note 1	-	14	-	dB
$EMF1_{IP3}$	3rd order intercept point		-	115	-	dBμV
NF	noise figure		-	9	-	dB
	total noise figure	including transforming network	-	11	-	dB
Oscillator		f_{osc} = 108.7 MHz				
$V_{7,8}$	DC input voltage (pins 7 and 8)		-	1.3	-	V
V_6	DC output voltage (pin 6)		-	2.0	-	V
Δf	residual FM at pin 6	f = 300 to 15000 Hz; de-emphasis 50 μs	-	2.2	-	Hz
Oscillator buffered output (pin 9)						
V_o	output signal (RMS value)	R_L = 500 Ω; C_L = 2 pF	75	-	-	mV
V_9	DC output voltage		-	6	-	V
R_9	DC output resistor		-	950	-	Ω
THD	total harmonic distortion		-	–15	-	dBC
f_S	spurious frequencies	EMF1 = 2 V; R_S = 50Ω f_{osc} = 108.7 MHz	-	–37	-	dBC
Automatic gain control (AGC)		f_i = 98 MHz				
R_3	input resistance (pin 3)		-	4	-	kΩ
C_3	input capacitance		-	3	-	pF
V_{16}	AGC output swing (DC)	Fig.3 and 4	0.5	-	V_P–0.3	V
I_{16}	output current at I_3 = 0	V_{16} = 1/2 V_P	–25	–50	–150	μA
	output current at U_3 = 2 V	V_{16} = 7 to 10 V	2	-	5	mA
EMF2	threshold (RMS value), see figures 4 and 5	I_{16} = 0; V_{16} = 1/2 V_P	-	17	-	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear IF amplifier		IF = 10.7 MHz				
$V_{11, 12}$	DC input voltage (pins 11 and 12)		-	1.25	-	V
Z_{12-11}	input impedance		240	300	360	Ω
C_{12-11}	input capacitance		-	13	-	pF
V_{10}	DC output voltage (pin 10)		-	4.4	-	V
Z_{10}	output impedance		240	300	360	Ω
C_{10}	output capacitance		-	3	-	pF
V_o	output signal (RMS value)	–1 dB compression	-	-	650	mV
G_v	IF voltage gain (20 log (V_{10-4} / V_{12-11}))		27	30	-	dB
ΔG_v	IF voltage gain deviation	T_{amb} = –40 to +85 °C	-	0	-	dB
NF	noise figure	R_S = 300 Ω	-	6.5	-	dB

Note to the characteristics

1. $G_P = 10 \log (4V_{o\ mix} \times 10{,}7\ MHz) / (EMF2 \times 98\ MHz)^2 \times (R_{S1} / R_{ML})$

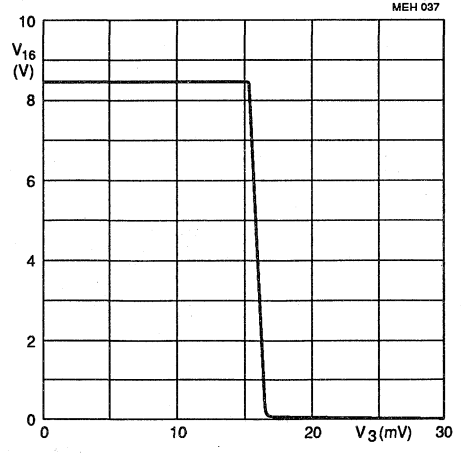


Fig.3 AGC output voltage V_{16} as a function of $V_{i\ 3\ (rms)}$ at I_{16} = 0, measured in test circuit Fig.1.

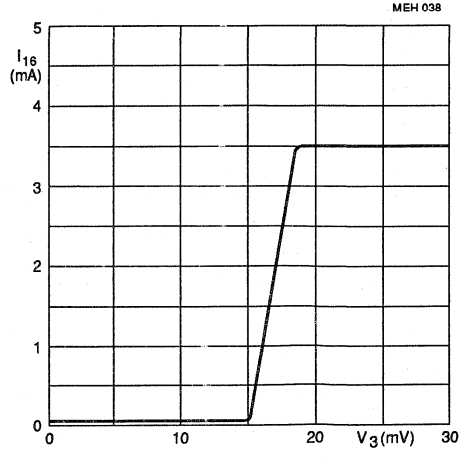


Fig.4 AGC output current I_{16} as a function of $V_{i\ 3\ (rms)}$ at V_{16} = 8.5 V, measured in test circuit Fig.1.

APPLICATION INFORMATION

Operating characteristics

Measurements taken with figure 6, according to "Amtsblatt 69, Kapitel 5.1.1. (Eingangs-Störfestigkeit). Measurements are shown in figure 7.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage (range in brackets)		(7)	8.5	(10)	V
I_S	total supply current			37		mA
f_{RF}	tuning range of RF input		87.5	-	108	MHz
V_{tune}	tuning voltage of RF input		1	-	7	V
G	gain (20 log $V_{o\ IF}$ / V_{ant})		-	43	-	dB
$V_{i\ ant}$	input sensivity	S/N = 26 dB; R_{ant} = 150 Ω	-	3	-	µV
IR	image rejection	f = 98 MHz	-	58	-	dB
RSS	repeat spot suppression	f = 98 MHz; $V_{i\ ant}$ = 10 µV	-	95	-	dB
DBS	double beat suppression	f1 = 93 MHz; f2 = 98 MHz				
	DBS1	f_{tune} = 88 MHz	-	82	-	dB
	DBS2	f_{tune} = 103 MHz	-	73	-	dB
	DBS3	f_{tune} = 90.15 MHz	-	88	-	dB
CBS	continous beat suppression	f1 = 90 MHz; f2 = 100.7 MHz				
		f_{tune} = 95 MHz	-	87	-	dB

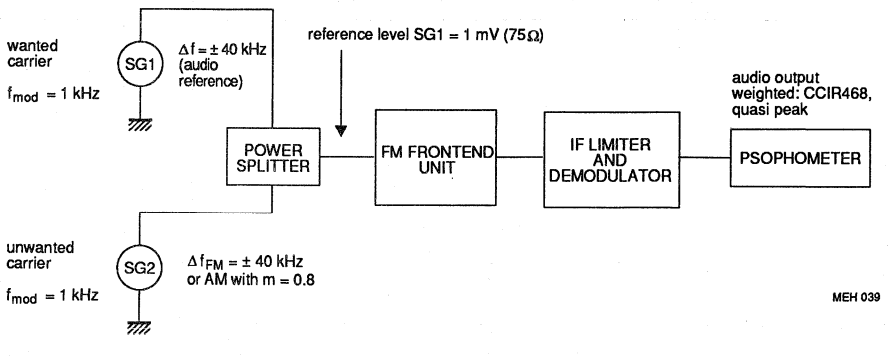


Fig.5 Set-up for "Amtsblatt" measurments.

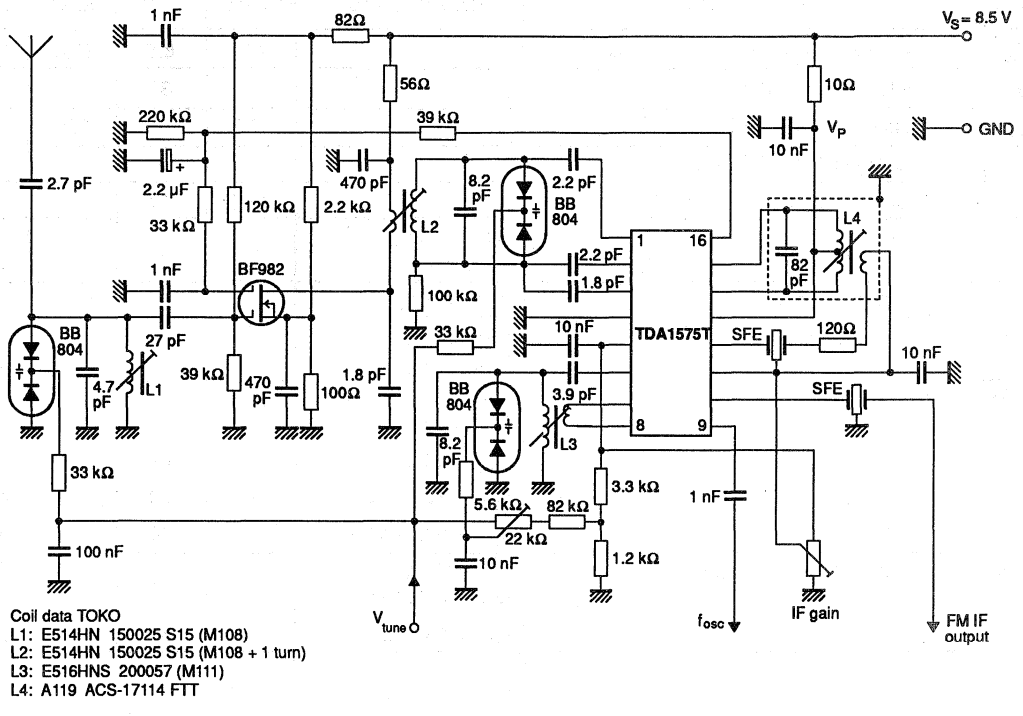
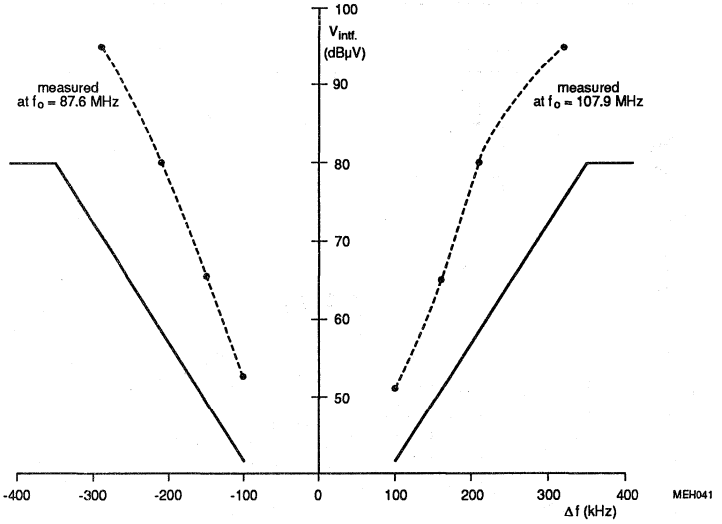


Fig.6 Application circuit of a FM-Tuner with TDA1575T and FET-preamplifier.



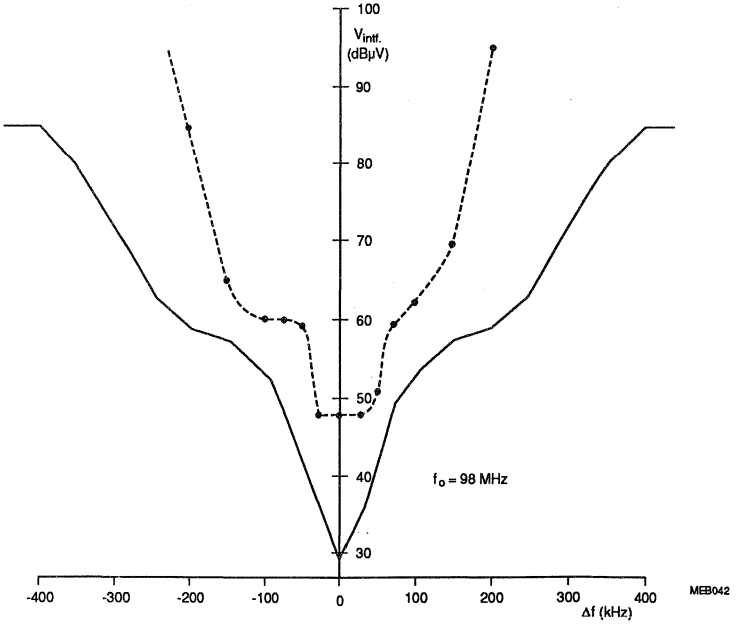


Fig.7 Interference level V_{intf} as a function of detuning for S/N = 26 dB; interference-carrier AM-modulated according to "Amtsblatt 69".

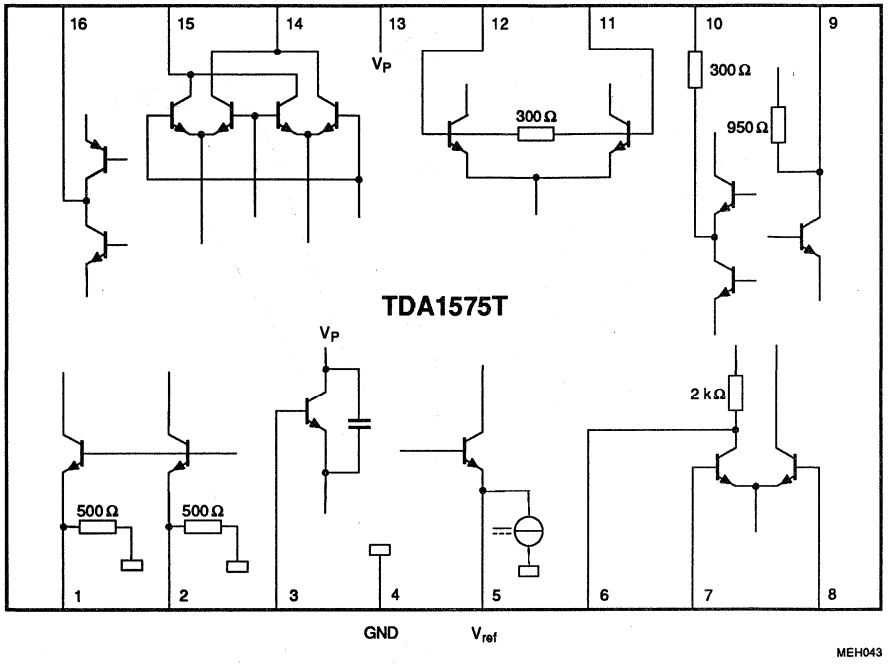


Fig.8 Internal circuits.

Data sheet	
status	Preliminary specification
date of issue	February 1991

TDA1576T
FM-IF amplifier/demodulator circuit

FEATURES

- Fully balanced 4-stage limiting IF amplifier
- Symmetrical quadrature demodulator
- Field-strengh indication output for 1 mA ammeter
- Detune detector for side response and noise attenuation
- Detune voltage output
- Internal muting circuit
- 0° and 180° AF output signals
- Reference voltage output
- Electronic smoothing of the supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)	7.5	8.5	15	V
I_P	supply current	10	16	23	mA
V_{iIF}	input sensivity (RMS value)				
	–3 dB before limiting	14	22	35	µV
	S/N = 26 dB	-	10	-	µV
	S/N = 46 dB	-	55	-	µV
V_{oAF}	AF output signal (RMS value)	-	67	-	mV
THD	total harmonic distortion with double resonant circuits	-	0.02	-	%
S/N	signal-to-noise ratio (V_i > 1 mV)	-	72	-	dB
α_{AM}	AM suppression	-	50	-	dB
RR	ripple rejection (f = 100 Hz)	43	48	-	dB
I_{15}	maximum indicator output current	-	-	2	mA
T_{amb}	operating ambient temperature	–30	-	+80	°C

GENERAL DESCRIPTION

The TDA1576T is a monolithic integrated FM-IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1576T	20	mini-pack	plastic	SOT163A

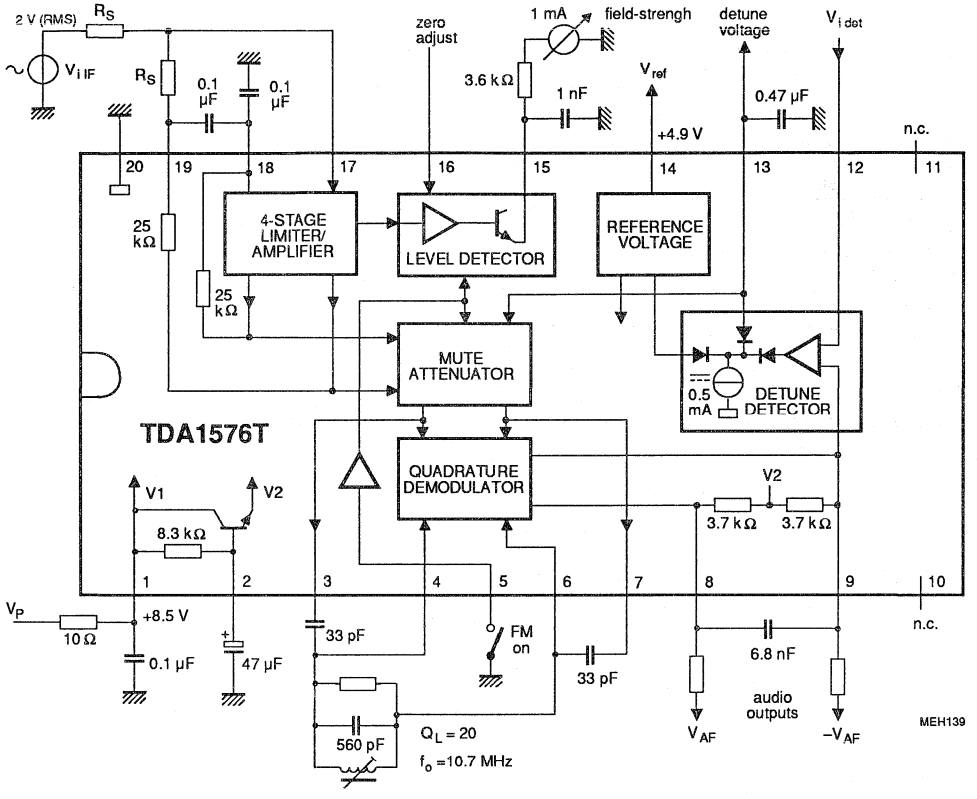


Fig.1 Block diagram and application circuit.

FM-IF amplifier/demodulator circuit TDA1576T

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit
IF2	7	IF signal to resonant circuit
$V_{o\ AF1}$	8	AF output voltage (0° phase)
$V_{o\ AF2}$	9	AF output voltage (180° phase)
n.c.	10	not connected
n.c.	11	not connected
$V_{i\ det}$	12	detune detector input for external audio reference
$V_{o\ det}$	13	detune detector output voltage
V_{ref}	14	reference voltage output
V_F	15	level output for field-strengh
$V_{F\ o}$	16	zero adjust for field-strengh
$V_{i\ IF}$	17	FM-IF input signal
IN2	18	input 2 of differential IF amplifier
IFLV	19	IF input level
GND	20	ground (0 V)

PIN CONFIGURATION

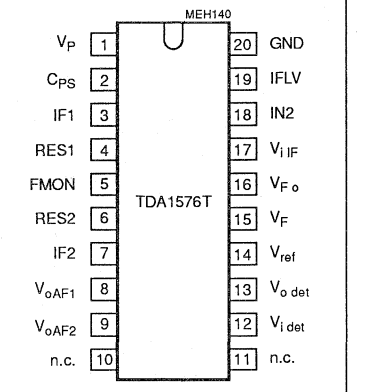


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	15	V
$V_{2, 5, 16}$	voltage on pins 2, 5 and 16	0	V_P	V
P_{tot}	total power dissipation	0	450	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	−30	+85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	85	K/W

CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 µs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for $V_{i\,ZF}$ = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	15	V
I_P	supply current	$V_5 = V_9 = V_{13} = 0$	10	16	23	mA
Reference voltage						
V_{ref}	reference voltage (pin 14)	I_{14} = −1 mA	-	4.9	-	V
ΔV_{ref}	reference voltage dependence on temperature	$\Delta V_{14} / V_{14} * \Delta T$	-	0.3	-	%/K
I_{14}	maximum output current	short-circuit current	4	6	7.5	mA
R_{14}	output resistor ($\Delta V_{14} / \Delta I_{14}$)	I_{14} < 1.2 mA	-	60	150	Ω
IF amplifier						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	−3 dB before limiting	14	22	35	µV
$R_{17\text{-}18}$	input resistance	$V_{i\,IF}$ = 200 mV (RMS)	10	-	-	kΩ
$C_{17\text{-}18}$	input capacitance	$V_{i\,IF}$ = 200 mV (RMS)	-	5	-	pF
$V_{o\,IF}$	output signal at pins 3 and 7 (peak-to-peak value)	$Z_{3,7}$ = 10 pF // 1MΩ	610	680	750	mV
$R_{3\text{-}7}$	output impedance		200	250	300	Ω
Demodulator						
$R_{4\text{-}6}$	input resistance		20	30	40	kΩ
$C_{4\text{-}6}$	input capacitance		-	1	2.5	pF
$R_{8,9}$	output impedance		2.9	3.7	4.5	kΩ
$V_{8,9}$	DC offset voltage on output pins at $V_{4\text{-}6}$ = 0	V_5 > 3 V or $V_{3\text{-}7}$ = 0 or V_{13} < 0.3 V	-	0	±100	mV
$\Delta V/\Delta\varphi$	demodulator efficiency	$\Delta V_{8\text{-}9}/\Delta\varphi$	-	40	-	mV/°
	demodulator efficiency dependent on supply voltage (note 1)	K	-	6.2	-	mV/°
V/V	DC voltage ratio	$V_{8+}V_9 / 2*V_2$	0.653	0.667	0.680	V/V
$\Delta V/\Delta T$	dependence on temperature	$\Delta(V_8+V_9 / 2*V_2)/\Delta T$	-	10^{-5}	-	1/K
Field-strengh output						
V_{15}	output voltage (Fig.4)	$V_{i\,IF}$ = 0	0	0.1	0.25	V
		$V_{i\,IF}$ = 1 mV (RMS)	1.1	1.5	1.9	V
		$V_{i\,IF}$ = 250 mV (RMS)	3.2	3.6	4.1	V
S	control steepness	Fig.4	-	0.85	-	V/dec
R_{15}	output resistance		-	150	200	Ω
$\Delta V/\Delta T$	dependence on temperature	$V_{i\,IF} = \Delta V_{15} / (\Delta T * V_{15})$	-	0.3	-	%/K
I_{15}	stand-by operational cut-off current	$V_5 \geq 3$ V; V_{15} = 0 to 5 V	-	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero level adjustment						
V_{16}	internal bias voltage		-	260	-	mV
R_{16}	input resistance		-	19	-	kΩ
S	control steepness	$V_{i\,IF}$ = 100 mV; $A = \Delta V_{15}/\Delta V_{16}$	0.87	1.0	1.2	V/V
Detuning detector						
I_{12}	input bias current		-	20	100	nA
R_{12}	input resistance (Fig.5)	5 V/ΔI_{12}	6	30	-	MΩ
V_{13}/V_{14}	output voltage ratio for $\Delta\varphi = \varphi$ (pins 3-7) – φ (pins 4-6) –90°; (Fig.6)	$V_1 = V_2$ = 7.5 V; $R_{13\text{-}14}$ = 10 kΩ; pins 9 and 12 short-circuit				
	$\Delta\varphi$ = 9.2° (43 kHz), Q = 20	$V_{9,\,12}$ = 334 mV	0.45	0.5	0.55	V/V
	$\Delta\varphi$ = 3.5° (16 kHz), Q = 20	$V_{9,\,12}$ = 138 mV	0.75	0.8	0.85	V/V
	$\Delta\varphi$ = 14° (65 kHz), Q = 20	$V_{9,\,12}$ = 501 mV	0.335	0.345	0.355	V/V
I_{13}	maximum output current (Fig.7)	V_{13} = 6 V	0.4	0.5	0.6	mA
	cut-off current	V_{13} = 2.5 V; $V_{9,\,12}$ = 0	-	-	–100	nA
Internal audio attenuation						
V_{13}/V_{14}	output voltage ratio (Fig.8)	α = attenuation factor				
	for α = 1 dB		0.11	0.12	0.13	
	for α = 7.2 dB		0.095	0.1	0.105	
	for α ≥ 40 dB		-	0.06	-	
I_{13}	input current	$V_{13} / V_{13} \leq 0.1$	-	-	–225	nA
Stand-by switch						
V_5	input voltage for FM-on	$V_{3,\,7} / V_{3,\,7(max)}$ = 0.9	2.4	2.5	-	V
	input voltage for FM-off	V_{19} = 0.3 V	-	2.9	3	V
	linear range (Fig 9)		-	350	-	mV
I_5	input current	V_5 = 0 to 2 V	-	-	–100	µA
		V_5 = 3.5 to 15 V	-	-	1	µA
$V_5/\Delta T$	temperature dependence	FM-on ($3.5V_{BE}$)	-	7	-	mV/K
		FM-off ($5V_{BE}$)	-	10	-	mV/K
Supply voltage smoothing						
$V_{1\text{-}2}$	internal voltage drop	proportional to $V_1 - 3V_{BE}$	80	210	400	mV
$R_{1\text{-}2}$	internal resistor		5.8	8.3	10.8	kΩ

OPERATING CHARACTERISTICS

V_P = 8.5 V; $f_{i\,ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 μs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion with $V_{i\,ZF}$ = 1 mV.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
$V_{i\,IF}$	input sensivity (RMS value, pin 17)	–3 dB before AF limiting	14	22	35	μV
	input signal for S/N = 26 dB	f = 250 to 15000 Hz	-	10	-	μV
	input signal for S/N = 46 dB	f = 250 to 15000 Hz	-	55	-	μV
$V_{o\,AF}$	output signal at (RMS value, pins 8 and 9)		60	67	75	mV
$V_{o\,N}$	noise voltage for $V_{i\,IF}$ = 0 (RMS value, pins 8 and 9)	R_S = 300 Ω f = 250 to 15000 Hz	-	900	-	μV
	weighted noise voltage according to	DIN 45405	-	2	-	mV
S/N	signal-to-noise ratio Fig.3 (pin 8 and 9)	$V_{i\,IF}$ = 1 mV (RMS)	-	72	-	dB
α_{AM}	AM suppression	$V_{i\,IF}$ = 0.5 to 200 mV FM: 70 Hz, ±15 kHz AM: 1 kHz, m = 30%	-	50	-	dB
$\alpha_{FM.}$	FM rejection for FM-off	$V_{i\,IF}$ = 500 mV; V_5 = 3V	80	-	-	dB
$\Delta V_{8,9}$	AFC shift in relation to minimum second harmonic distortion α_{2H}	$V_{i\,IF}$ = 0.03 to 500 mV	-	25	-	mV
	DC offset at second harmonic distortion	operating	-	0	±100	mV
		mute or FM-off	-	0	±50	mV
α_{3H}	distortion for third harmonic		-	0.65	-	%
RR	ripple rejection V_{ripple} = 200 mV on V_P	f = 100 Hz	43	48	-	dB

Note to the characteristics

1. $V_{8\text{-}9} / \Delta\varphi = K(V_P - 3\,V_{BE})$

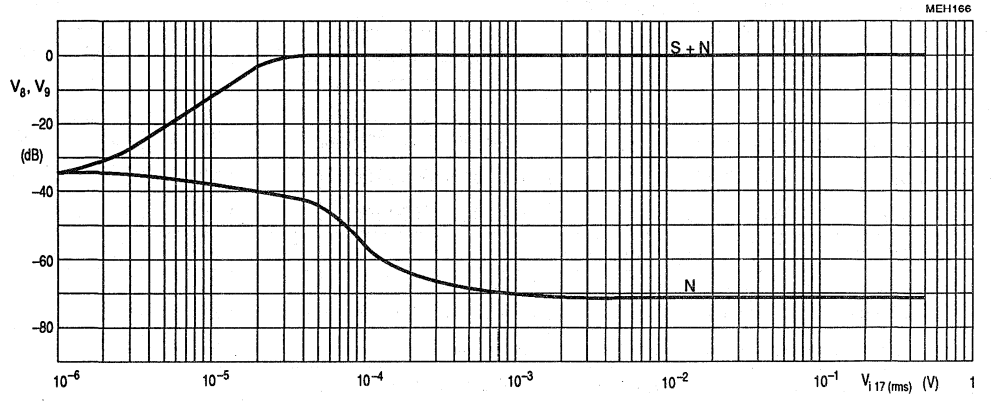


Fig.3 AF output voltage level on pins 8 and 9 as a function of $V_{i\,IF}$ at V_P = 8.5 V; f_m = 1 kHz; Q_L = 20 and with de-emphasis. S = signal; N = noise.

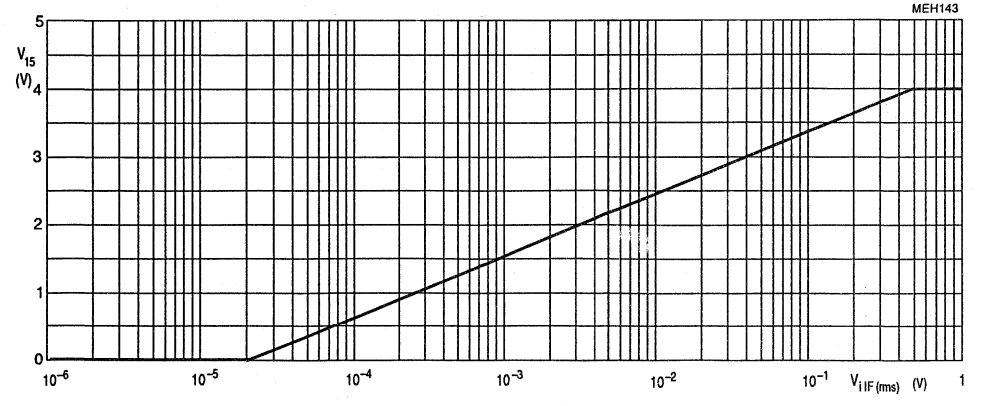


Fig.4 Field-strengh output (I_{16} = 0).

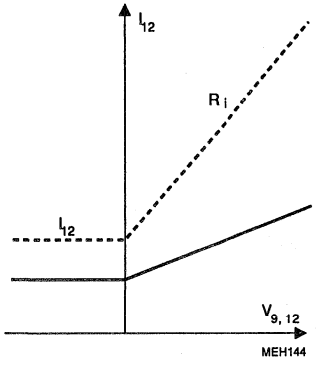


Fig.5 Detuning input impedance.

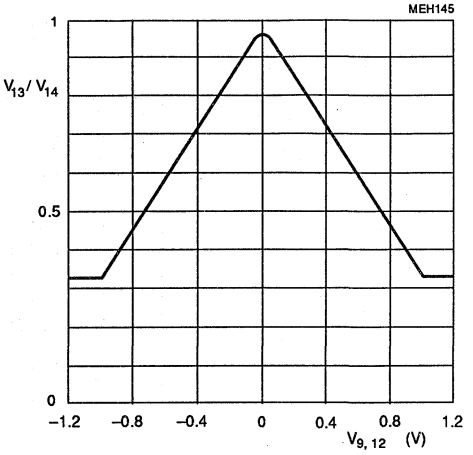


Fig.6 Detuning curve.

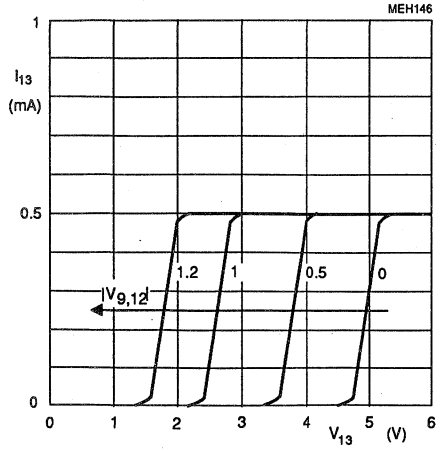


Fig.7 Detuning output.

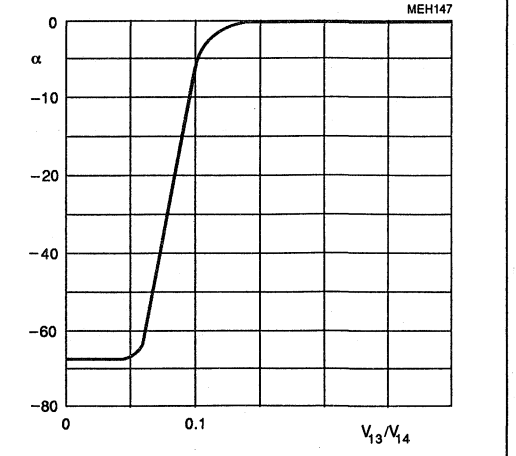


Fig.8 Internal audio attenuation.

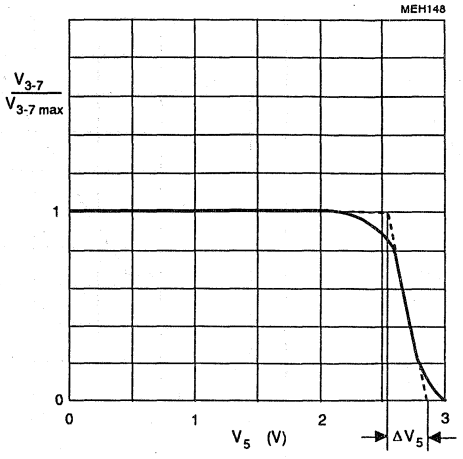


Fig.9 Stand-by switch.

TIME MULTIPLEX PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

QUICK REFERENCE DATA

Measured with a frequency deviation $\Delta f = \pm 75$ kHz without pilot; $f_m = 1$ kHz					
Supply voltage (pin 8)	$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)	$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)	$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)	R_i	typ.		47	kΩ
A.F. output voltage (R = 15 kΩ)	V_o	typ.	0,75	1,5	V
Output resistance	R_o			low-ohmic	
Spread in gain	ΔG_v	⩽		1	dB
Channel separation	α	typ.		50	dB
Total harmonic distortion	THD	⩽		0,3 | 0,1	%
Signal-to-noise ratio	S/N	typ.		90	dB
Carrier and harmonic suppression					
pilot signal; f = 19 kHz	α_{19}	typ.		32	dB
subcarrier; f = 38 kHz	α_{38}	typ.		50	dB
f = 57 kHz	α_{57}	typ.		46	dB
f = 76 kHz	α_{76}	typ.		60	dB
traffic radio (V.W.F.); f = 57 kHz	$\alpha_{57(VWF)}$	typ.		70	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz	α_{67}	typ.		70	dB
ACI (Adjacent Channel Interference); f = 114 kHz	α_{114}	typ.		80	dB
intermodulation; f = 10/13 kHz	α_2, α_3	typ.		70	dB
Supply voltage range (pin 8)	$V_P = V_{8-7}$			7,5 to 18	V
Operating ambient temperature range	T_{amb}			−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

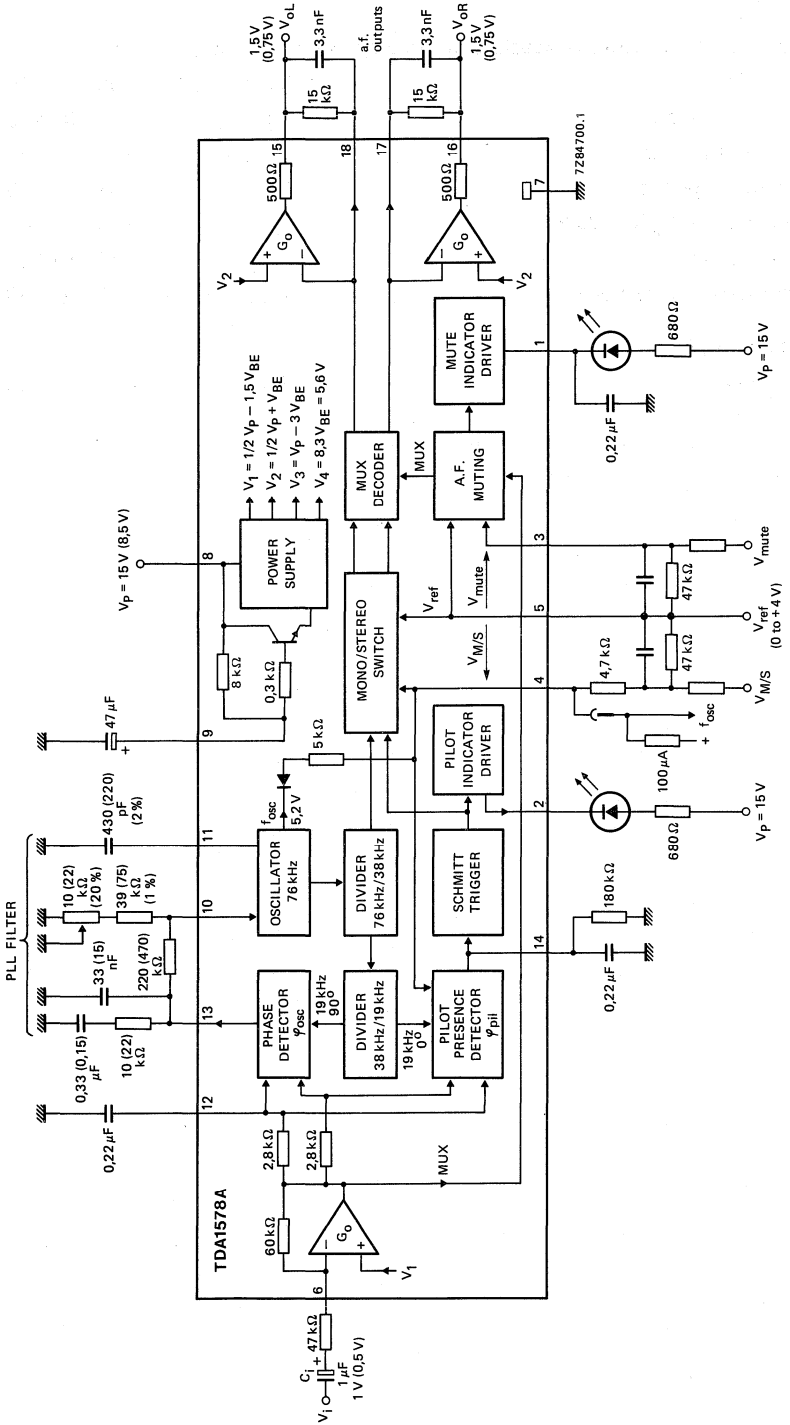


Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for V_P = 8,5 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-7}$	max.	20	V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5-7}$		0 to 12	V
Indicator driver output voltage	$V_{1;2-7}$	max.	24	V
Indicator driver output current	$I_1; I_2$	max.	30	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c-a}$	=	80	K/W

CHARACTERISTICS (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz);
modulation frequency: 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V;
de-emphasizing time: T = 50 μs; oscillator adjusted to f_{osc} at a pilot voltage $V_i = 0$ V;
$T_{amb} = 25\ ^{o}C$; unless otherwise specified

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	–	V_P	7,5	–	18	V
Supply current (except output and indicator) pin 8	8,5	I_P	–	21	–	mA
	15	I_P	–	30	40	mA
Nominal multiplex input voltage (peak-to-peak value)	8,5	$V_{MUX(p\text{-}p)}$	–	0,5	–	V
$R_i = 47$ kΩ	15	$V_{MUX(p\text{-}p)}$	–	1,0	–	V
Overdrive reserve of input						
at THD = 1 %	8,5		3	6	–	dB
at THD = 0,3 %	15		3	6	–	dB
A.F. output voltage (r.m.s. value; mono without pilot)						
$R_{15\text{-}18} = R_{16\text{-}17} = 15$ kΩ	8,5	$V_{o(rms)}$	–	0,75	–	V
	15	$V_{o(rms)}$	–	1,5	–	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	8,5	$V_{o(rms)}$	–	1,2	–	V
	15	$V_{o(rms)}$	–	2,4	–	V
Overdrive reserve of output $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	*		3	–	–	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	–	–	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15\text{-}16}/V_o$	–	–	1	dB
Output resistance	*	R_o	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	–	–	–	mA
Modulation range at output (unloaded)	*	$V_{15;16\text{-}7}$	–	1 to $V_{9\text{-}7} - 1$	–	V
Internal current limiting	*	I_o	–	15	–	mA
D.C. output voltage	8,5	$V_{15;16\text{-}7}$	3,6	4,1	4,6	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	15	$V_{15;16\text{-}7}$	7,0	7,7	8,4	V
D.C. current	8,5	$-I_{17;18}$	–	33	–	μA
(pins 17 and 18)	15	$-I_{17;18}$	–	23	–	μA

* $V_P = 8{,}5$ or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Channel separation	8,5	α	32	50	–	dB
at V_{4-5} = 0 V	15	α	39	50	–	dB
Total harmonic distortion	8,5	THD	–	0,1	0,3	%
	15	THD	–	0,04	0,1	%
Signal-to-noise ratio	8,5	S/N	–	87	–	dB
f = 20 Hz to 16 kHz	15	S/N	–	90	–	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	*	α_{38}	40	50	–	dB
f = 57 kHz	*	α_{57}	–	46	–	dB
f = 76 kHz	*	α_{76}	–	60	–	dB
intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz						
PLL-filter Fig. 1	*	α_2	–	50	–	dB
PLL-filter Fig. 2	*	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	*	α_3	–	75	–	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	–	70	–	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	*	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3);						
f = 114 kHz	*	α_{114}	–	80	–	dB
f = 190 kHz	*	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV (pin 8)	*	RR_{100}	40	43	–	dB
Voltage on filter capacitor without external load	*	V_{9-7}	–	V_P–0,25	–	V
Source resistance	*	R_{9-8}	6	8	10	kΩ

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Mono/stereo control						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	$V_{i(p-p)}$	–	21	30	mV
	15	$V_{i(p-p)}$	–	43	61	mV
for mono 'ON'	8,5	$V_{i(p-p)}$	6	15	–	mV
	15	$V_{i(p-p)}$	12	30	–	mV
Switch hysteresis $V_{i\,ON}/V_{i\,OFF}$	*	ΔV_i	–	3	–	dB
Switching time at $C_{14-7} = 0{,}22\ \mu F$						
for stereo 'ON'	*	$t_{st\,ON}$	–	15	–	ms
for mono 'ON'	*	$t_{m\,ON}$	–	27	–	ms
External mono/stereo control (see Fig. 12 and note 5)						
Switching voltage for external mono control	8,5	V_{14-7}	–	–	0,7	V
	15	V_{14-7}	–	–	1,4	V
	*	or: $-V_{4-5}$	315	–	–	mV
Control voltage for channel separation: $\alpha = 6$ dB	8,5	$-V_{4-5}$	–	120	–	mV
	15	$-V_{4-5}$	–	130	–	mV
	*	ΔV_{4-5}	–	–	± 20	mV
$\alpha = 26$ dB	8,5	$-V_{4-5}$	–	70	–	mV
	15	$-V_{4-5}$	–	80	–	mV
Control voltage for mono 'ON'	8,5	$-V_{4-5}$	–	240	–	mV
	15	$-V_{4-5}$	–	270	–	mV
for stereo 'ON'	8,5	$-V_{4-5}$	–	220	–	mV
	15	$-V_{4-5}$	–	250	–	mV
Control voltage difference for $\alpha = 6$ dB; stereo 'ON'	8,5	ΔV_{4-7}	80	100	120	mV

* $V_P = 8{,}5$ or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Muting circuit (see Fig. 13 and note 5)						
Control voltage for an attenuation: α = 3 dB	8,5	$-V_{3-5}$	–	140	–	mV
	15	$-V_{3-5}$	–	145	–	mV
	*	ΔV_{3-5}	–	± 20	–	mV
α = 26 dB	8,5	$-V_{3-5}$	–	255	–	mV
	15	$-V_{3-5}$	–	270	–	mV
Attenuation						
with V_{3-5} = 0 V	*	α	–	–	0,2	dB
with $-V_{3-5}$ = 450 mV	*	α	–	80	–	dB
LED driver output current at an attenuation: α = 3 dB	*	I_1	1,2	1,7	2,2	mA
Control voltage for I_1 = 200 μA	8,5	$-V_{3-5}$	–	150	–	mV
	15	$-V_{3-5}$	–	160	–	mV
Control inputs						
Recommended voltage range	*	$V_{3;4;5-7}$	0	–	4	V
Input bias current	*	$I_{3;4;5}$	–	10	100	nA
Indicator driver						
Output saturation voltages at I_1 = 20 mA; V_{3-5} = 0 V	*	V_{1-7sat}	–	1,2	1,8	V
at I_2 = 20 mA	*	V_{2-7sat}	–	0,5	1,0	V
Output leakage current at $V_{1;2-7}$ = 24 V	*	$I_{1;2}$	–	20	–	μA

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
VCO						
Oscillator frequency adjustable with R_{10-7}	*	f_{osc}	–	76	–	kHz
Spread of free-running frequency at nominal external circuitry	*	f_{osc}	71	–	82	kHz
Free-running frequency dependency (note 6)						
with temperature	*	TC	–	1×10^{-4}	–	K^{-1}
with supply voltage	*	$\Delta f_{osc}/\Delta V_P$	–	–	400	Hz/V
Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\,nom}$	*	$\Delta f/f$	± 2	–	–	%
PLL control slope (total)	*	S_{tot}	–	4,5	–	kHz/μs
D.C. voltage at pin 10	*	V_{10-7}	–	2,1	–	V
		or:	–	3,2 V_{BE}	–	V
Frequency measuring point; internal switching threshold	*	V_{4-7}	–	6	–	V
		or:	–	9 V_{BE}	–	V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	$V_{4-7(p-p)}$	–	350	–	mV
Output resistance	*	R_{4-7}	–	5	–	kΩ

* V_P = 8,5 or 15 V.

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (2 \times 10\ kHz) - 19\ kHz$$

$$\alpha_3 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (3 \times 13\ kHz) - 38\ kHz$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz \pm 23\ kHz)}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 110\ kHz - (3 \times 38\ kHz)$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 186\ kHz - (5 \times 38\ kHz)$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal;
1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 9\ kHz)};\ f_s = (2 \times 38\ kHz) - 67\ kHz$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal;
10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q}$ = 28,6 mV at T_j = 330 K.

6. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at pin 12 (C_{12-7}): phasing 19/38 kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

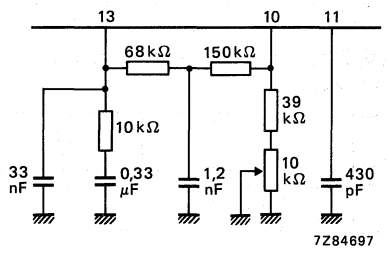


Fig. 2 PLL-filter for α_2 = 70 dB at V_P = 15 V (see also Fig. 1).

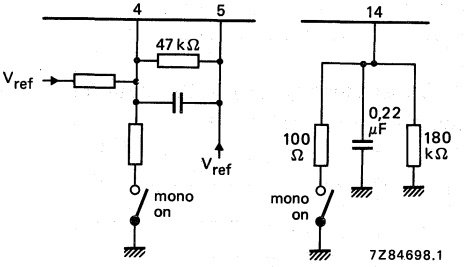


Fig. 3 (a) At pin 4; $-V_{4-5} > 300$ mV; (b) at pin 14.

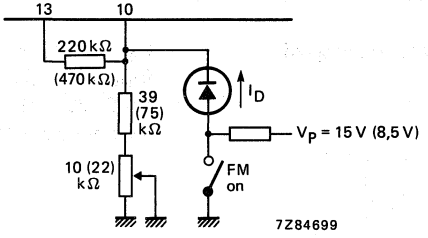


Fig. 4 The oscillator is switched-off when: $I_D > 100$ μA (> 50 μA for V_P = 8,5 V) and $I_D < 1$ mA.

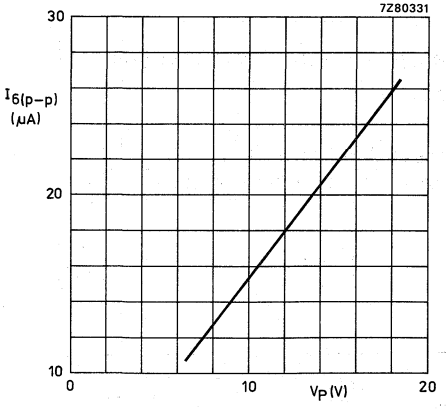


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9-7} = V_P$.

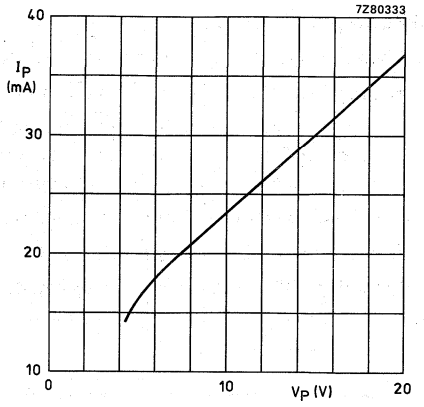


Fig. 6 Supply current comsumption at $V_{9-7} = V_P$.

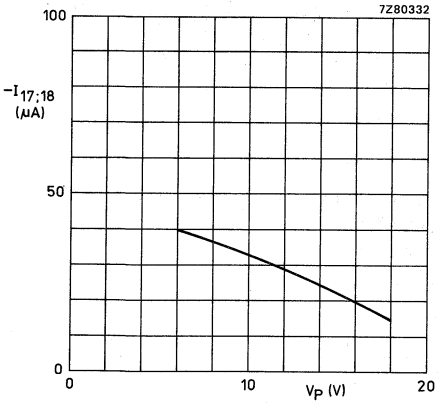


Fig. 7 D.C. current in the feedback loop of the output amplifier.

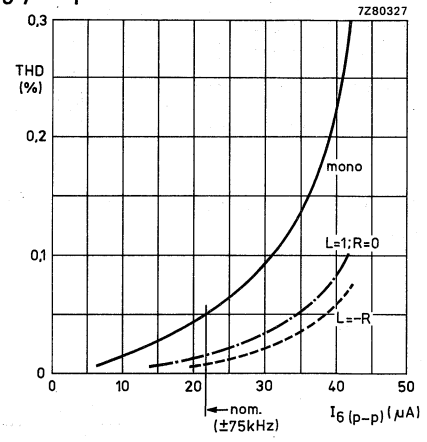


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; V_P = 15 V; f_m = 1 kHz; $V_{3-5} = V_{4-5}$ = 0 V.

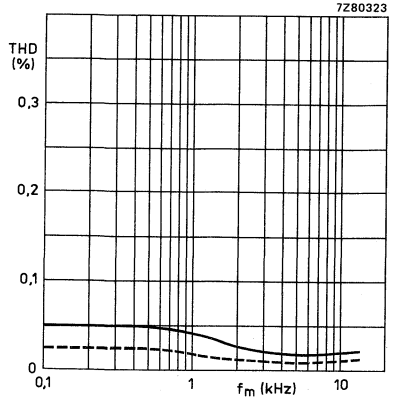


Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency (f_m); V_P = 15 V; $I_{6(p-p)}$ = 21,5 μA.

——— mono

– – – – stereo; L = –R; 91% + 9% pilot signal.

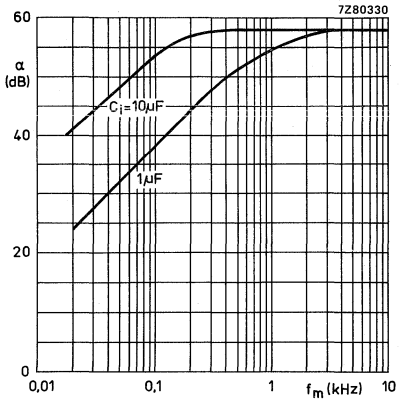


Fig. 10 Channel separation (α) as a function of the modulation frequency (f_m); V_P = 15 V; R_i = 47 kΩ; V_{4-5} = 0 V.

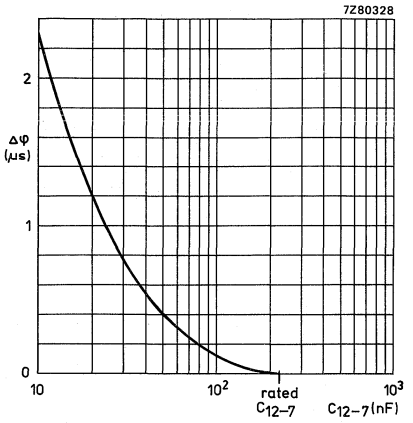


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of C_{12-7}.

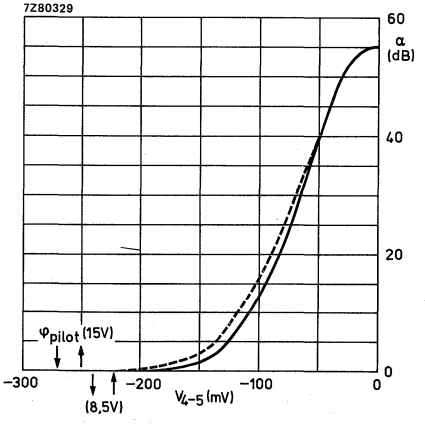


Fig. 12 Mono/stereo control at f_m = 1 kHz; α is the channel separation.
——— V_P = 8,5 V
– – – – V_P = 15 V

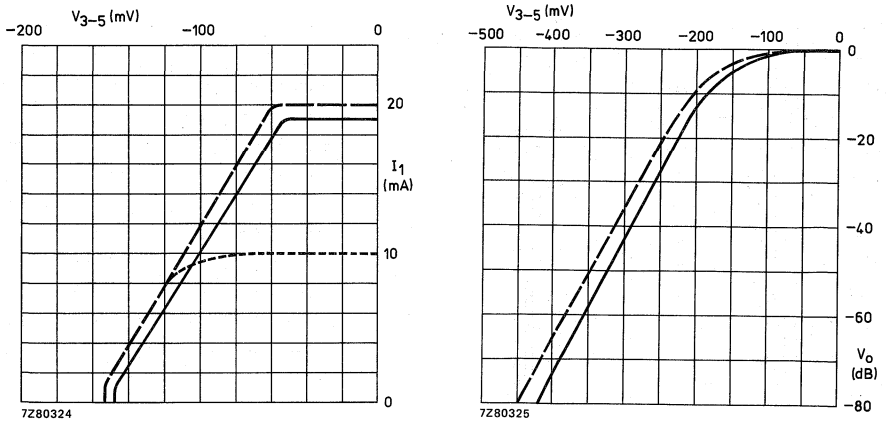


Fig. 13 Muting (V_o) and muting indicator current (I_1) as a function of V_{3-5}.

V_o in dB curves; ——— V_P = 8,5 V
– – – – V_P = 15 V

I_1 in mA curves for V_{PL}/R_{bias1} (pin 1); – – – – 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - - 10 V/680 Ω

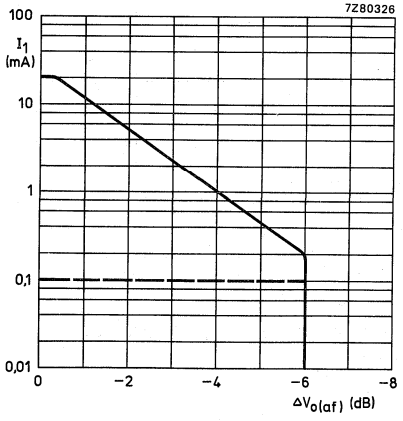


Fig. 14 Muting indicator current; V_P = 8,5 to 15 V; V_{PL} = 14 V.

——— R_{bias1} = 680 Ω
– – – – R_{bias1} = matched

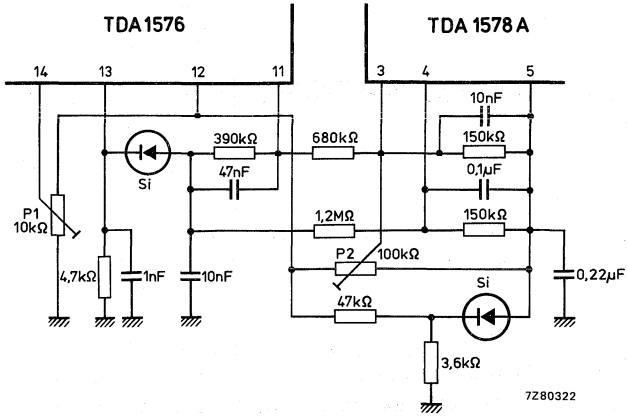


Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)}$ = 100 μV with P1 to α = 6 dB (channel separation),
at $V_{i(hf)}$ = 15 μV with P2 to $V_{o(af)}$ = −3 dB.

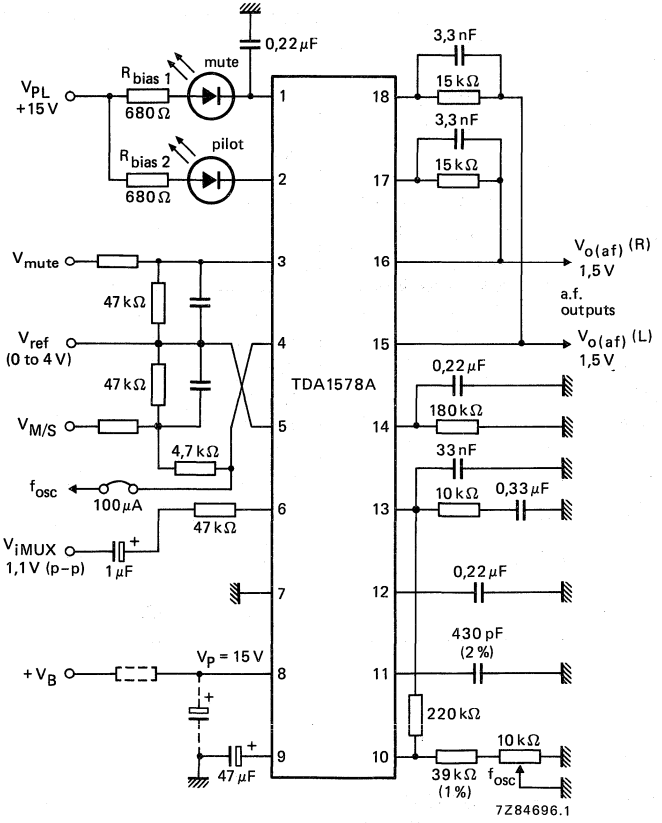


Fig. 16 Typical application circuit using TDA1578A for V_P = 15 V.

DECODER FOR TRAFFIC WARNING (VWF) RADIO TRANSMISSIONS

GENERAL DESCRIPTION

The TDA1579 decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the German 'Verkehrs Warnfunk' (VWF) traffic warning system.

Features

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- Driver output for SK indicator (LED)
- SK and BK control outputs

QUICK REFERENCE DATA

Measured in Fig. 1 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	7.5	8.5	12	V
Supply current		I_P	–	6	–	mA
Nominal input voltage	at f = 57 kHz	V_{iSK}	–	8	–	mV
Input impedance	at f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Control level	−3 dB	V_{iSK}	–	2.4	–	mV
Input voltage	peak-to-peak value	$V_{i(p-p)}$	2	–	–	V
SK switch-on threshold level		m_{BKon}	–	42	–	%
SK switch hysteresis		Δm_{BK}	–	3.5	–	dB
SK switch-on delay		t_{dSKon}	–	150	–	ms
SK switch-off delay		t_{dSKoff}	–	750	–	ms
DK switch-on threshold level		m_{DKon}	–	13	–	%
DK switch hysteresis		Δm_{DK}	–	3.6	–	dB
DK switch-on delay		t_{dDKon}	–	750	–	ms
DK switch-off delay		t_{dDKoff}	–	750	–	ms
Ambient operating temperature range		T_{amb}	−30	–	+ 80	°C

PACKAGE OUTLINES

TDA1579: 18-lead DIL; plastic (SOT102).
TDA1579T: 20-lead mini-pack; plastic (SO20; SOT163A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
All pin numbers in this table apply to TDA1579; for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	$V_P = V_{7\text{-}18}$	–	–	15	V
Switch output voltage	pin 1	$V_{1\text{-}18}$	–	–	23	V
	pins 2 or 3	$V_{2;3\text{-}18}$	–	–	15	V
	pins 1, 2 or 3	$-V_{1;2;3\text{-}18}$	–	–	0.5	V
Switch output current	pin 1	I_1	–	–	50	mA
	pins 2 or 3	$I_{2;3}$	–	–	5	mA
	pins 1, 2 or 3	$-I_{1;2;3}$	–	–	10	mA
Signal input voltage	pin 13	$V_{13\text{-}18}$	–	–	V_P	
	pin 13	$-V_{13\text{-}18}$	–	–	0.5	V
Signal input current	pin 13	$-I_{13}$	–	–	10	mA
Total power dissipation		P_{tot}	–	–	800	mW
Storage temperature range		T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range		T_{amb}	−30	–	+ 80	°C

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal.
All pin numbers in this table apply to TDA1579, for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	V_P	7.5	–	12	V
Supply current	pin 7	I_P	–	6	10	mA
SK amplifier/decoder						
Input impedance	f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Input voltage (peak-to-peak value)		$V_{i(p\text{-}p)}$	2	–	–	V
Input voltage at start of gain control	V_{o9BK} = −3 dB	V_{iSK}	–	2.4*	–	mV
Voltage gain	V_{9BK}/V_{13SK}	$G_{v9\text{-}13}$	–	44*	–	dB

* Selectable by $R_{12\text{-}8}$ or $Z_{10\text{-}8}$.

parameter	conditions	symbol	min.	typ.	max.	unit
SK amplifier/decoder (continued)						
Gain spread		$\pm \Delta G_{v9\text{-}13}$	–	–	2	dB
Gain control range		ΔG_v	40	–	–	dB
Controlled output voltage		V_{o9BK}	–	440	–	mV
		V_{o9DK}	–	220	–	mV
BK circuit						
Switch-on threshold level	pin 3 high-Z	V_{o5BKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{o5BKon}}{V_{o5BKoff}}$	3	3.5	4	dB
BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8\text{-}18}$)	pin 3 conducting	$V_{4\text{-}18off}$	0.8	0.88	0.97	V
SK output (pin 3)						
allowable load current		I_3	–	–	1.5	mA
saturation voltage	I_3 = 1.5 mA	$V_{3\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_3 < 5\ \mu A$	$V_{3\text{-}18}$	18	–	–	V
Indicator driver (pin 1)						
allowable load current		I_1	–	–	40	mA
saturation voltage	I_1 = 20 mA	$V_{1\text{-}18sat}$	–	–	0.8	V
rejection voltage	$I_1 < 10\ \mu A$	$V_{1\text{-}18}$	23	–	–	V
DK circuit						
Switch-on threshold level	pin 2 high-Z	V_{15DKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{15DKon}}{V_{15DKoff}}$	3.1	3.6	4.1	dB
DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	$V_{16\text{-}18off}$	–	0.6	–	V
DK output (pin 2)						
allowable load current		I_2	–	–	1.5	mA
saturation voltage	I_2 = 1.5 mA	$V_{2\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_2 < 5\ \mu A$	$V_{2\text{-}18}$	18	–	–	V
BK and DK filter amplifiers						
Open loop gain	f = 100 Hz	G_o	84	–	–	dB
Current gain		G_i	120	–	–	dB
Input bias current		$\pm I_i$	–	–	50	nA
Output offset voltage	$R_{5\text{-}6} = R_{14\text{-}15}$ = 680 kΩ	$\pm V_{o5\text{-}8}$ $\pm V_{15\text{-}8}$	–	–	50	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BK and DK filter amplifiers (continued)						
Available output current		$\pm I_o$	1	–	–	mA
Output resistance		R_o	–	2	3.5	kΩ
Allowable load capacitance		C_L	–	–	50	pF
Internal reference voltage						
Output voltage (typ. value = 0.5 V_P)		$V_{8\text{-}18}$	4.0	4.25	4.5	V
Internal resistance of voltage source		R_8	–	–	5	Ω
Available output current		$-I_8$	2	–	–	mA
		$+I_8$	0.6	–	–	mA
Output short-circuit current (typ. value = V_P/1 kΩ)		$-I_{8sc}$	–	8	–	mA
Reference current source						
Reference voltage (typ. value = $V_{8\text{-}18}-V_{BE}$)		$V_{17\text{-}18}$	–	3.6	–	V
Internal biasing resistor		R_{i17}	–	5	–	kΩ
Allowable range of external reference resistor		$R_{17\text{-}18}$	180	–	270	kΩ

APPLICATION INFORMATION (Fig. 1)

parameter	symbol		application	unit
SK switch-on threshold level at m_{BK} = 60%	V_{iSKon}	typ.	1.8	mV
SK switch-on threshold level at V_{iSK} = 8 mV	m_{BKon}	typ.	32	%
SK switch hysteresis	$\frac{m_{BKon}}{m_{BKoff}}$	>	3.0	dB
		typ.	3.5	dB
		<	4.0	dB
SK switch-on delay (note 1)	t_{dSKon}	typ.	95	ms
		<	130	ms
SK switch-off delay (note 2)	t_{dSKoff}	>	380	ms
		typ.	500	ms
		<	620	ms
DK switch-on threshold level at m_{DK} = 30%	V_{iDKon}	typ.	1.5	mV
DK switch-on threshold level at V_{iDK} = 8 mV	m_{DKon}	typ.	13	%
DK switch hysteresis	$\frac{m_{DKon}}{m_{DKoff}}$	>	3.1	dB
		typ.	3.6	dB
		<	4.1	dB
DK switch-on delay (note 1)	t_{dDKon}	typ.	750	ms
		<	1000	ms
DK switch-off delay (note 2)	t_{dDKoff}	>	600	ms
		typ.	750	ms
		<	1000	ms

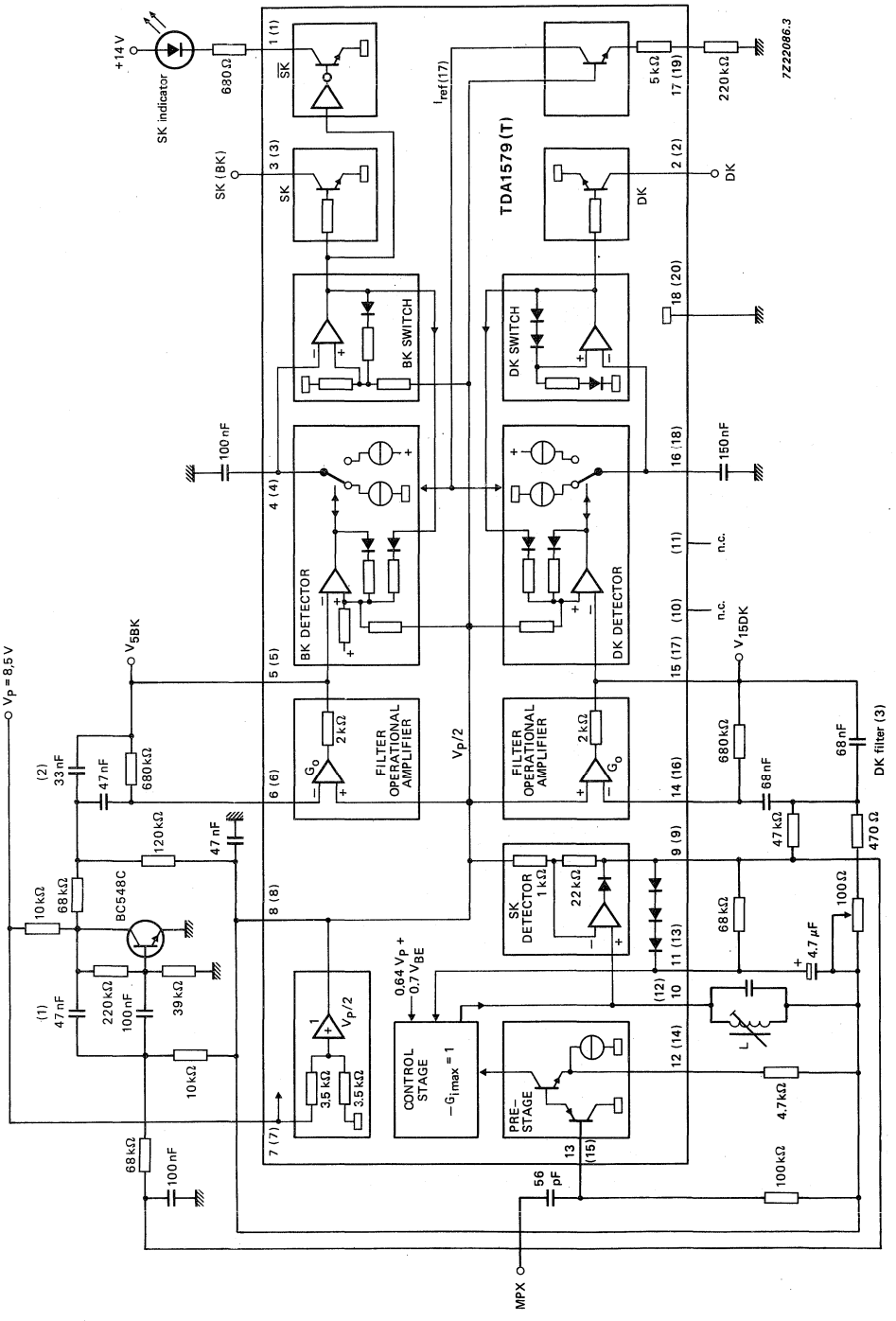
Notes

1. **Sequence for measuring switch-on delay times** (t_{don})
   a) Nominal BK or DK input signal at pin 13: $V_{i(p-p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 16 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 16) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{don} ends when the positive-going edge of the SK output arrives at pin 13 (DK at pin 2).
2. **Sequence for measuring switch-off delay times** (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

APPLICATION INFORMATION (continued)



L = 2.36 mH; Q_L = 70; C = 3.3 nF; f_o = 57 kHz.
Pin numbers in parentheses are for TDA1579T, other pin numbers are for TDA1579.

Fig. 1 Application diagram.

(1) f_o = 55 Hz; Q = 1.9
(2) f_o = 24 Hz; Q = 1.9
(3) f_o = 125 Hz

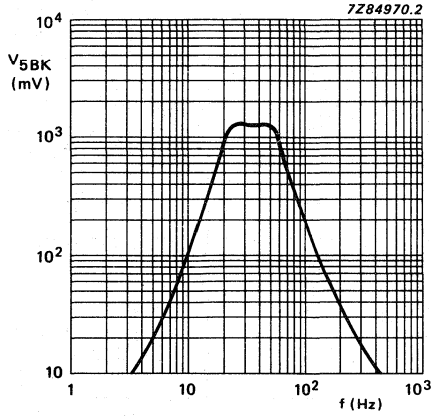


Fig. 2 BK signal voltage at pin 5 as a function of frequency.

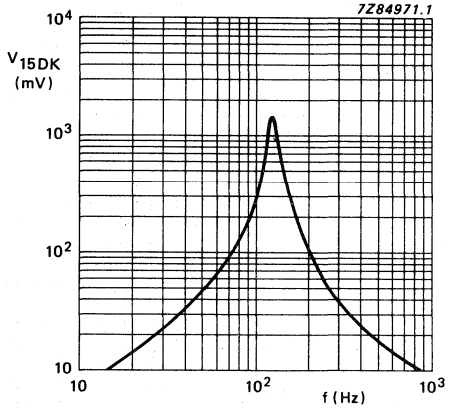


Fig. 3 DK signal voltage at pin 15 as a function of frequency: f_o = 125 Hz; Q ≈ 18.

APPLICATION INFORMATION (continued)

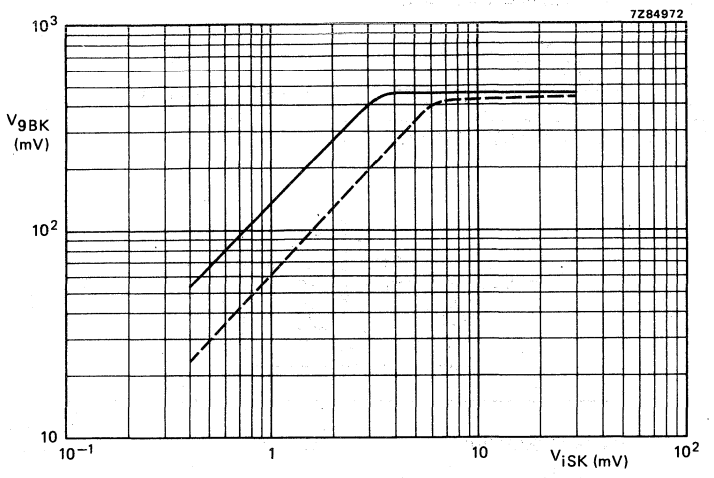


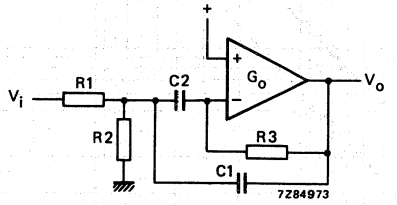
Fig. 4 Control characteristic of the SK amplifier at V_P = 8.5 V, m_{BK} = 60% and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p \frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	general equation	C1 = C2 = C	C1 = C2 = C R2 << R1
Resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$	$\frac{1}{C\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3}}$	$\frac{1}{C\sqrt{R2 \cdot R3}}$
Gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$
Quality $Q =$	$\sqrt{\frac{C1 \cdot C2}{C1 + C2}} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2} \cdot \frac{R3}{R2}$

Recommended components

C1, C2 and R1, R2, R3	metallized polycarbonate film (MKC) capacitors; ± 5% metal film (MR) resistors; ± 2%
or	
C1, C2 and R1, R2, R3	metallized polyester film (MKT) capacitors; ± 5% carbon film (CR) resistors; ± 2%

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

FEATURES

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- SK and BK control outputs

GENERAL DESCRIPTION

The TDA1581T decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the german 'Verkehrs Warnfunk' (VWF) traffic warning system.

QUICK REFERENCE DATA

Measured in Fig.3 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60 % for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30 % for DK signal

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		7.5	8.5	10	V
I_P	supply current		–	6	–	mA
V_{iSK}	nominal input voltage	f = 57 kHz	–	8	–	mV
Z_i	input impedance	f ≤ 57 kHz	100	–	–	kΩ
V_{iSK}	control level	-3 dB	–	2.4	–	mV
$V_{i(p-p)}$	input voltage peak-to-peak value		2	–	–	V
m_{BKon}	SK switch-on threshold level		–	42	–	%
Δm_{BK}	SK switch hysteresis		–	3.5	–	dB
t_{dSKon}	SK switch-on delay		–	150	–	ms
t_{dSKoff}	SK switch-off delay		–	750	–	ms
m_{DKon}	DK switch-on threshold level		–	13	–	%
Δm_{DK}	DK switch hysteresis		–	3.6	–	dB
t_{dDKon}	DK switch-on delay		–	750	–	ms
t_{dDKoff}	DK switch-off delay		–	750	–	ms
T_{amb}	operating ambient temperature range		-30	–	+80	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1581T	20	SO	plastic	SOT163A

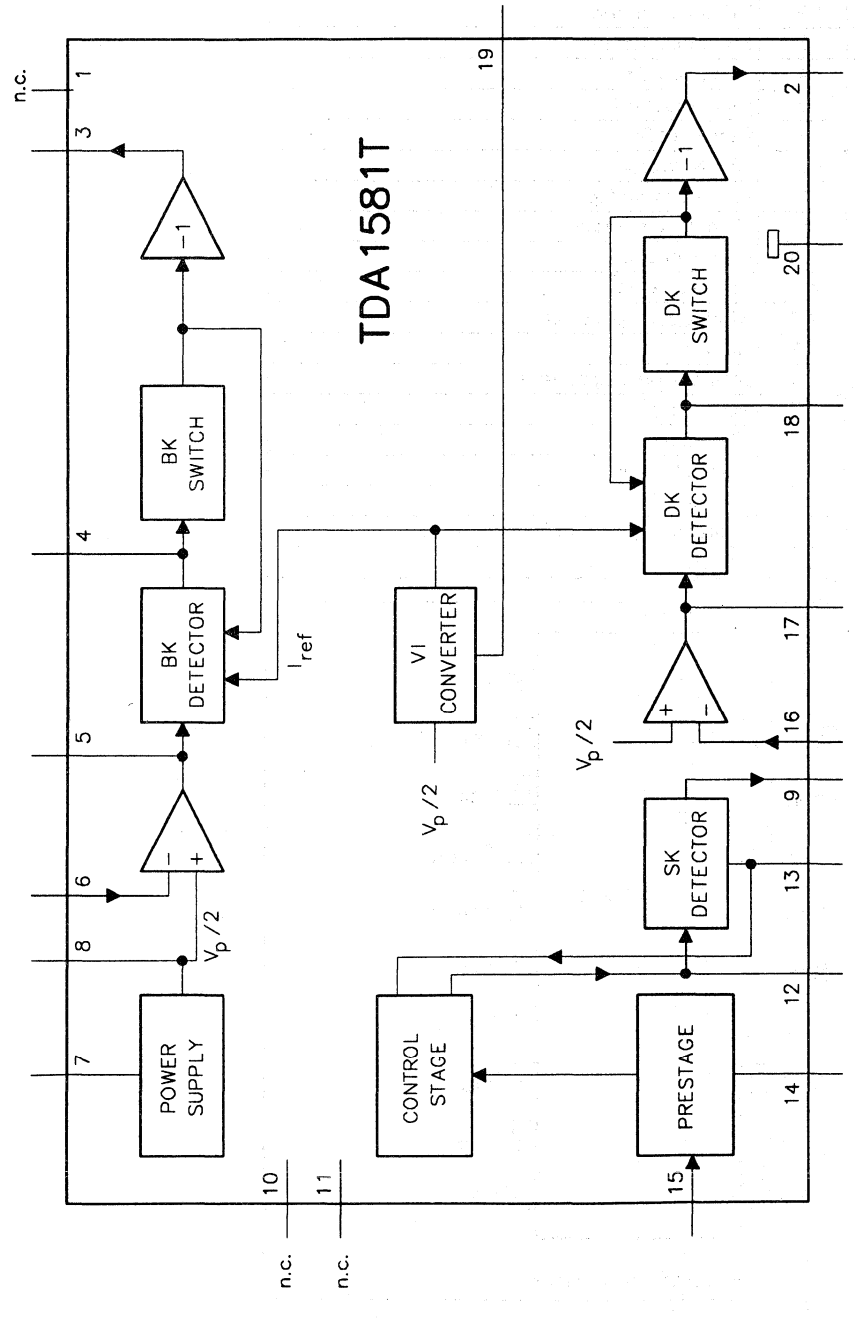


Fig.1 Block diagram.

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DK_{out}	2	DK output current
SK_{out}	3	SK output current
τ_{BK}	4	time delay BK
V_{5BK}	5	filter output BK
V_{6BK}	6	filter input BK
V_p	7	supply voltage
$V_p / 2$	8	half supply voltage
V_{9SK}	9	SK detector output
n.c.	10	not connected
n.c.	11	not connected
V_{12SK}	12	57 kHz band pass filter
V_{AGC}	13	AGC
I_{14}	14	prestage biasing current
V_{MPX}	15	MPX input
V_{16DK}	16	filter input DK
V_{17DK}	17	filter output DK
τ_{DK}	18	time delay DK
I_{19}	19	reference current for BK, DK detector
GND	20	ground

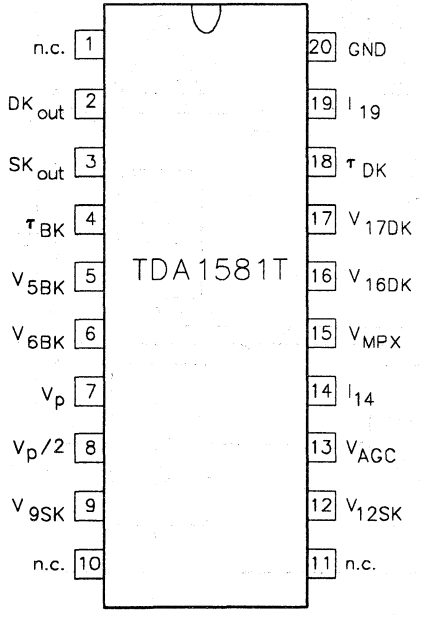


Fig.2 Pin configuration.

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P = V_{7-20}$	supply voltage	pin 7	–	–	15	V
$V_{2;3-20}$	switch output voltage	pins 2 or 3	-0.5	–	15	V
$I_{2;3}$	switch output current	pins 2 or 3	-10	–	5	mA
V_{15-20}	signal input voltage	pin 15	-0.5	–	V_p	V
I_{15}	signal input current	pin 15	–	–	-10	mA
P_{tot}	total power dissipation		–	–	800	mW
T_{stg}	storage temperature range		-55	–	+150	°C
T_{amb}	operating ambient temperature range		-30	–	+80	°C

CHARACTERISTICS

V_p = 8.5 V; T_{amb} = +25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60 % for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30 % for DK signal.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	pin 7	7.5	–	10	V
I_p	supply current	pin 7	–	6	15	mA
SK amplifier/decoder						
Z_i	input impedance	f ≤ 57 kHz	60	–	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)		2	–	–	V
V_{iSK}	input voltage at start of gain control	V_{o9BK} = -3 dB	–	2.4 *	–	mV
G_{v9-15}	voltage gain	V_{9BK} / V_{15SK}	–	44 *	–	dB
ΔG_{v9-15}	gain spread		–	–	±2	dB
ΔG_v	gain control range		40	–	–	dB
V_{o9BK}	controlled output voltage		–	440	–	mV
V_{o9DK}			–	220	–	mV
BK circuit						
V_{o5BKon}	switch-on threshold level	pin 3 high-Z	600	670	750	mV
$\frac{V_{o5BKon}}{V_{o5BKoff}}$	switch hysteresis		3	3.5	4	dB
$V_{4-20off}$	BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8-20}$)	pin 3 conducting	0.8	0.88	0.97	V
	SK output (pin 3)					
I_3	permitted load current		–	–	0.5	mA
$V_{3-20sat}$	saturation voltage	I_3 = 1.5 mA	–	–	0.35	V
V_{3-20}	rejection voltage	I_3 < 5 µA	18	–	–	V
DK circuit						
V_{17DKon}	switch-on threshold level	pin 2 high-Z	600	670	750	mV
$\frac{V_{17DKon}}{V_{17DKoff}}$	switch hysteresis		3.1	3.6	4.1	dB
$V_{18-20off}$	DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	–	0.6	–	V

* selectable by R_{14-8} or Z_{12-8}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DK output (pin 2)					
I_2	permitted load current		–	–	0.5	mA
$V_{2\text{-}20sat}$	saturation voltage	I_2 = 1.5 mA	–	–	0.35	V
$V_{2\text{-}20}$	rejection voltage	$I_2 < 5$ µA	18	–	–	V
BK and DK filter amplifiers						
G_o	open loop gain	f = 100 Hz	84	–	–	dB
G_i	current gain		120	–	–	dB
I_i	input bias current		–	–	±50	nA
$V_{o5\text{-}8}$	output offset voltage	$R_{5\text{-}6} = R_{16\text{-}17}$ = 680 kΩ	–	–	±50	mV
$V_{17\text{-}8}$						
I_o	available output current		±1	–	–	mA
R_o	output resistance		–	2	3.5	kΩ
C_L	permitted load capacitance		–	–	50	pF
Internal reference voltage						
$V_{8\text{-}20}$	output voltage (typ. value = $0.5V_p$)		4.0	4.25	4.5	V
R_8	internal resistance of voltage source		–	–	5	Ω
$I_{8\text{-}20}$	available output current		-2	–	–	mA
$I_{20\text{-}8}$			0.6	–	–	mA
I_{8sc}	output short-circuit current (typ. value = V_p / 1 kΩ)		–	-8	–	mA
Reference current source						
$V_{19\text{-}20}$	reference voltage (typ. value = $V_{8\text{-}20} - V_{BE}$)		–	3.6	–	V
R_{i19}	internal biasing resistor		–	5	–	kΩ
$R_{19\text{-}20}$	permitted range of external reference resistor		180	–	270	kΩ

APPLICATION INFORMATION (see Fig.3)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{iSKon}	SK switch-on threshold level	m_{BK} = 60 %	–	1.8	–	mV
m_{BKon}	SK switch-on threshold level	V_{iSK} = 8 mV	–	32	–	%
$\frac{m_{BKon}}{m_{BKoff}}$	SK switch hysteresis		3.0	3.5	4.0	dB
t_{dSKon}	SK switch-on delay	note 1	–	95	200	ms
t_{dSKoff}	SK switch-off delay	note 2	380	500	700	ms
V_{iDKon}	DK switch-on threshold level	m_{DK} = 30 %	–	1.5	–	mV
m_{DKon}	DK switch-on threshold level	V_{iDK} = 8 mV	–	13	–	%
$\frac{m_{DKon}}{m_{DKoff}}$	DK switch hysteresis		3.1	3.6	4.1	dB
t_{dDKon}	DK switch-on delay	note 1	–	750	1000	ms
t_{dDKoff}	DK switch-off delay	note 2	600	750	1000	ms

Notes to the application information

1. Sequence for measuring switch-on delay times (t_{don})
   a) Nominal BK or DK input signal at pin 15: $V_{i(p-p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 18 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 18) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 17) crosses zero.
   t_{don} ends when the positive-going edge of the SK output arrives at pin 15 (DK at pin 2).
2. Sequence for measuring switch-off delay times (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 17) crosses zero.
   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

Decoder for traffic warning (VWF) radio transmissions

TDA1581T

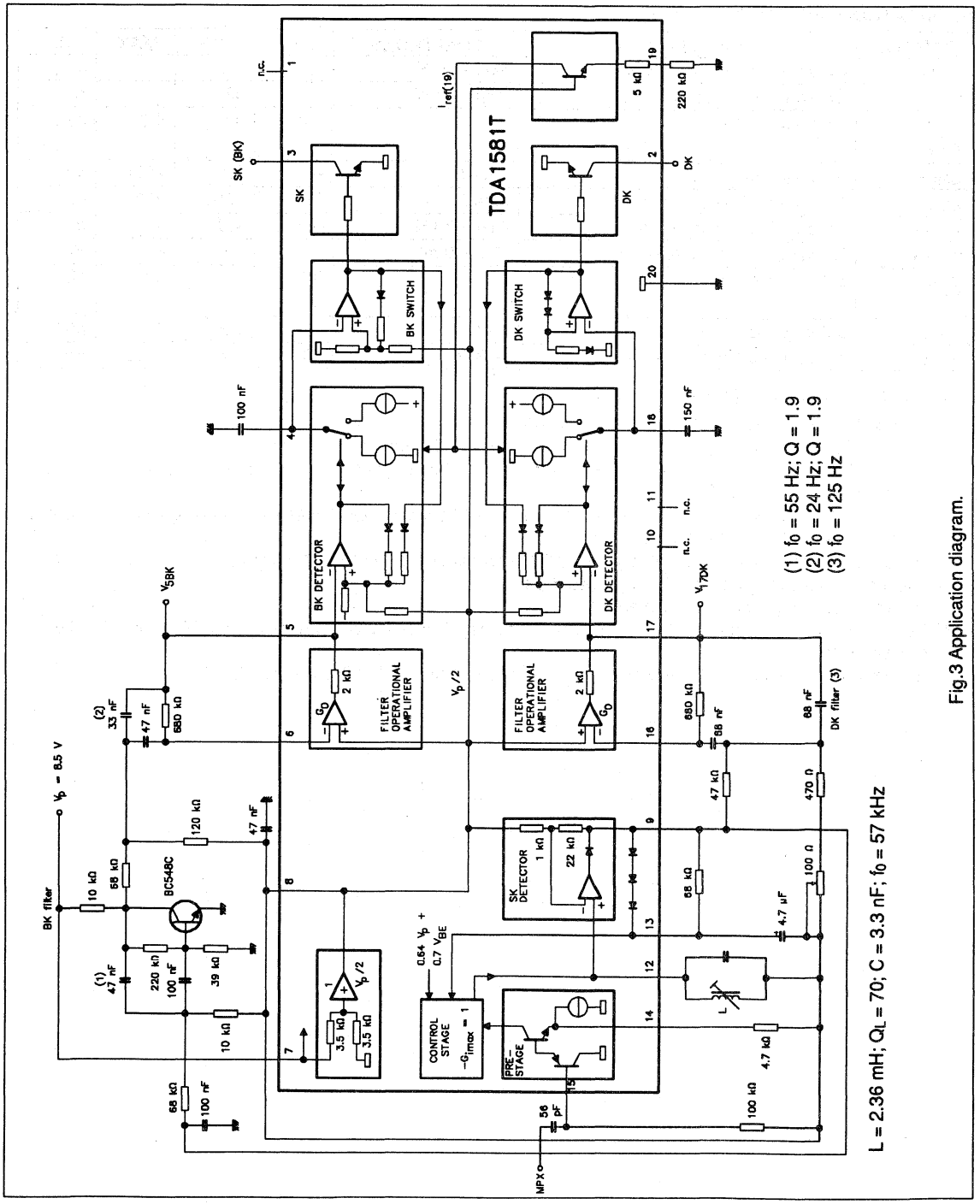


Fig.3 Application diagram.

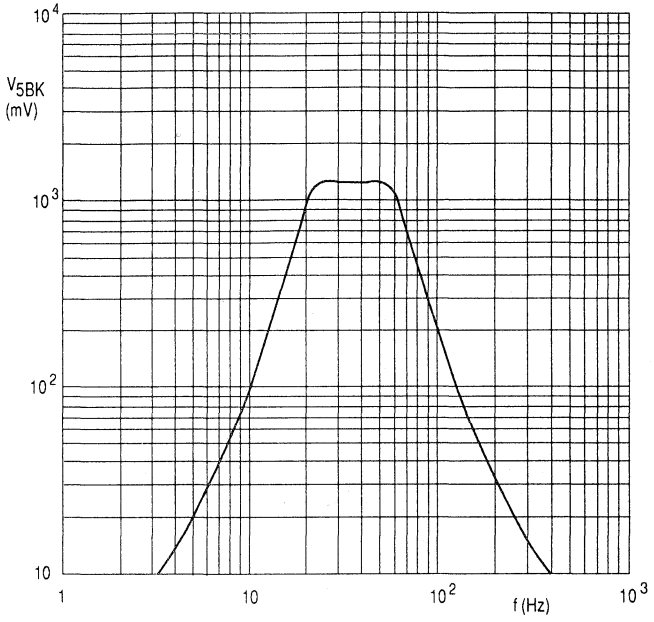


Fig.4 BK signal voltage at pin 5 as a function of frequency.

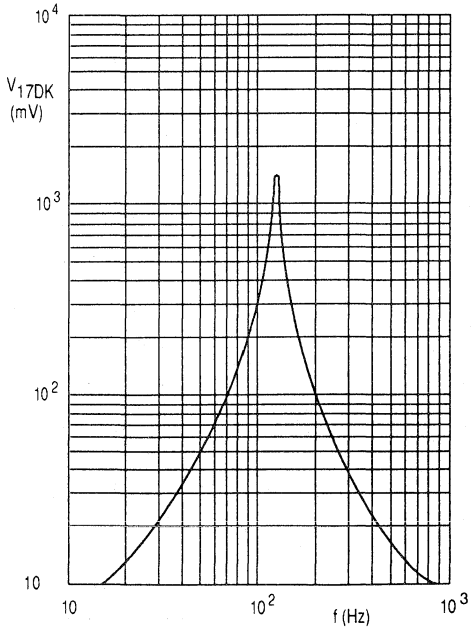


Fig.5 DK signal voltage at pin 17 as a function of frequency: f_0 = 125 Hz; Q ≈ 18.

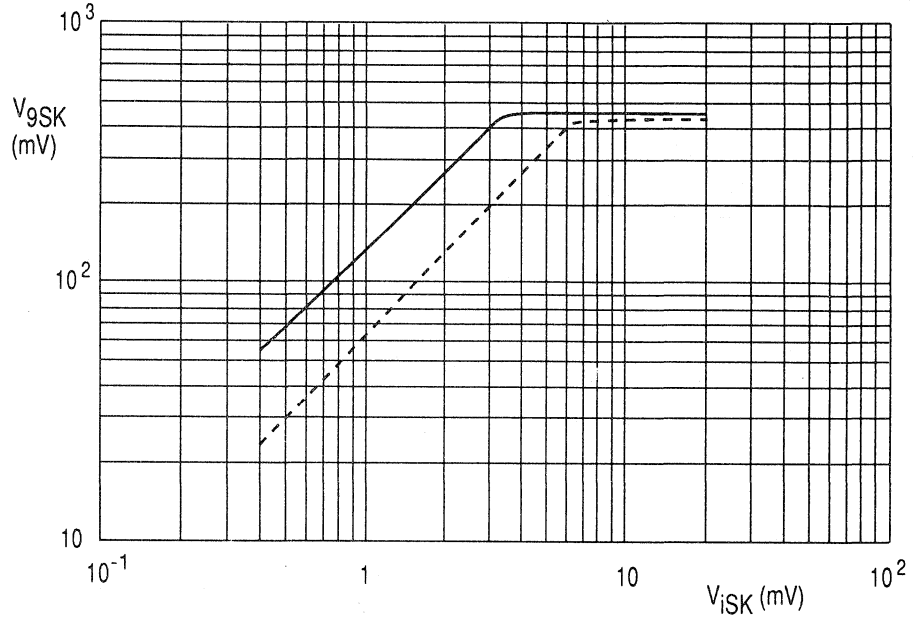


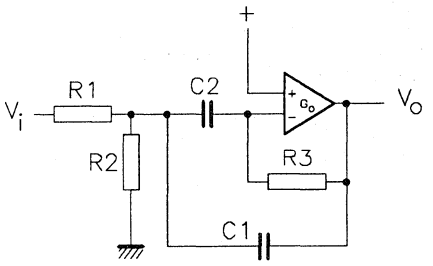
Fig.6 Control characteristic of the SK amplifier at V_p = 8.5 V, m_{BK} = 60 % and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \times Q^2$

$$G_v = -\frac{\frac{p}{R1 \times C1}}{p^2 + p \times \frac{C1 + C2}{R3 \times C1 \times C2} + \frac{R1 + R2}{R1 \times R2 \times R3 \times C1 \times C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	GENERAL EQUATION	C1 = C2 = C	C1 = C2 = C R2 << R1
resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \times R2}{R1 + R2} \times R3 \times C1 \times C2}}$	$\frac{1}{C\sqrt{\frac{R1 \times R2}{R1 + R2} \times R3}}$	$\frac{1}{C\sqrt{R2 \times R3}}$
gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \times \frac{R3}{R1}$	$\frac{1}{2} \times \frac{R3}{R1}$	$\frac{1}{2} \times \frac{R3}{R1}$
quality $Q =$	$\sqrt{\frac{C1 \times C2}{C1 + C2}} \times \sqrt{\frac{R3\,(R1 + R2)}{R1 \times R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \times R2}}$	$\frac{1}{2} \times \frac{R3}{R2}$

Recommended components

C1, C2	metallized polycarbonate film (MKC) capacitors; ±5 %
and	
R1, R2, R3	metal film (MR) resistors; ±2 %
or	
C1, C2	metallized polyester film (MKT) capacitors; ±5 %
and	
R1, R2, R3	carbon film (CR) resistors; ±2 %

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1992

TDA1591/T
PLL stereo decoder and noise blanker

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz).
- Mono/stereo switching, dependent on pilot signal.
- Analog control of mono/stereo change over (stereo blend, SNC).
- Adjacent channel noise suppression (114 kHz).
- Pilot canceller
- Analog control of de-emphasis (High Cut Control input, HCC).
- Applicable as source selector for AM/FM/cassette switching
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking.
- Noise blanking at MPX-demodulator outputs
- Internal voltage stabilization

GENERAL DESCRIPTION

The TDA1591/T is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications.
The device operates in a power supply range of 7.5 to 12 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	7.5	10	12	V
I_P	supply current	–	12	–	mA
V_o	audio output signal (RMS value)	–	900	–	mV
THD	total harmonic distortion	–	0.1	0.3	%
S/N	signal-to-noise ratio	–	76	–	dB
α	channel separation	–	40	–	dB
V_{trigg}	interference voltage trigger level	–	10	–	mV

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1591	20	DIL	plastic	SOT146
TDA1591T	20	mini-pack	plastic	SOT163A

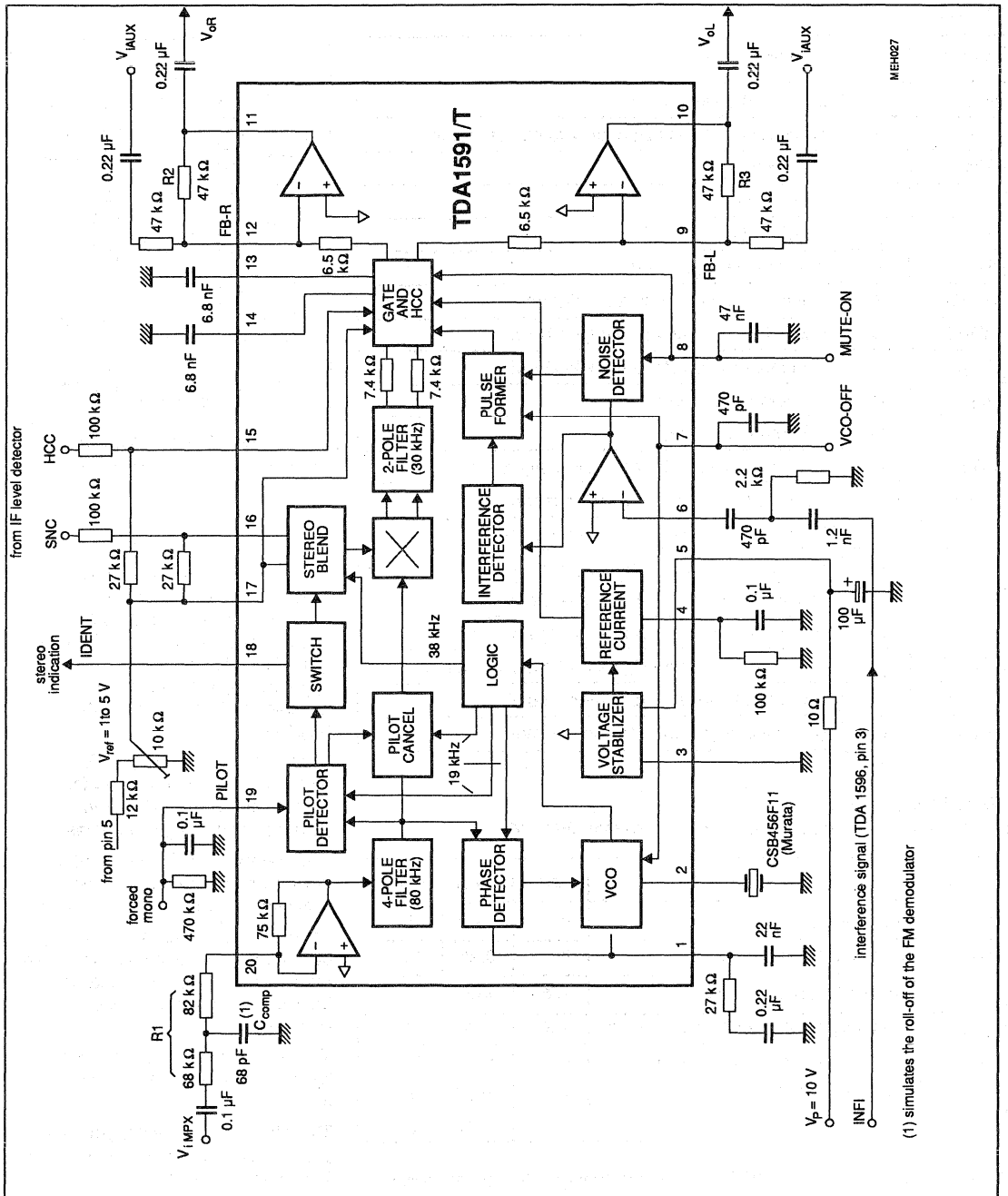


Fig.1 Block diagram, test and application circuit.

PLL stereo decoder and noise blanker

TDA1591/T

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{ref}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant, VCO off
NDET	8	noise detector time constant, mute on
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	High Cut Control input for de-emphasis control
SNC	16	stereo blend input (Stereo Noise Controller)
V_{ref}	17	externally-applied reference voltage of 1 to 5 V
IDENT	18	identification output (High = pilot existing, stereo)
PILOT	19	pilot detector level (forced mono input)
V_{iMPX}	20	MPX input signal from IF demodulator

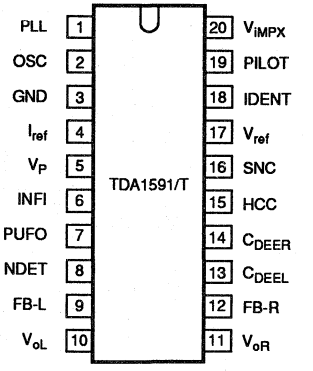


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	0	13.2	V
P_{tot}	total power dissipation	0	0.25	W
T_{stg}	storage temperatur range	−55	+150	°C
T_{amb}	operating ambient temperatur range	−40	+85	°C
V_{ESD}	electrostatic handling* for all pins	−	±600	V
	except pin 1, 16	−	±400	V
	pin 5	−	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

FUNCTIONAL DESCRIPTION

By changing the value of the input resistor R1 the MPX input can be adapted to the level of the FM demodulator output (Fig.3). The total gain of the stereo decoder is applicable by variation of the feedback resistors R2 and R3 (Fig.1 and 4).

In mute and VCO-OFF position the output amplifier can be used for cassette playback, AM-stereo purpose or other signal sources.

The Stereo Noise Controller SNC provides a smooth mono to stereo take over (Fig.5).

For High Cut Control (HCC), dependent on an analog input signal, the de-emphasis time constant can be changed to higher values (Fig.7 and 8).

The noise blanking facility is achieved by gating the stereo decoder output signal.

The interference detector generates a gating pulse preferable forced by the level detector voltage of the IF part.

CHARACTERISTICS

V_P = 10 V, T_{amb} = +25 °C, input signal $V_{i\ MPX\ (p\text{-}p)}$ = 1.7 V; m = 100% (deviation Δf = ±75 kHz, f_{mod} = 1 kHz), de-emphasis 50 µs and serial resistor at input R1 = 150 kΩ; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)		7.5	10	12	V
I_P	supply current		–	12	–	mA
Stereo decoder						
V_i	MPX input signal on pin 20 (peak-to-peak value)		–	1.7	–	V
ΔV_i	overdrive margin of MPX input signal	THD = 1%	3	–	–	dB
V_o	AF mono output signal at pins 10 and 11 (RMS value)	without pilot	–	900	–	mV
ΔV_o	overdrive margin of output signal	THD = 1%	3	–	–	dB
$V_{10\text{-}11}/V_o$	difference of output voltage levels		–	–	1	dB
$V_{10,11}$	DC output voltage (pins 10 and 11)		3.3	3.8	4.3	V
$R_{10,11}$	output resistance		–	130	–	Ω
α	channel separation, see Fig.6	pin 16 open-circuit	–	40	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 to 16000 Hz	–	76	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	–	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	–	50	–	dB
α_{57}		f = 57 kHz	–	46	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
α_2	intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz, note 1	–	60	–	dB
α_3		f_{mod} = 13 kHz	–	58	–	dB
$\alpha_{57\ VF}$	traffic radio (VWF)	f = 57 kHz, note 2	–	70	–	dB
α_{67}	SCA (subsidiary communications authorization)	f = 67 kHz, note 3	70	–	–	dB
α_{114}	ACI (adjacent channel interference)	f = 114 kHz, note 4	–	80	–	dB
α_{190}		f = 190 kHz	–	70	–	dB
RR	ripple rejection with ripple on V_P	f = 100 Hz $V_{ripple\ (rms)}$ = 100 mV	–	35	–	dB
VCO (pin 2)						
f_{osc}	oscillator frequency (ceramic resonator)		–	456	–	kHz
f_{osc}	frequency range of free running oscillator		452	–	460	kHz
$\Delta f/f$	capture and holding range		–	1	–	%
V_7	VCO-OFF voltage (pin 7)		0	–	0.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mono/stereo control (pins 16, 17 and 19)						
$V_{i\ pil}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)					
	for stereo on		–	24	30	mV
	for stereo off		8	20	–	mV
H	hysteresis of pilot threshold voltage		–	2	–	dB
V_{19}	switching voltage for external mono control (pin 19)		0	–	1	V
V_{ref}	reference input voltage range (pin 17)		1	–	5	V
V_{16-17}	control voltage for channel separation due to pin 17 (V_{ref}), see Fig.5	α = 6 dB	–	–85	–	mV
		α = 26 dB	–	–32	–	mV
	pilot indicator logic level output					
V_{18}	LOW voltage (pin 18)	I_{18} = –500 µA	–	250	400	mV
I_{18}	HIGH current	V_{18} = 10 V	–	–	1	µA
Muting (pin 8)						
V_8	mute attenuation (pin 8)	V_8 < 0.4 V	–	80	–	dB
		V_8 > 4 V	–	–	0.2	dB
$V_{10, 11}$	DC offset voltage	after muting	–	–	±400	mV
High Cut Control HCC (pin 15)						
t_{deem}	control range of de-emphasis	(Fig.7 and 8)				
	for European standard	C_{deem} = 6.8 nF	50	–	150	µs
	for US standard	C_{deem} = 10 nF	75	–	225	µs
V_{15-17}	control voltage (pin 15 due to pin 17) in both standards	lower value t_{deem}	–	0	–	mV
		upper value t_{deem}	–	–300	–	mV
Noise interference detector						
V_{trigg}	trigger threshold (pin 6)	f_{int} = 120 kHz				
		$V_{8\ (DC)}$ = 7.7 V	–	10	–	mV
		$V_{8\ (DC)}$ = 6.7 V	–	100	–	mV
ΔV_8	voltage offset as a function of V_{trigg}	$V_{6\ trigg}$ = 10 mV	–	200	–	mV
		$V_{6\ trigg}$ = 100 mV	–	2.3	–	V
t_{suppr}	AF suppression time, pulse width		–	40	–	µs
$I_{13,14}$	input offset current (pins 13 and 14)	during AF suppression time	–	20	–	nA
V_{pulse}	trigger sensitivity (pin 6)	τ_{pulse} = 10 µs	–	10	–	mV

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})} \quad ; \quad f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz})} \quad ; \quad f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_{mod}= 10 kHz or 13 kHz; 9% pilot signal

2. Traffic radio (V.F.) suppression

$$\alpha_{57}\ (VF) = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 1\ \text{kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_{mod}= 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 kHz; f_{mod}= 23 Hz AM, m = 0.6).

3. SCA (Subsidiary Communication Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 9\ \text{kHz})} \quad ; \quad f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_{mod}= 1 kHz; 9% pilot signal;
10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})} \quad ; \quad f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})} \quad ; \quad f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

measured with 90% mono signal; f_{mod}= 1 kHz; 9% pilot signal; 1% spurious signal
(f_s = 110 kHz or 186 kHz, unmodulated).

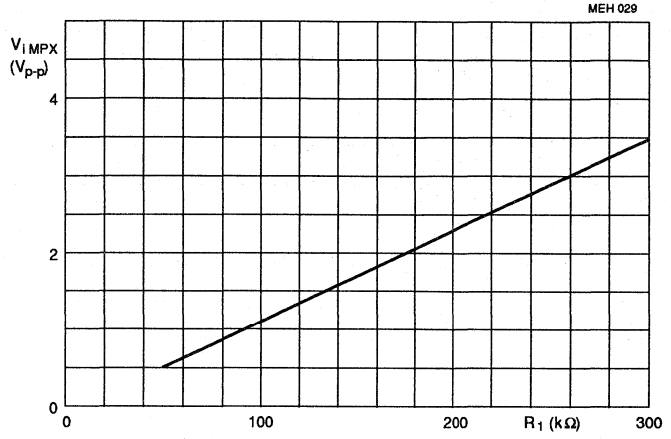


Fig.3 Input signal as a function of serial input resistor R1.

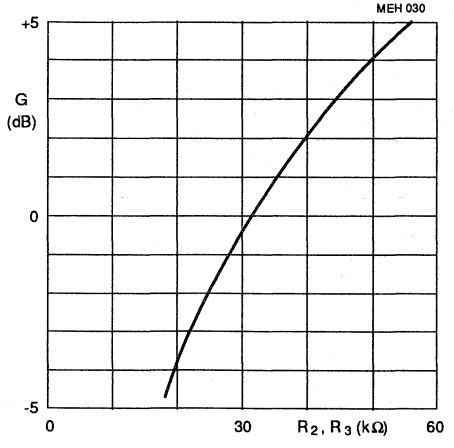


Fig.4 Over all signal gain as a function of feedback resistors R2 and R3 (R1 = 150 kΩ).

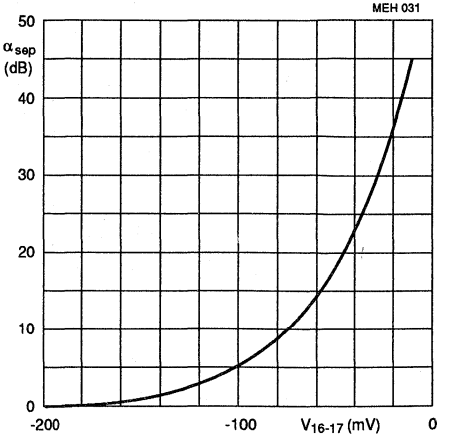


Fig.5 Stereo blend characteristic (SNC).

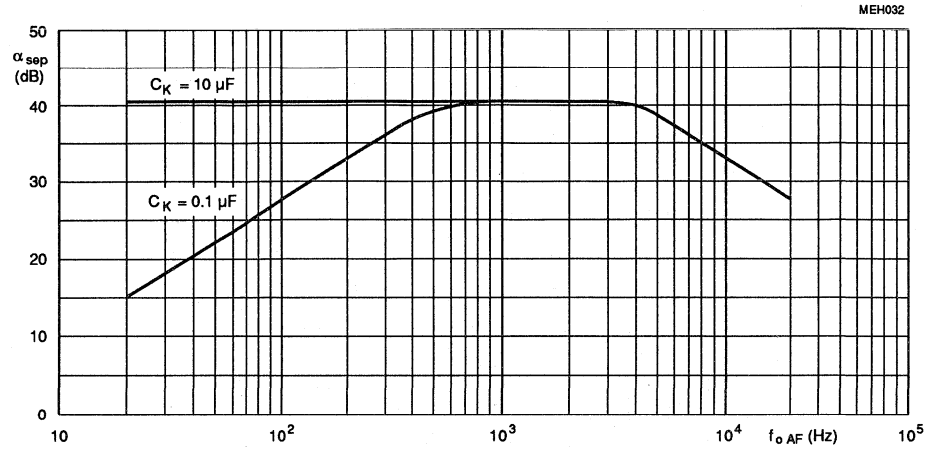


Fig.6 Channel separation as a function of audio frequency.

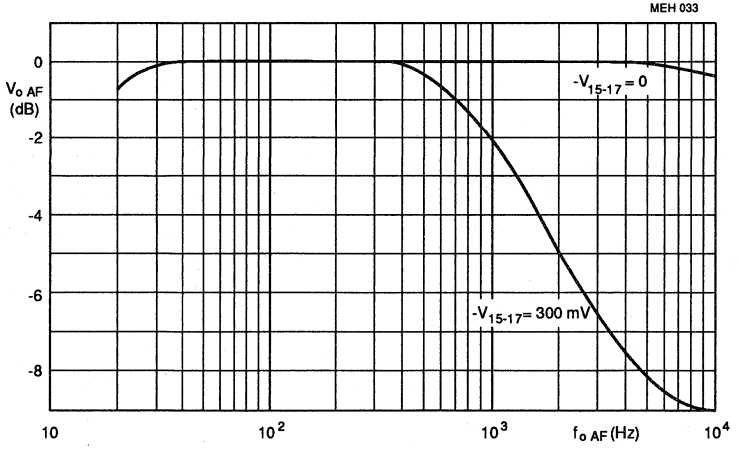


Fig.7 High Cut Control (HCC) as a function of audio frequency.

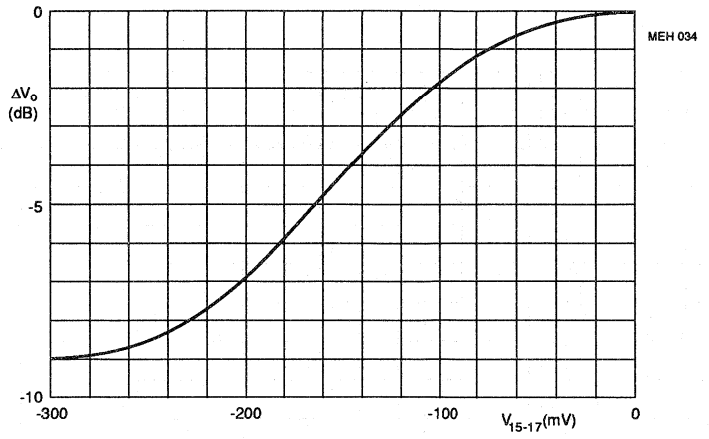


Fig.8 High Cut Control (HCC) with f_{mod} = 10 kHz.

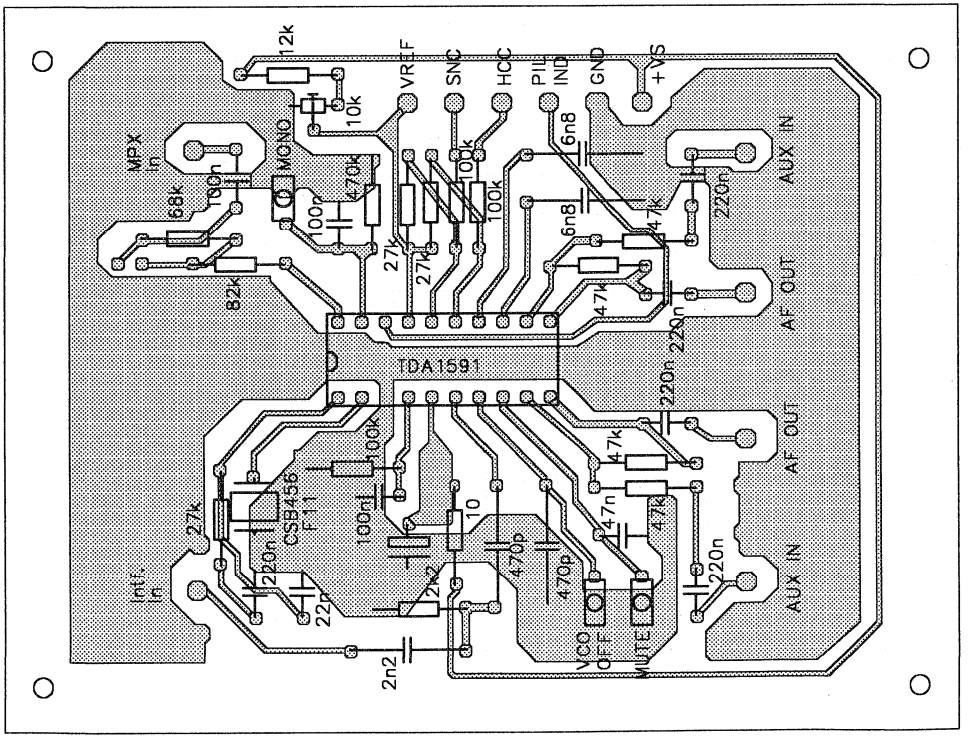


Fig.9 TDA1591 testboard (component side).

Data sheet	
status	Objective specification
date of issue	March 1991

TDA1595T

FM front-end for car radios (FM tuner and FM-IF amplifier)

FEATURES

- Radio frequency range of 76 to 90 MHz (Japan) or 87.5 to 108 MHz (Europe, USA)
- Integrated pre-amplifier
- Internal wideband AGC controlling the pre-amplifier
- Tuning by varicap diodes
- Current output for driving an external PIN diode
- Buffered oscillator output
- Imposed application diagram fulfils Cenelec requirement EN55020

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 11)	7	8.5	10	V
I_P	supply current	-	28	-	mA
NF	pre-amplifier noise figure	-	5	-	dB
	mixer noise figure	-	8	-	dB
	IF amplifier noise figure	-	8	-	dB
G_v	IF gain	-	36	-	dB
Z_o	IF output impedance	-	330	-	Ω
T_{amb}	operating ambient temperature	–40	-	+85	°C

GENERAL DESCRIPTION

The TDA1595T is a monolithic integrated FM tuner circuit for use especially in car radios. The circuit provides the RF and the IF functions of a radio set and comprises an automatic gain controlled pre-amplifier, oscillator, mixer, 36 dB IF amplifier and an oscillator buffer amplifier. The IF selectivity is achieved by ceramic filters.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1595T	16	mini-pack	plastic	SOT109

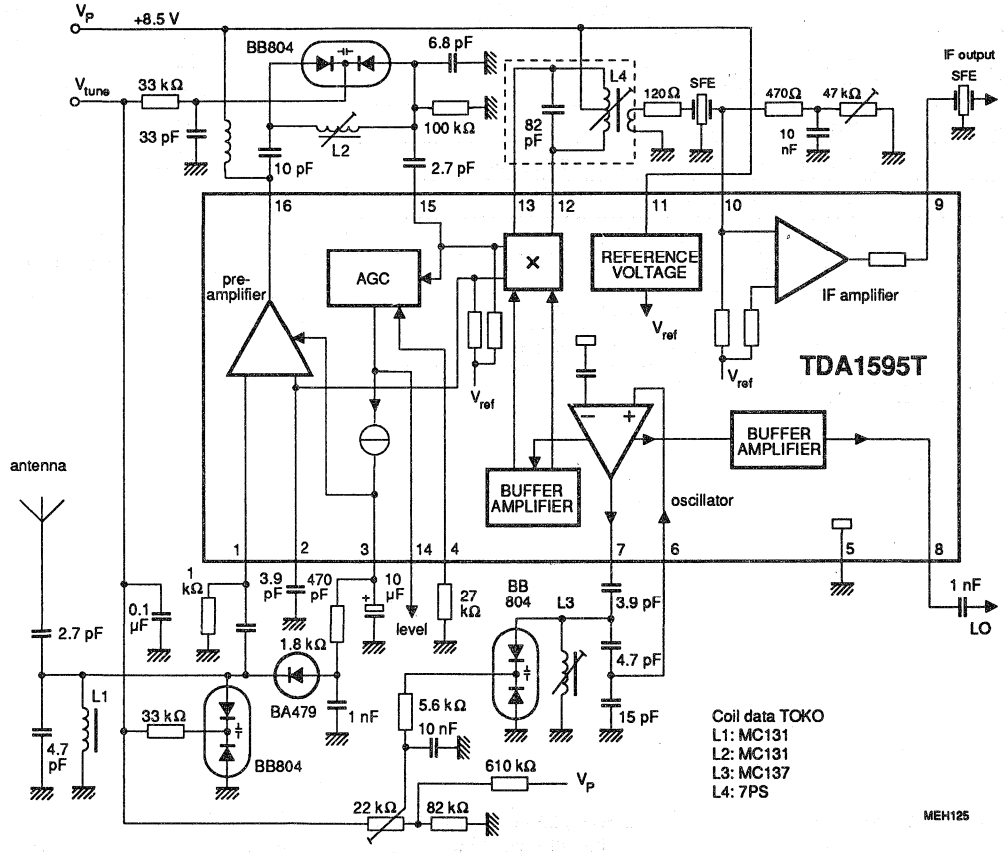


Fig.1 Block diagram, test and application circuit with internal RF pre-amplifier.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i1\ RF}$	1	radio frequency input 1
$V_{i2\ RF}$	2	radio frequency input 2, blocking capacitor
AGC	3	AGC voltage for pre-amplifier
REF	4	external reference voltage for AGC stage
GND	5	ground (0 V)
OSCI	6	oscillator input
OSCO	7	oscillator output
LO	8	buffered oscillator signal (local oscillator)
$V_{o\ IF}$	9	main IF output signal
$V_{i\ IF}$	10	IF input signal from bandfilter
V_P	11	+8.5 V supply voltage
MIX1	12	mixer output signal to resonant circuit
MIX2	13	mixer output signal to resonant circuit
LEVEL	14	RF signal level output
$V_{i\ mix}$	15	mixer input signal
$V_{o\ RF}$	16	RF pre-amplifier output

PIN CONFIGURATION

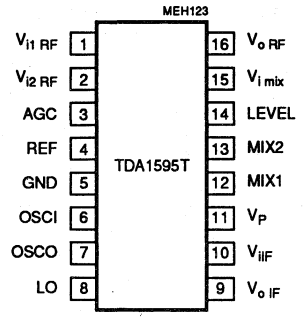


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Pre-amplifier and mixer

The pre-amplifier is a common base input stage to obtain large signal handling and decoupling between input and output signals (Fig.1). The mixer stage is a double-balanced multiplier with a common emitter input. This achieves a high-ohmic input resistances.

Automatic gain control (AGC)

AGC comprises a radio frequency detector, dependent on mixer input signal level; and a control amplifier to control the internal RF pre-amplifier. This output is fed to pin 3 to attenuate the RF input signal by means of an external PIN diode.

Oscillator

The oscillator amplifier has differential inputs to reduce second harmonics. A built-in buffer amplifier feeds out the local oscillator frequency (LO) to drive a synthesizer. The output impedance is low-ohmic.

IF amplifier stages

The IF signal is fed through a tuned resonant circuit and a ceramic filter. It is fed to pin 10, one of the two differential inputs of a linear, 2-stage wideband IF amplifier. The amplified signal is output on pin 9, this output is suitable for driving a ceramic filter.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 11)	0	10.5	V
$V_{12, 13}$	voltage on pins 12 and 13	4	16	V
P_{tot}	total power dissipation	-	500	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
V_{ESD}	electrostatic handling* for all pins	-	±1500	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	-	115	K/W

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; measurements taken in Fig.1 with f_o = 98 MHz (EMF1) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 11)		7	8.5	10	V
I_P	supply current		-	28	-	mA
RF pre-amplifier		EMF1 = 98 MHz				
$V_{1, 2}$	input bias voltage		-	2	-	V
$Z_{1, 2}$	input impedance		-	13	-	Ω
V_{16}	DC output voltage		-	-	V_P	V
I_{16}	DC output current		-	2	-	mA
C_{16}	output capacitance		-	t.b.f.	-	pF
G_P	power gain		-	10	-	dB
NF	noise figure		-	5	-	dB
IP3	3rd order intercept point		-	5	-	dBm

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mixer		EMF1 = 98 MHz				
V_{15}	input bias voltage		-	2.8	-	V
R_{15}	input resistance		-	3	-	kΩ
C_{15}	input capacitance		-	t.b.f.	-	pF
$V_{12, 13}$	DC output voltage		-	-	V_P	V
I_{12+13}	mixer supply current		-	7	-	mA
C_{12-13}	output capacitance		-	t.b.f.	-	pF
G_P	conversion power gain		-	t.b.f.	-	dB
IP3	3rd order intercept point		-	t.b.f.	-	dBm
NF	noise figure		-	8	-	dB
Oscillator		f_{osc} = 108.7 MHz				
V_6	DC input voltage		-	1.0	-	V
V_7	DC output voltage		-	2.8	-	V
Δf	residual FM at pin 6	f = 300 to 15000 Hz; de-emphasis 50 µs	-	5	-	Hz
Oscillator buffered output (pin 8)						
V_o	output signal (RMS value)	R_L = 500 Ω; C_L = 2 pF	75	-	-	mV
V_8	DC output voltage		-	7.6	-	V
R_8	DC output resistor		-	900	-	Ω
THD	total harmonic distortion		-	t.b.f.	-	dBC
f_S	spurious frequencies	EMF1 = 2 V; R_S = 50Ω f_{osc} = 108.7 MHz	-	t.b.f.	-	dBC
Automatic gain control (AGC)		f_i = 98 MHz				
V_4	AGC reference input voltage		-	1.0	-	V
I_4	input current		-	37	-	µA
V_3	AGC output swing (DC) to pin diode		0	-	5.7	V
I_3	output current	V_{15} = 60 mV (RMS value); f = 98 MHz	3		-	mA
V_{14}	RF level output voltage	V_{15} = 60 mV (RMS value); f = 98 MHz	-	1.4	-	V
R_{14}	DC output resistance		-	14	-	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear IF amplifier		IF = 10.7 MHz				
V_{10}	input bias voltage		-	1.8	-	V
Z_{10}	input impedance		-	3	-	kΩ
C_{10}	input capacitance		-	t.b.f.	-	pF
V_o	output signal (RMS value, pin 9)	−1 dB compression	-	600	-	mV
V_9	DC output voltage		-	5.5	-	V
Z_9	output impedance		-	330	-	Ω
C_9	output capacitance		-	t.b.f.	-	pF
G_v	IF voltage gain (20 log (V_9 / V_{10}))		-	36	-	dB
ΔG_v	IF voltage gain deviation	T_{amb} = −40 to +85 °C	-	0	-	dB
NF	noise figure	R_S = 300 Ω	-	8	-	dB

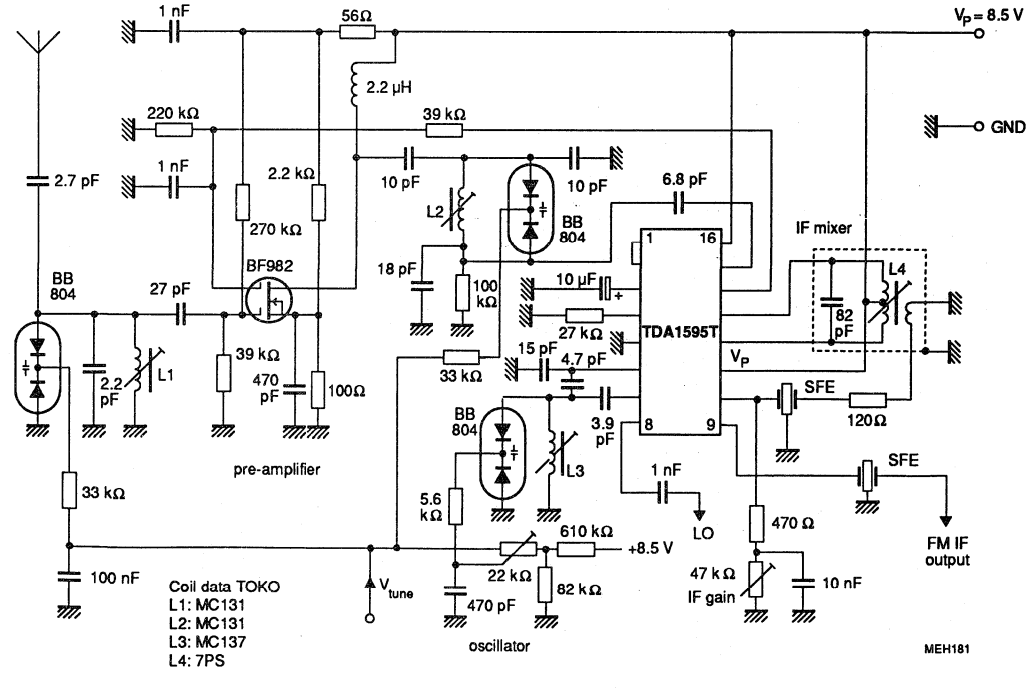


Fig.3 Application circuit with external RF pre-amplifier.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

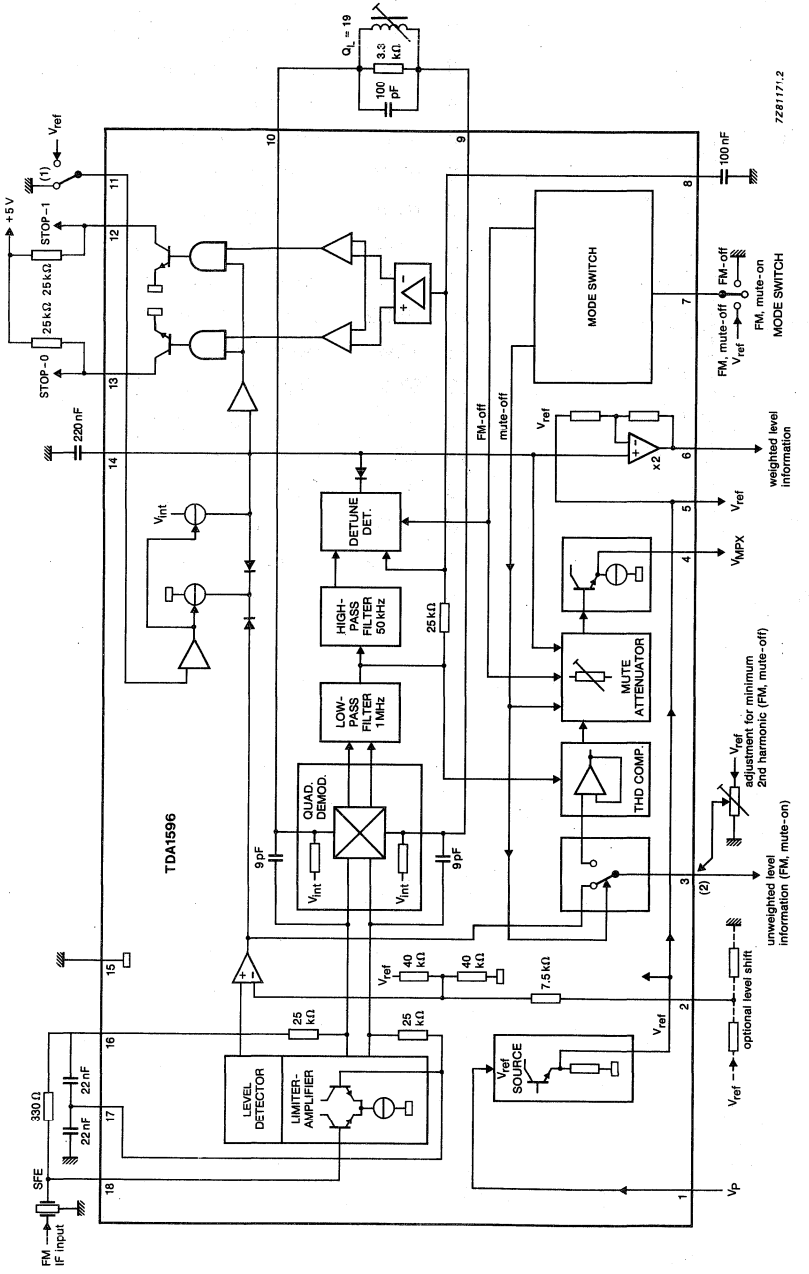
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{18(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{18(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	–40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596T

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

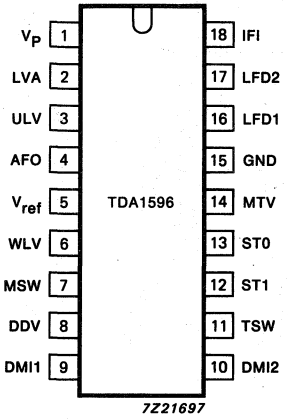


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	DMI1	demodulator input 1
10	DMI2	demodulator input 2
11	TSW	tau switch
12	ST1	stop pulse output 1
13	ST0	stop pulse output 0
14	MTV	mute voltage
15	GND	ground
16	LFD1	IF limiter feedback 1
17	LFD2	IF limiter feedback 2
18	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 9 and 10 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 14 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 14. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 13 and 12 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 12 and 13 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-15}$	−0.3	+ 16	V
Reference voltage range (pin 5)	V_{5-15}	−0.3	+ 10	V
Level adjustment range (pin 2)	V_{2-15}	−0.3	+ 10	V
Mode switch voltage range (pin 7)	V_{7-15}	−0.3	+ 16	V
Control input voltage range (pin 11)	V_{11-15}	−0.3	+ 6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-15}	−0.3	+ 16	V
Tuning-stop output voltage range				
STOP-0 (pin 13)	V_{13-15}	−0.3	+ 16	V
STOP-1 (pin 12)	V_{12-15}	−0.3	+ 16	V
Tuning-stop output current				
STOP-0 (pin 13)	I_{13}	−	2	mA
STOP-1 (pin 12)	I_{12}	−	2	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+ 2000	V
pin 5	V_{es}	−2000	+ 900	V
pin 6	V_{es}	−2000	+ 1600	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-15} = 8.5$ V; $V_I = V_{18(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 9, 10 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 15); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{9-10}	25	40	55	kΩ
	C_{9-10}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{9, 10(p-p)} \leqslant 100\ \mu V$; $V_{18(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-15}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 14)					
at $V_{18(rms)} \leqslant 5\ \mu V$	V_{14}	–	2.0	–	V
at $V_{18(rms)} = 1$ mV	V_{14}	–	3.45	–	V
Output impedance (pin 14)	R_{14-15}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-15}	15	–	–	kΩ
Internal muting (Fig. 4)					
Internal attenuation of signals ± 22.5 kHz ≤ detuning ≤ ± 80 kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{14} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{14} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{14} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 14)					
Pin 11 connected to ground *					
charge current	$+I_{14}$	–	8	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Pin 11 connected to V_{ref}					
charge current	$+I_{14}$	–	100	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 18) (Fig. 5):					
$V_{18(rms)} \leqslant 5\ \mu V$; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{18(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range $V_{18(rms)} \geqslant 50\ \mu V$ to $V_{18(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{18}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 6) at input voltage $V_{18(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning = for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ± 200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{18(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 7)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{18(rms)} \leqslant 5\ \mu V$	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{18(rms)} \leqslant 5\ \mu V$	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 8 and 9)					
Stop-0: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{13} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{13} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{12} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{12} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 18)					
input voltage (RMS value) for $V_{12} = V_{13} \geqslant 3.5$ V	$V_{18(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{12} = V_{13} \leqslant 0.3$ V	$V_{18(rms)}$	–	–	50	μV
Output voltage when $I_{12} = I_{13}$ = 1 mA	$V_{12, 13}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 10)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}15} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\lvert I_7 \rvert$	–	–	2.5	μA
Output voltage with $R_{3\text{-}15}$ = 10 kΩ; $C_{3\text{-}15} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{18} = \leqslant 5$ μV; I_3 = 500 μA	$R_{3\text{-}15}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	$0.9\,V_5$	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}15}$	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_{18(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 11)	$V_{18(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 12) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$					
with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 13)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{18} = 300 μV to 100 mV (Fig. 14)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

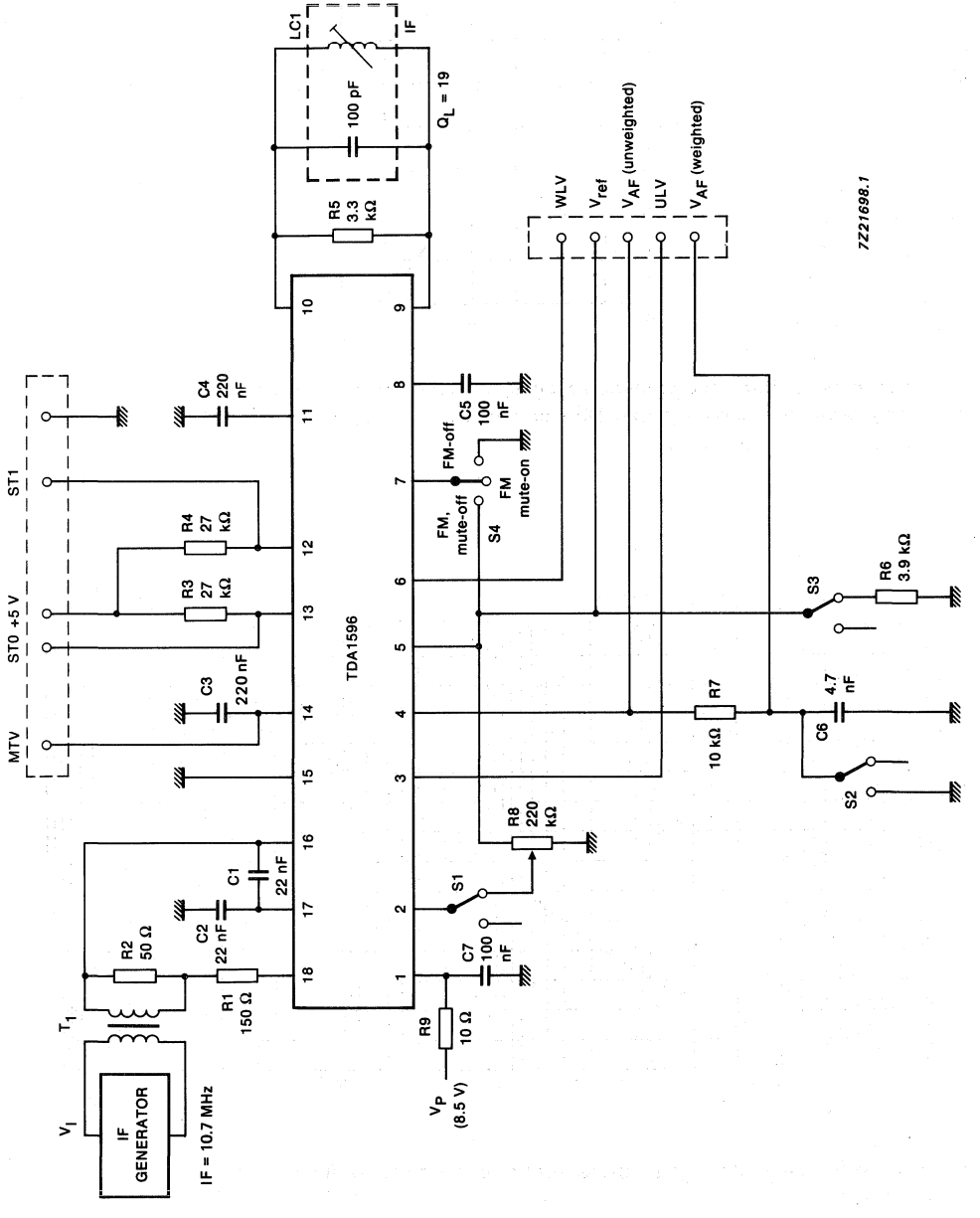


Fig. 3 Test circuit.

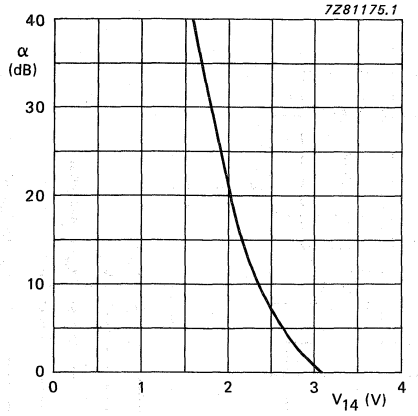


Fig. 4 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 14) and mute attenuation, $I_2 = I_7 = 0$ mA.

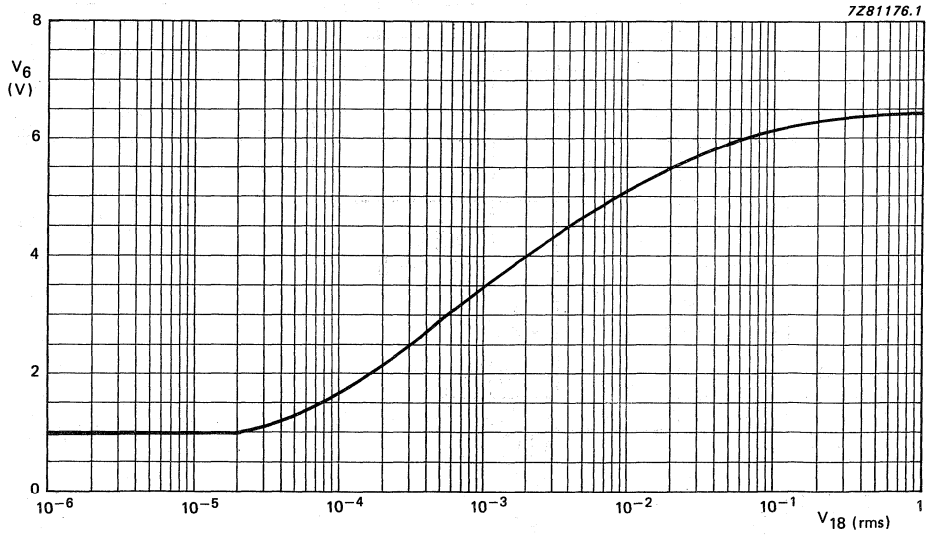


Fig. 5 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 18); $R_{6\text{-}15} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

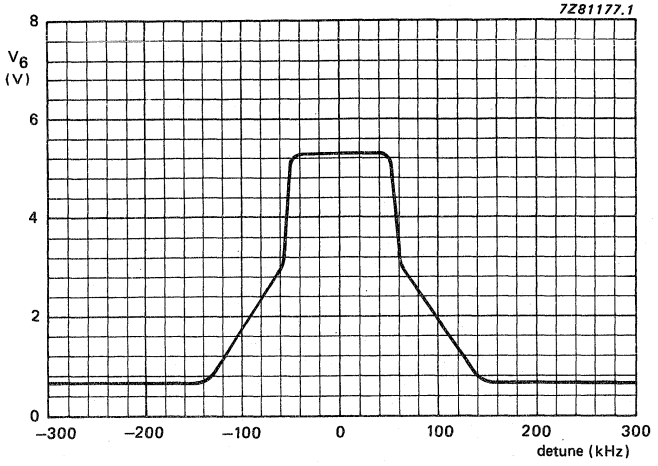


Fig. 6 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{18} = 10\ mV$.

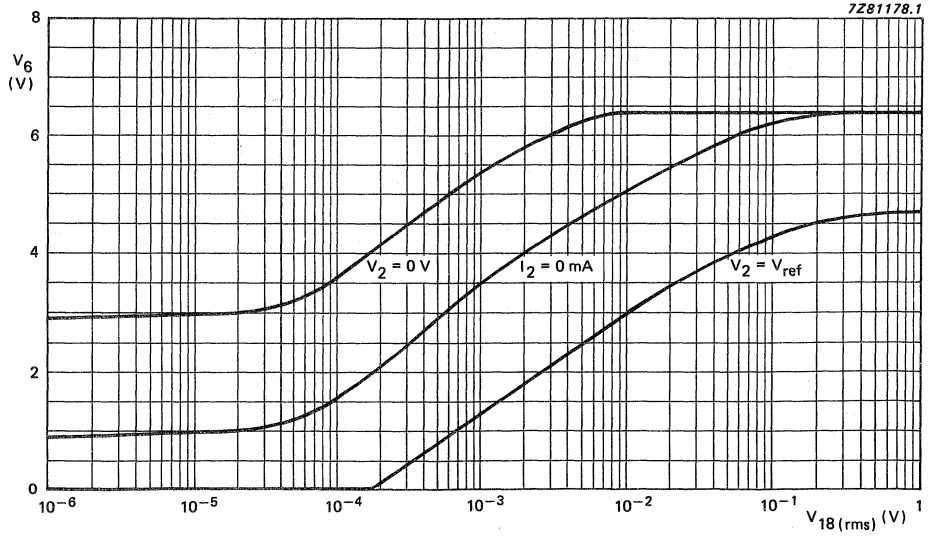
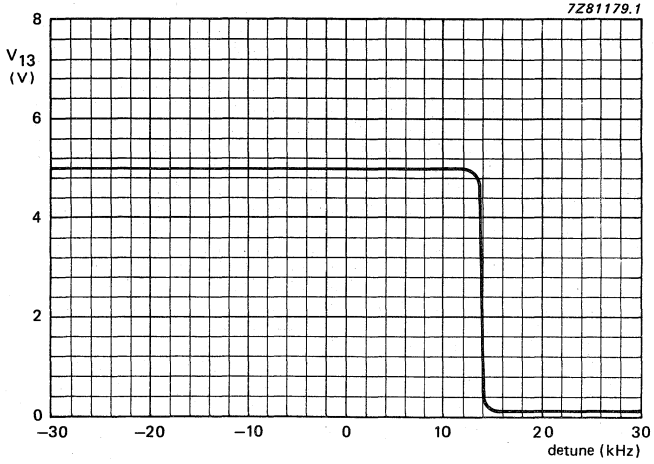
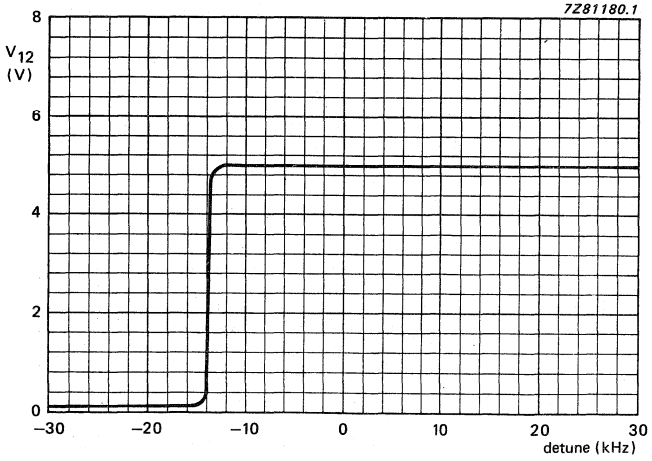


Fig. 7 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1

Fig. 8 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{18} = 10 mV.

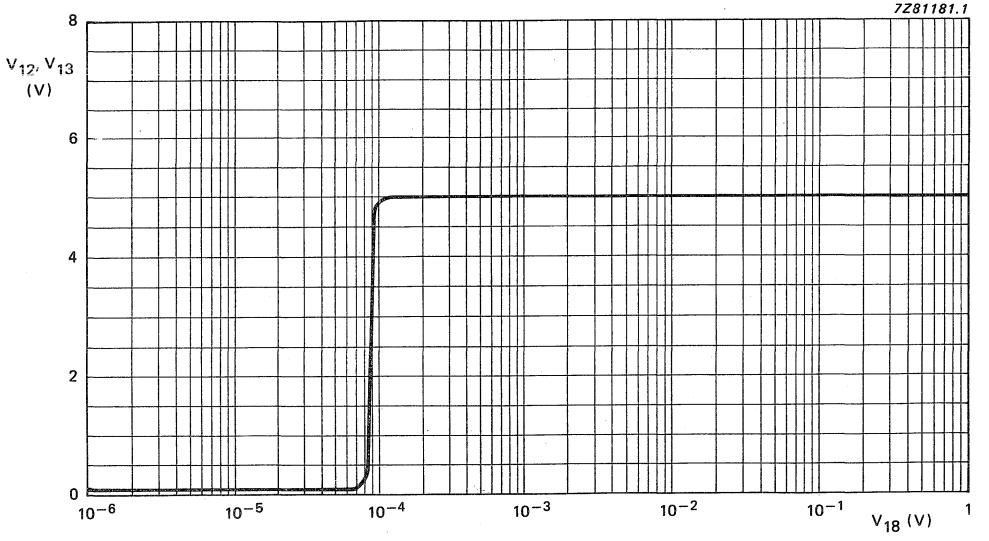


Fig. 9 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 18.

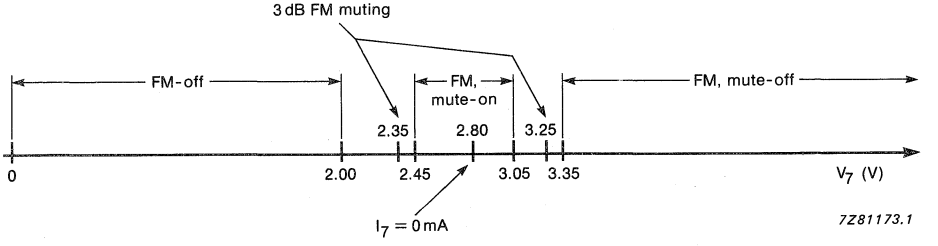
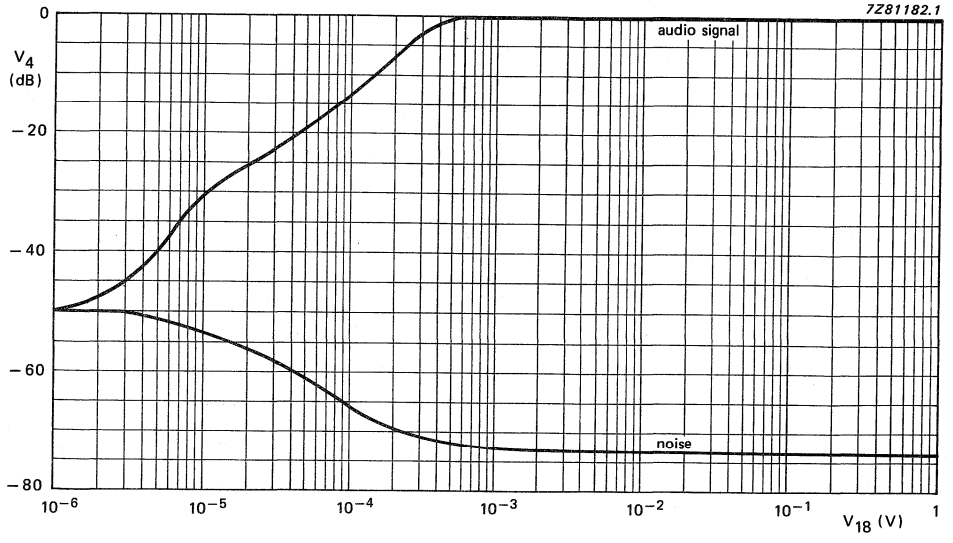
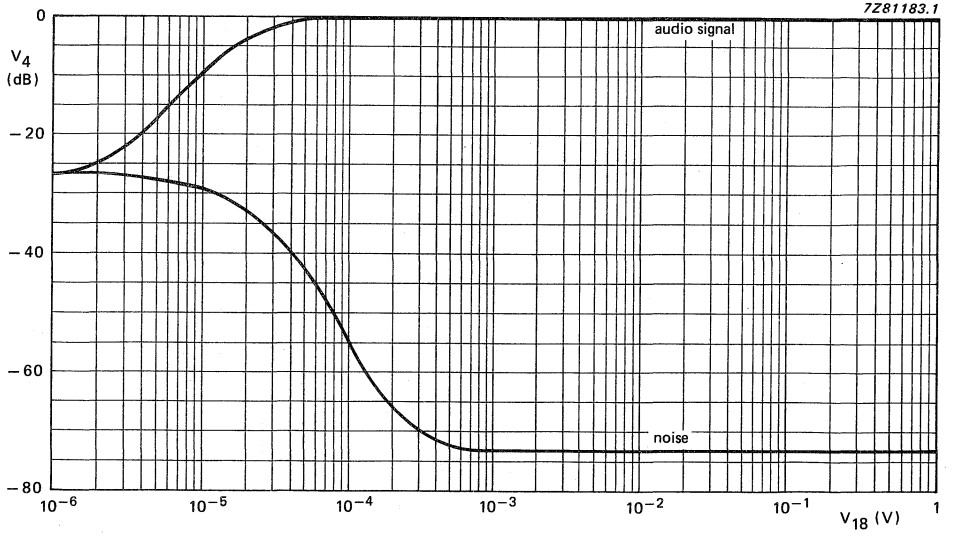


Fig. 10 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 11 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 18; measured with 50 μs de-emphasis.

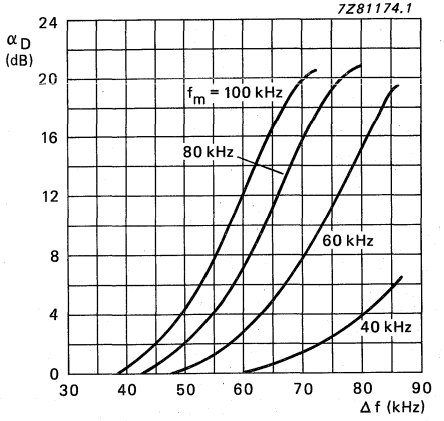


Fig. 12 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

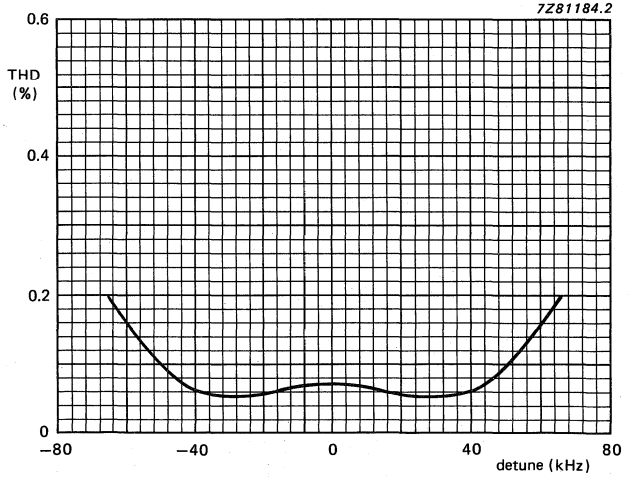
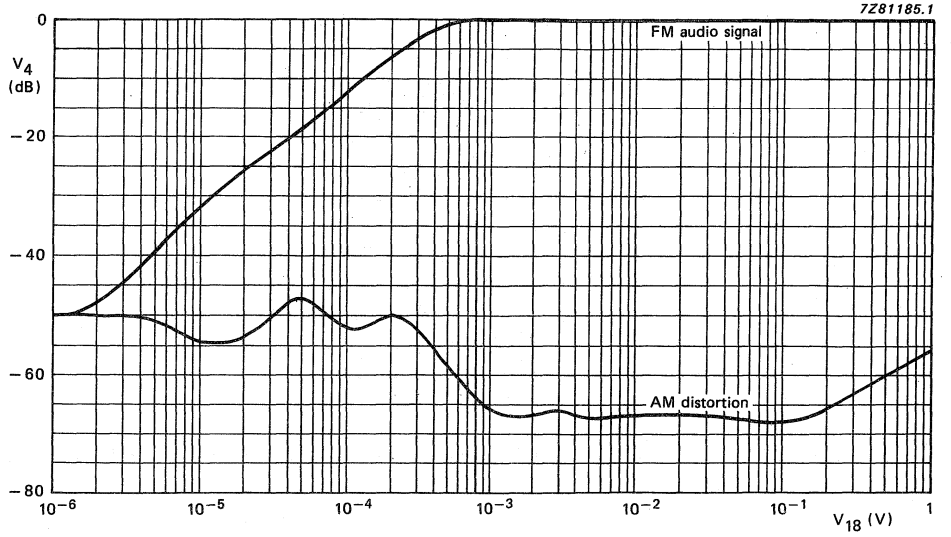
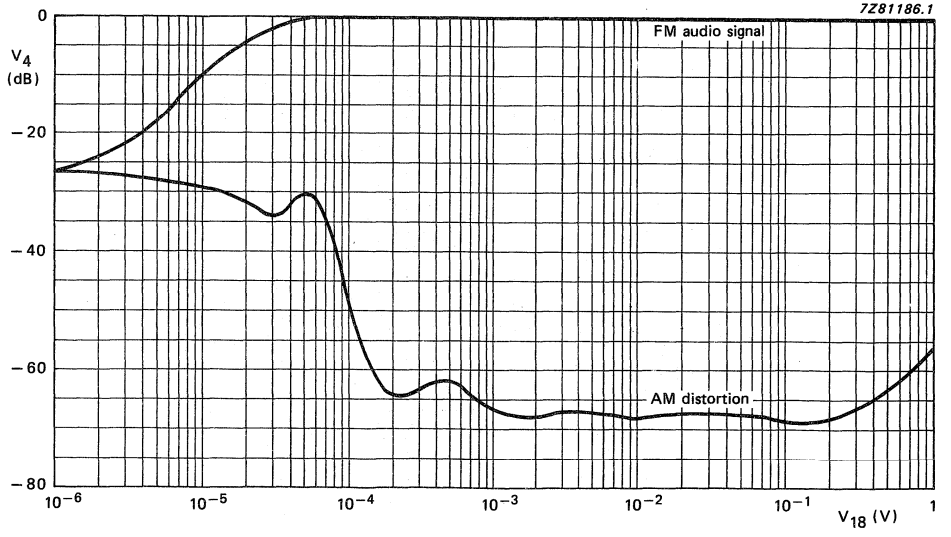


Fig. 13 THD as a function of detuning; mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{18(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 14 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596T provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

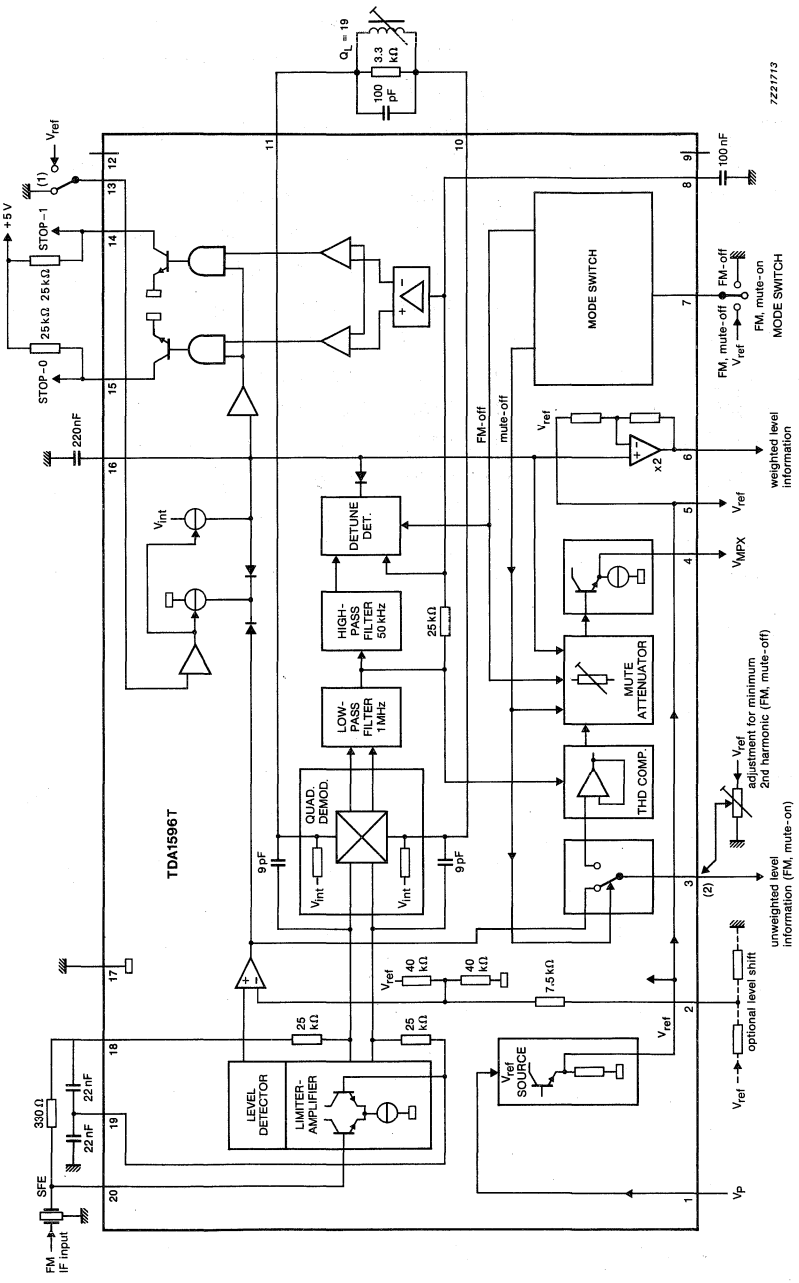
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{20(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{20(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	−40	–	+85	°C

SEE ALSO DATA SHEET FOR TDA1596

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

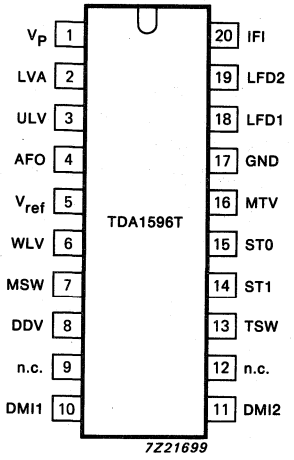


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	n.c.	not connected
10	DMI1	demodulator input 1
11	DMI2	demodulator input 2
12	n.c.	not connected
13	TSW	tau switch
14	ST1	stop pulse output 1
15	ST0	stop pulse output 0
16	MTV	mute voltage
17	GND	ground
18	LFD1	IF limiter feedback 1
19	LFD2	IF limiter feedback 2
20	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 10 and 11 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 16 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 16. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 15 and 14 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 14 and 15 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-17}$	−0.3	+16	V
Reference voltage range (pin 5)	V_{5-17}	−0.3	+10	V
Level adjustment range (pin 2)	V_{2-17}	−0.3	+10	V
Mode switch voltage range (pin 7)	V_{7-17}	−0.3	V_P	V
Control input voltage range (pin 13)	V_{13-17}	−	+6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-17}	−0.3	V_P	V
Tuning-stop output voltage range				
STOP-0 (pin 15)	V_{15-17}	−0.3	V_P	V
STOP-1 (pin 14)	V_{14-17}	−0.3	V_P	V
Tuning-stop output current				
STOP-0 (pin 15)	I_{15}	−	2	mA
STOP-1 (pin 14)	I_{14}	−	2	mA
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+2000	V
pin 5	V_{es}	−2000	+900	V
pin 6	V_{es}	−2000	+1600	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)}$ = 95 K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-17} = 8.5$ V; $V_I = V_{20(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 10, 11 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 17); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{10-11}	25	40	55	kΩ
	C_{10-11}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{10, 11(p-p)} \leqslant 100\ \mu V$; $V_{20(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-17}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 16)					
at $V_{20(rms)} \leqslant 5\ \mu V$	V_{16}	–	2.0	–	V
at $V_{20(rms)} = 1$ mV	V_{16}	–	3.45	–	V
Output impedance (pin 16)	R_{10-17}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-17}	15	–	–	kΩ
Internal muting (Fig. 6)					
Internal attenuation of signals ± 22.5 kHz ⩽ detuning ⩽ ± 80 kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{16} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{16} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{16} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 16)					
Pin 13 connected to ground *					
charge current	$+I_{16}$	–	8	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Pin 13 connected to V_{ref}					
charge current	$+I_{16}$	–	100	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 20) (Fig. 7):					
$V_{20(rms)} \leqslant 5\ \mu V$; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{20(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range					
$V_{20(rms)} \geqslant 50\ \mu V$ to $V_{20(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{20}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 8) at input voltage $V_{20(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ±200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{20(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 9)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{20(rms)} \leqslant 5\ \mu V$	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{20(rms)} \leqslant 5\ \mu V$	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 10 and 11)					
Stop-0: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{15} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{15} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{14} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{14} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 20)					
input voltage (RMS value) for $V_{14} = V_{15} \geqslant 3.5$ V	$V_{20(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{14} = V_{15} \leqslant 0.3$ V	$V_{20(rms)}$	–	–	50	μV
Output voltage when $I_{14} = I_{15}$ = 1 mA	$V_{14, 15}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 12)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7-17} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\|I_7\|$	–	–	2.5	μA
Output voltage with R_{3-17} = 10 kΩ; $C_{3-17} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{20} = \leqslant 5$ μV; I_3 = 500 μA	R_{3-17}	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	0.9 V_5	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	R_{3-17}	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_I = V_{20(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 13)	$V_{20(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 14) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$					
with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 15)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{20} = 300 μV to 100 mV (Fig. 16)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on)}/V_{4(FM\text{-}off)}$]		60	–	–	dB

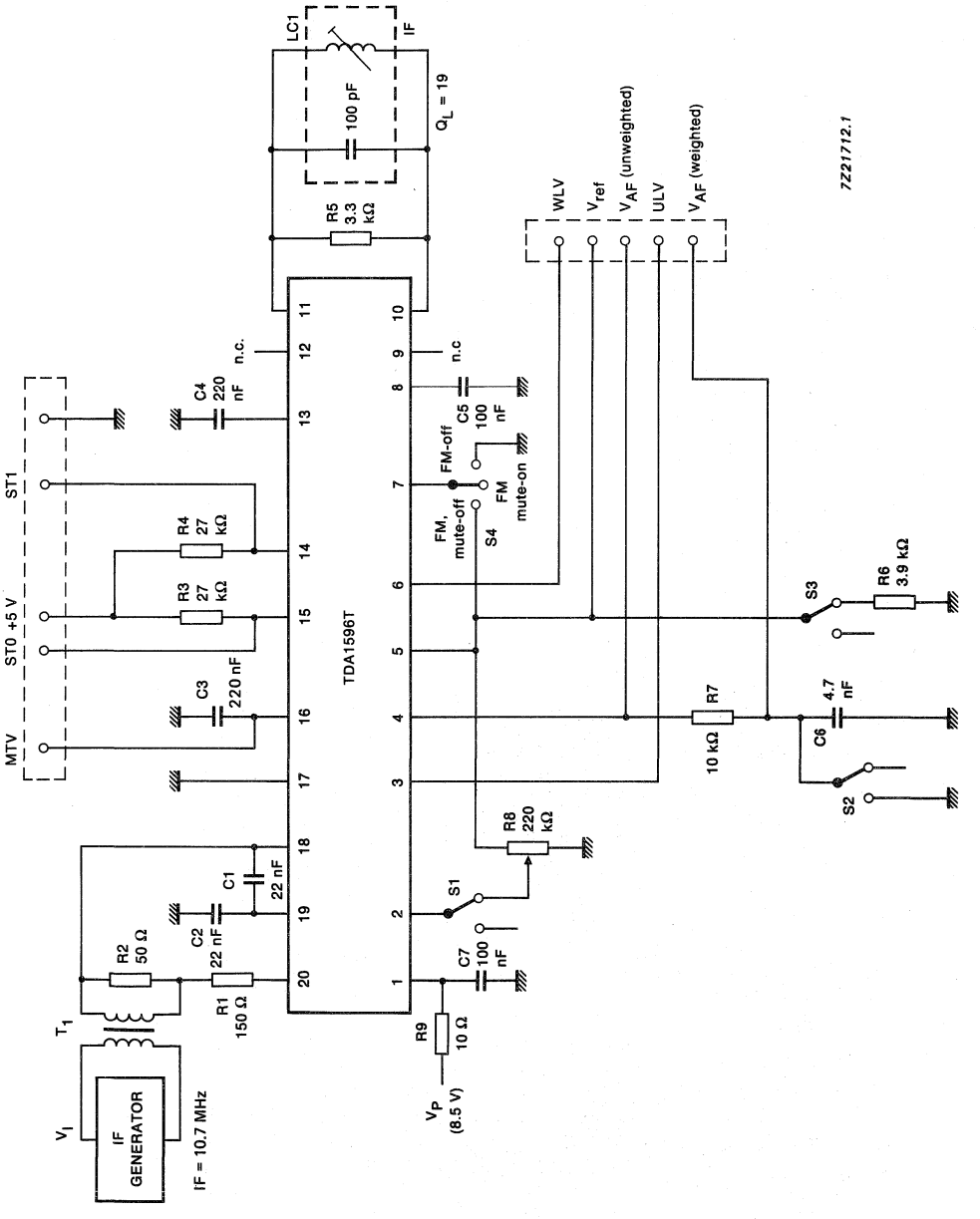


Fig. 3 Test circuit.

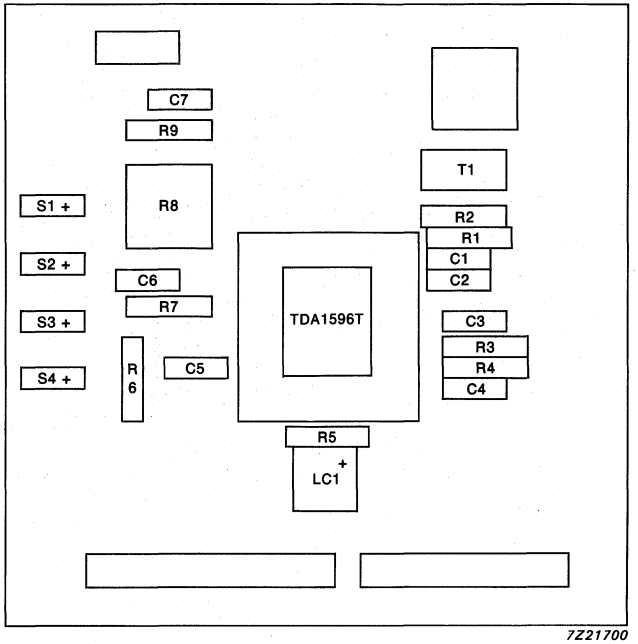


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

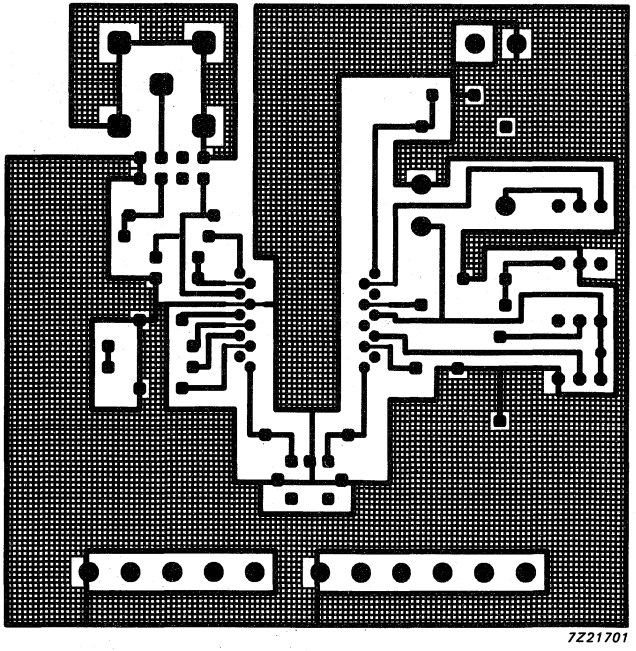


Fig. 5 Printed-circuit board showing track side.

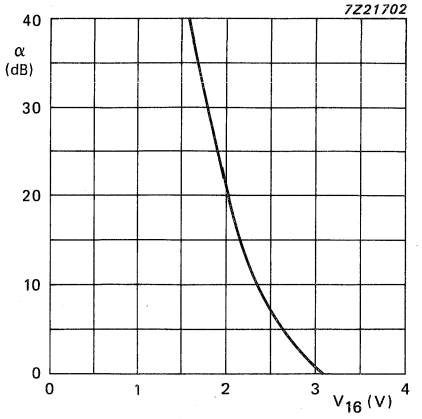


Fig. 6 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 16) and mute attenuation; $I2 = I7 = 0$ mA.

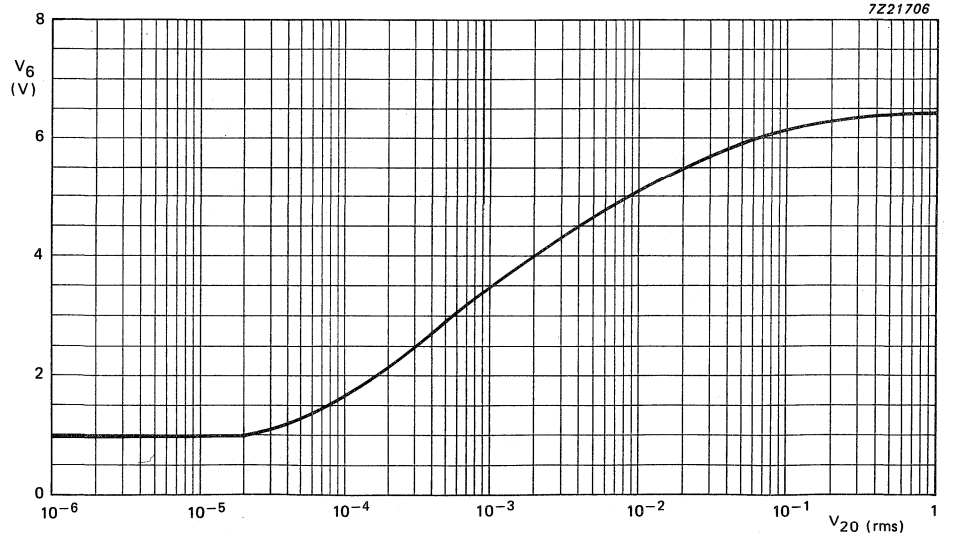


Fig. 7 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 20); $R_{6\text{-}17} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

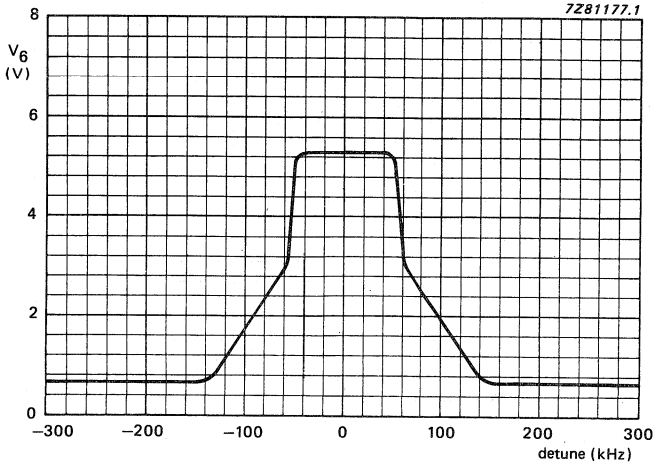


Fig. 8 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{20} = 10\ mV$.

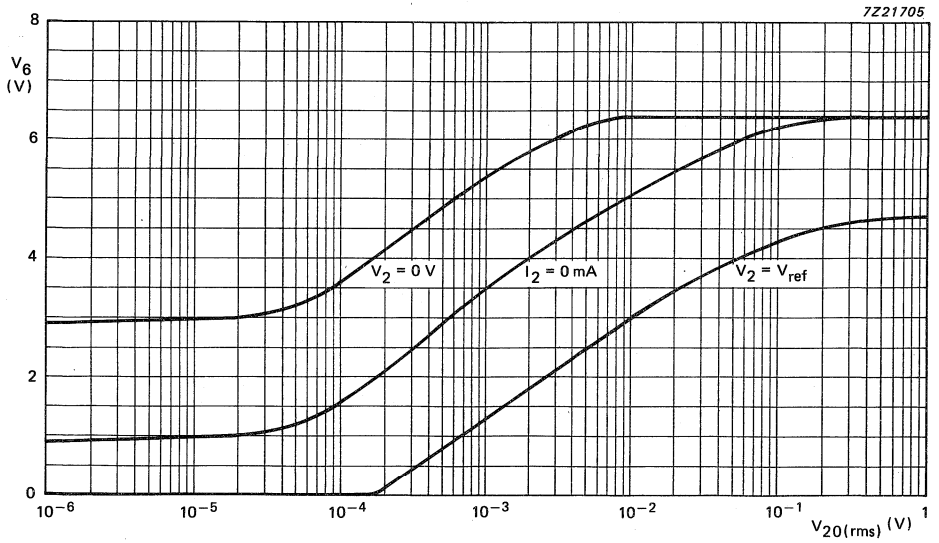
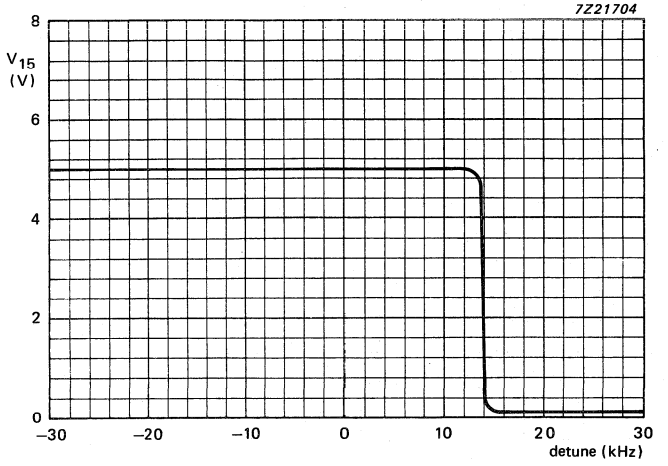
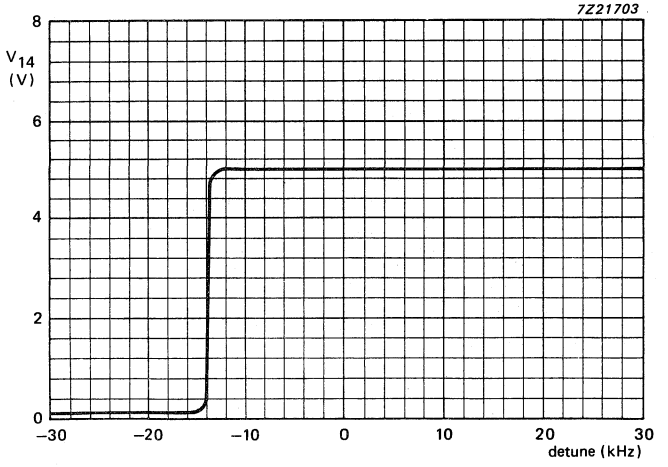


Fig. 9 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1.

Fig. 10 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{20} = 10 mV.

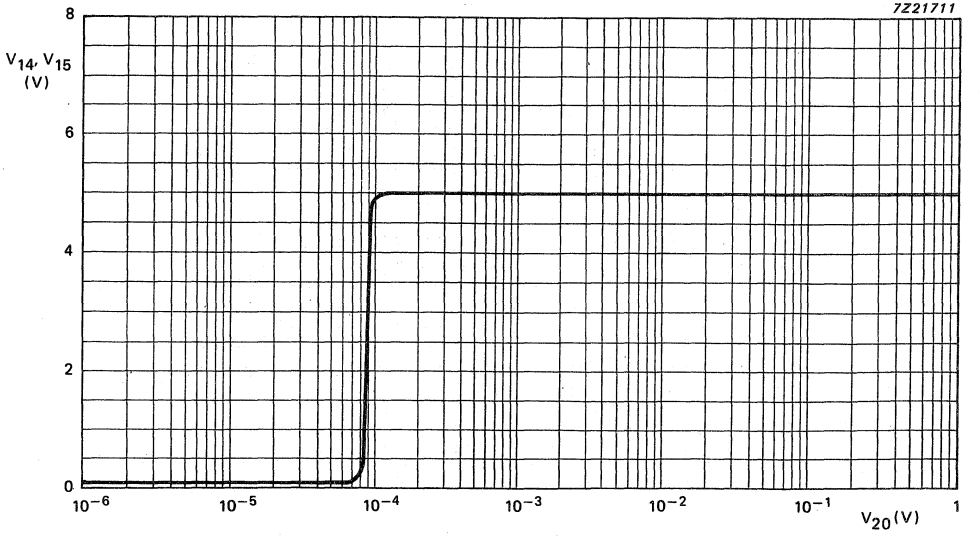


Fig. 11 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 20.

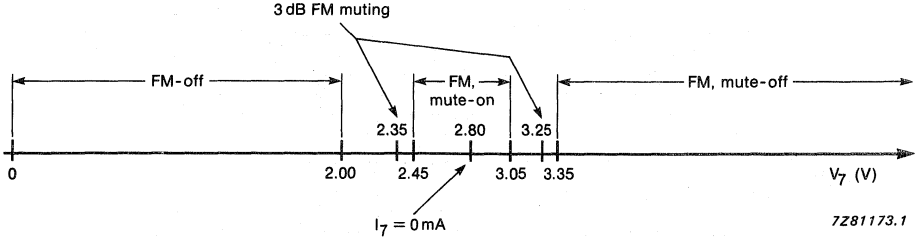
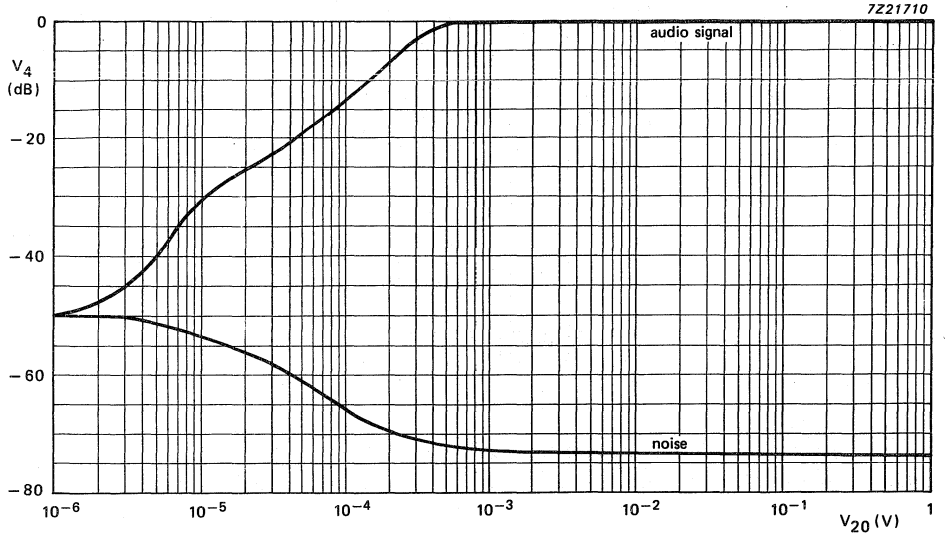
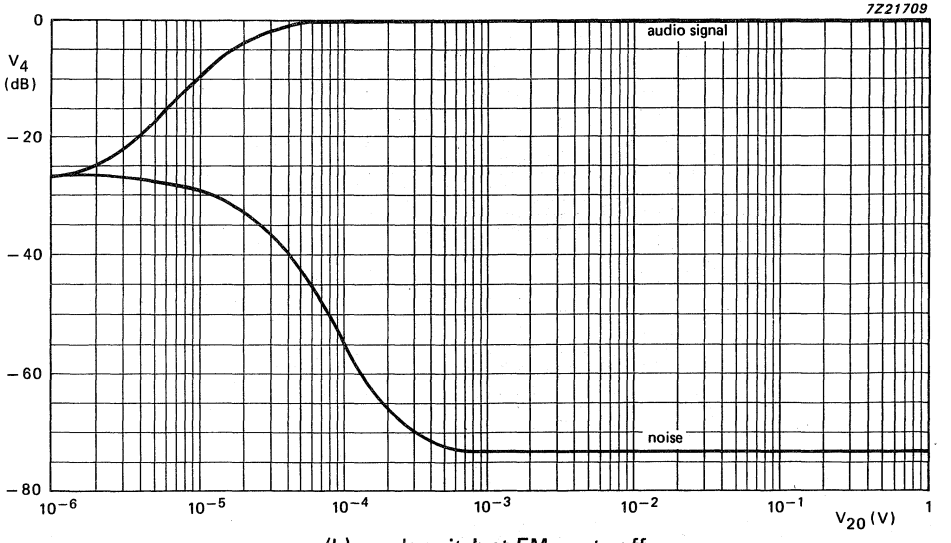


Fig. 12 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 13 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 20; measured with 50 μs de-emphasis.

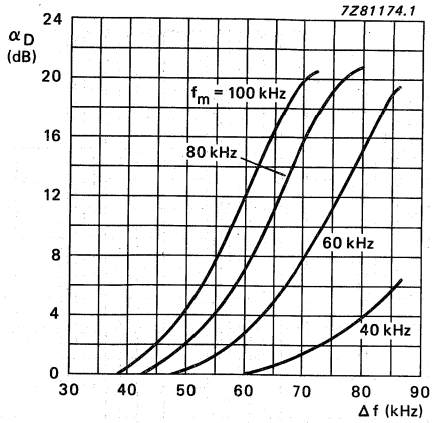


Fig. 14 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

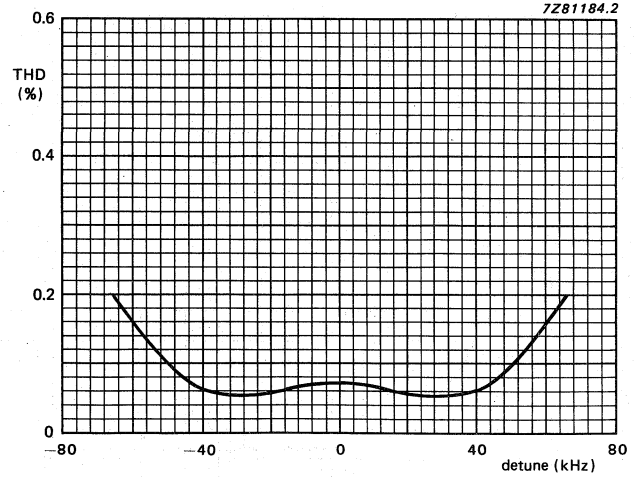
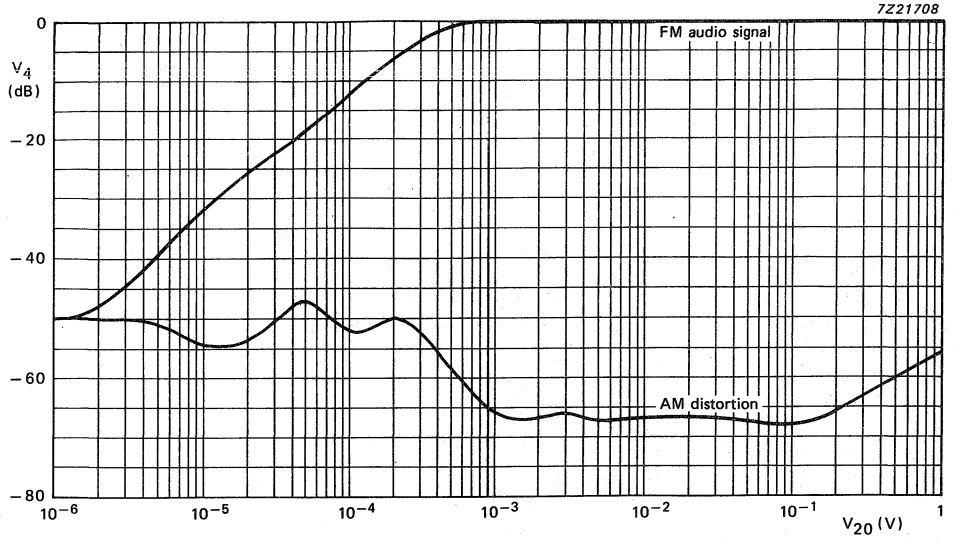
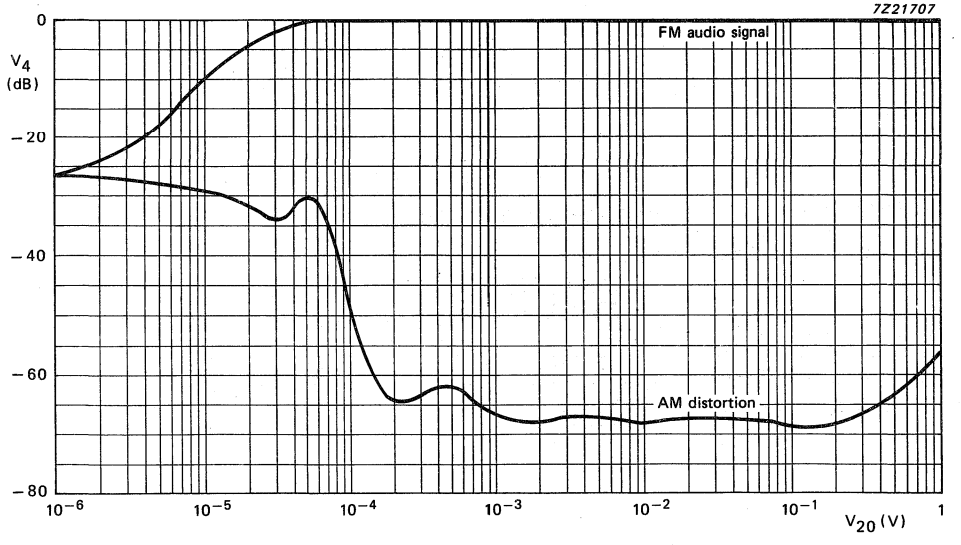


Fig. 15 THD as a function of detuning, mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{20(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 16 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	March 1992

TDA1599/T
IF amplifier/demodulator for FM radio receivers

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; $\Delta f = \pm 75$ kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; $\Delta f = \pm 75$ kHz)	–	0.1	0.3	%
	with K2-adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature range	–40	–	+85	°C

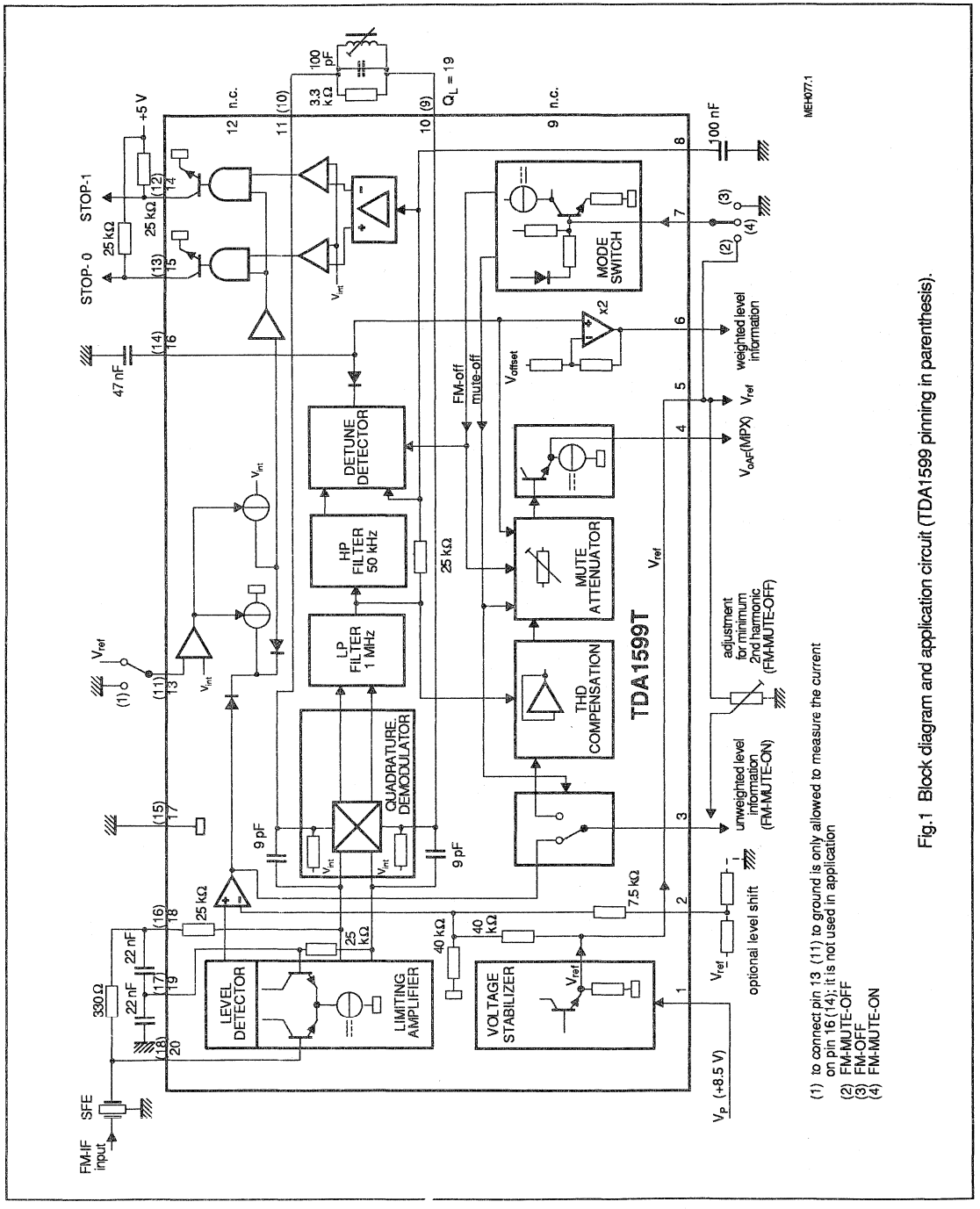
All pin numbers mentioned in this data sheet refer to the SO-version (TDA1599T) unless otherwise specified.

GENERAL DESCRIPTION

The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receivers circuits.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599T	20	mini-pack	plastic	SOT163A
TDA1599	18	DIL	plastic	SOT102



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14); it is not used in application
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1599 pinning in parenthesis).

IF amplifier/demodulator for FM radio receivers

TDA1599/T

PINNING (SO-version TDA1599T, pinning for DIL-version in parenthesis)

SYMBOL	PIN		DESCRIPTION
V_P	1	(1)	supply voltage (+8.5 V)
LVA	2	(2)	level adjustment for stop condition
ULV	3	(3)	unweighted level output / K2 adjustment
V_{oAF}	4	(4)	audio frequency output (MPX signal)
V_{ref}	5	(5)	reference voltage output
WLV	6	(6)	weighted level output
MODE	7	(7)	mode switch input
DDV	8	(8)	detune detector voltage
n. c.	9	-	not connected
DEMI1	10	(9)	demodulator input 1
DEMI2	11	(10)	demodulator input 2
n. c.	12	-	not connected
TSW	13	(11)	tau switch input
ST1	14	(12)	STOP-1, stop pulse output 1
ST0	15	(13)	STOP-0, stop pulse output 0
MUTE	16	(14)	muting voltage
GND	17	(15)	ground (0 V)
LFB1	18	(16)	IF limiter feedback 1
LFB2	19	(17)	IF limiter feedback 2
V_{iIF}	20	(18)	IF signal input

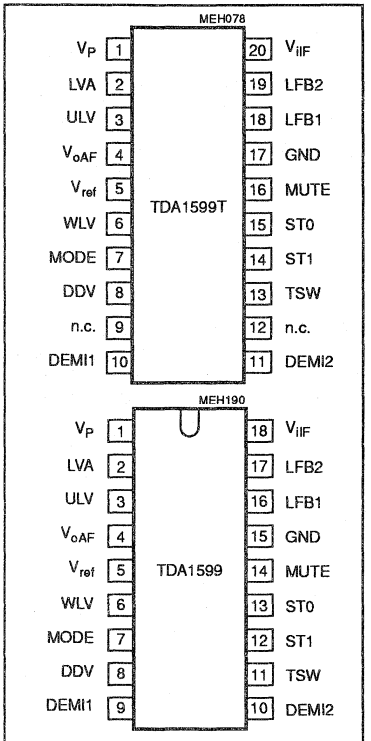


Fig.2 Pin configurations.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling. Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.

The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth on the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz.

Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19. Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse.

The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals. The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal. The unweighted level detector output signal is available in FM-MUTE-ON condition (mode switch).

The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES (TDA1599T pinning)
In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	−0.3	13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11, 16	−0.3	10	V
V_{n2}	voltage at pins 7, 3, 8, 14, 15, 18 19 and 20	−0.3	V_P	V
V_{13}	voltage on pin 13	–	6	V
$I_{14, 15}$	current at pins 14 and 15	–	2	mA
P_{tot}	power dissipation	–	360	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	−40	85	°C
V_{ESD}	electrostatic handling*			
	all pins except 5 and 6	–	±2000	V
	pin 5	–	+900	V
			−2000	V
	pin 6	–	+1500	V
			−2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	for DIL18 version TDA1599	80 K/W
	for SO20 version TDA1599T	90 K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS (TDA1599T pinning)
V_P = 8.5 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	–	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		–	0	–	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{ref}$	–	–	V
	input voltage for FM-OFF	AF attenuation >60 dB	–	–	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	$V_{iIF} \leq 5$ µV RMS on pin 20	2.75	3.1	3.45	V
RR_{1000}	power supply ripple rejection on pin 4	f = 1000 Hz; V_{ripple} = 50 mV RMS	33	36	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 15; Fig.10				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP 1	on pin 14; Fig.9				
	for $V_{14} \geq 3.5$ V		–	–	−14.0	kHz
	for $V_{14} \leq 0.3$ V		−22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.8				
		$V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	I_5 = −1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = −1 mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/VK

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External muting						
V_{16}	muting voltage at $I_2 = 0$	$V_{20} \leq 5$ μV RMS; Fig.11	1.45	1.75	2.05	V
		$V_{20} = 1$ mV RMS	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 μV ≤ V_{20} ≤ 100 mV)					
	20 Δlog V_{20} = 20 dB(ΔV_{16} /Δ log V_{20})		–	0.85	–	V/dec
Internal mute	$\alpha = 20 \log (\Delta V_{4\ (FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\ (FM\text{-}MUTE\text{-}ON)})$					
α	mute voltage	$V_{16} \geq V_{ref}$	–	0	–	dB
		$V_{16} = 0.77\ V_{ref}$	1.5	–	4.5	dB
		$V_{16} = 0.55\ V_{ref}$	–	20	–	dB
I_{16}	current for capacitor (pin16)					
	charge current	$V_{13} = 0$ V*	–	–8	–	μA
	discharge current	$V_{13} = 0$ V*	–	+120	–	μA
	charge current	$V_{13} = V_{ref}$	–	–100	–	μA
	discharge current	$V_{13} = V_{ref}$	–	+120	–	μA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ μV RMS; Fig.13	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.5	–	4.7	V
		±200 kHz detuning	1.2	1.5	1.8	V
	output voltage at $V_2 = V_5$	$V_{20} \leq 5$ μV RMS	–	–	0.3	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/VK
Δf	detuning frequency	$V_6 = 1.8$ V; Fig.12	90	–	160	kHz
S	steepness of control voltage (slope: 50 μV ≤ V_{20} ≤ 50 mV)					
	20 Δlog V_{20} = 20 dB (ΔV_6 /Δ log V_{20})		1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	Δf = 125 ±20 kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{ref}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{ref}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

* To connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14); it is not used in application.

OPERATING CHARACTERISTICS (TDA1599T pinning)
V_P = 7.5 to 12 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS on pin 20; de-emphasis of 50 μs; tuned circuit on pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value, pin 20)	$V_7 = V_{ref}$; FM-MUTE-OFF	14	22	35	μV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{ref}$	–	15	–	μV
	S/N = 46 dB	$V_7 = V_{ref}$	–	60	–	μV
S/N	signal-to-noise ratio	deviation ±75 kHz	–	82	–	dB
V_o	AF output signal (RMS value, pin 4)		180	200	220	mV
THD	total harmonic distortion without de-emphasis	deviation ±75 kHz; f_m = 1 kHz, I_7 = 0				
	without detuning		–	0.1	0.3	%
	±25 kHz detuning		–	–	0.6	%
	compensated via pin 3	$V_7 = V_{ref}$	–	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4 (V_3 = 0) - V_4 (V_3 = V_{ref})$)		10	–	–	mV
α_{AM}	AM suppression on pin 4	$V_7 = V_{ref}$; m = 30%				
	V_i = 0.3 to 1000 mV RMS	on pin 20	46	55	–	dB
	V_i = 1 to 300 mV RMS	on pin 20	60	65	–	dB
Dynamic mute attenuation $\alpha = 20 \log (\Delta V_{4\ (FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\ (FM\text{-}MUTE\text{-}ON)})$						
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz; V_2 = 1 V	–	14	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 15; Fig.10				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
	detuning frequency for STOP 1	on pin 14; Fig.9				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.8				
		$V_{14, 15} \geq 3.5$ V	250	–	–	μV
		$V_{14, 15} \leq 0.3$ V	–	–	50	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ
V_8	voltage on capacitor	$I_7 = 0$; $V_i \leq 5$ μV RMS on input pin 20	-	2.2	-	V
Level detector		$I_7 = 0$				
V_6	output voltage	$V_{20} \leq 5$ μV RMS	0.1	-	1.1	V
		$V_{20} = 1$ mV RMS	3.5	-	4.7	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	$I_5 = -1$ mA	3.3	3.7	4.1	V

Operation with AM-IF

Level and stop information (on pins 6, 13, 14, 15 and 16) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonance circuit is provided for demodulator (Fig.17).

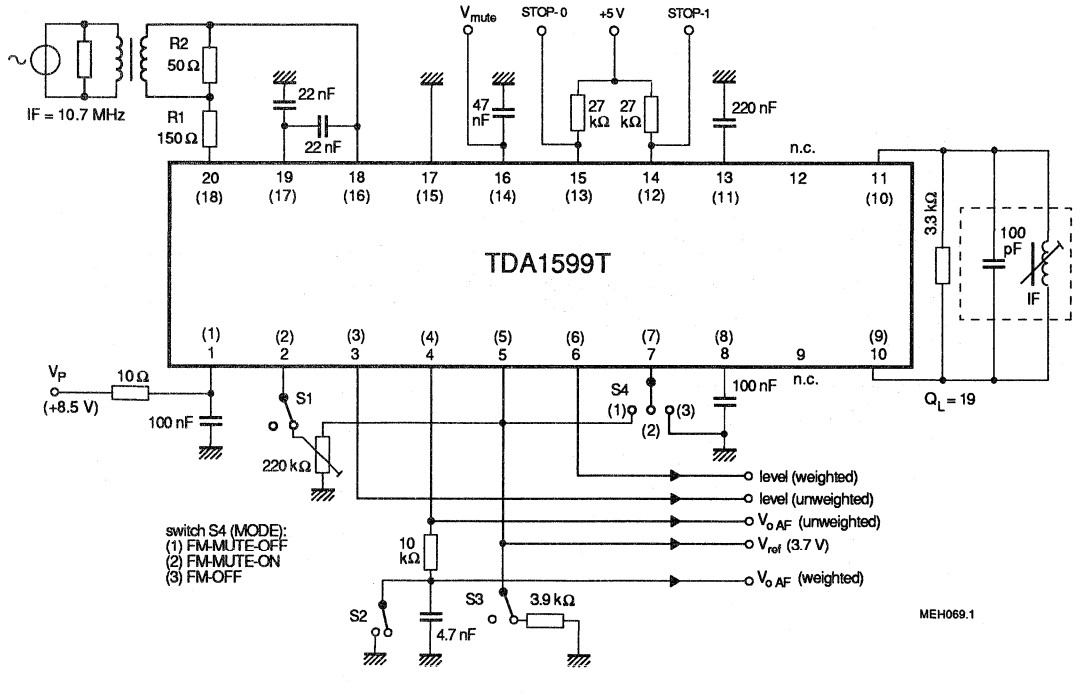
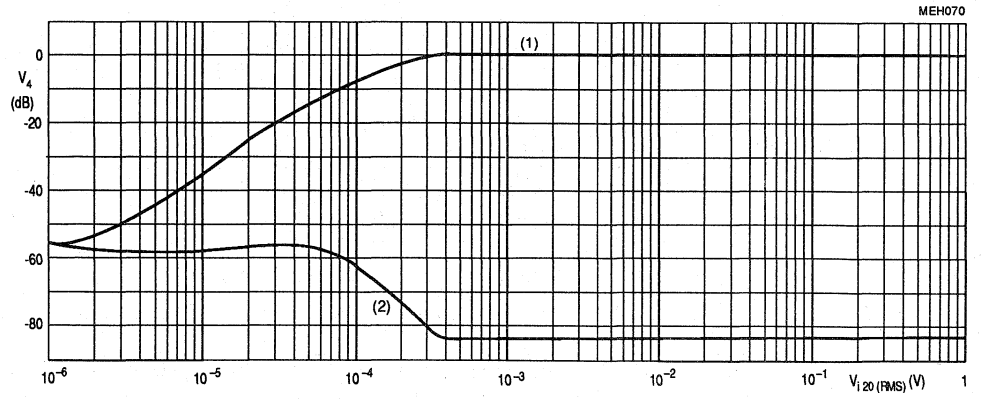
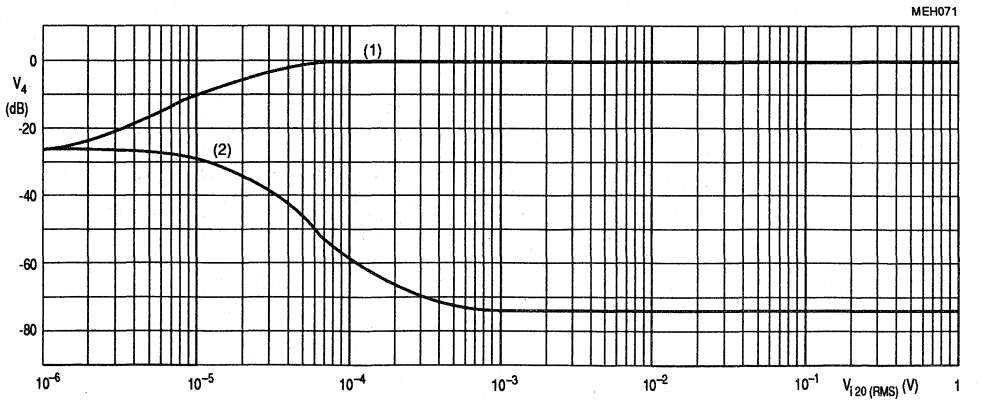


Fig.3 Test circuit (TDA1599 pinning in parenthesis).



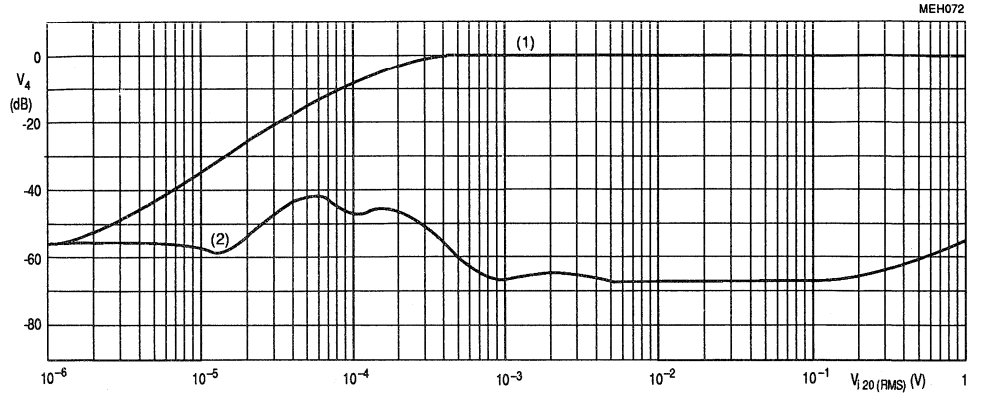
(1) audio signal
(2) noise

Fig.4 FM-MUTE-ON: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



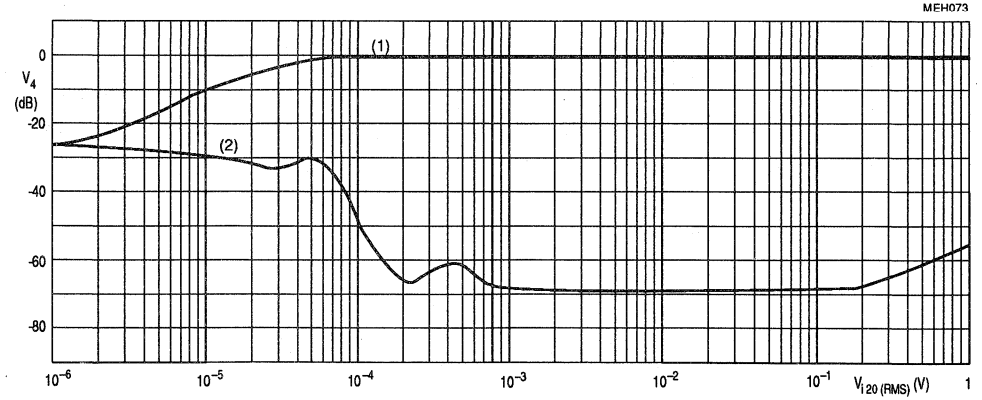
(1) audio signal
(2) noise

Fig.5 FM-MUTE-OFF: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 µs.



(1) audio signal
(2) spurious AM signal

Fig.6 FM-MUTE-ON: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-OFF: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

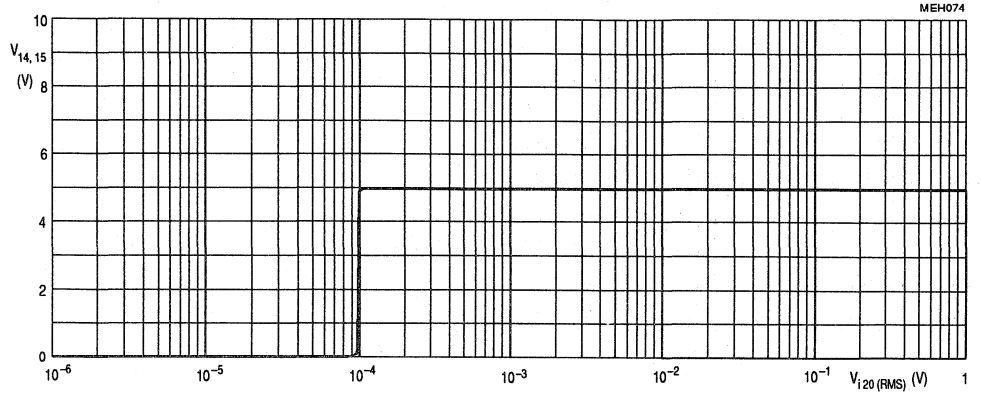


Fig.8 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

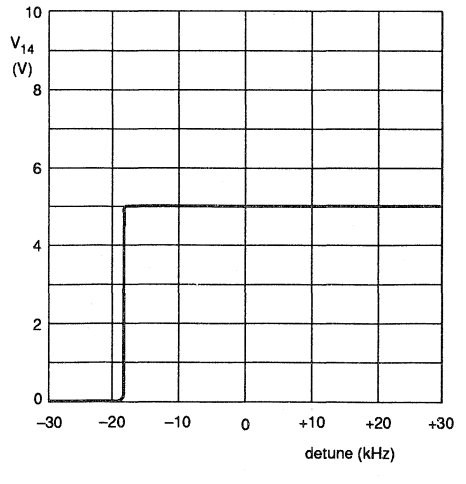


Fig.9 STOP-1 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

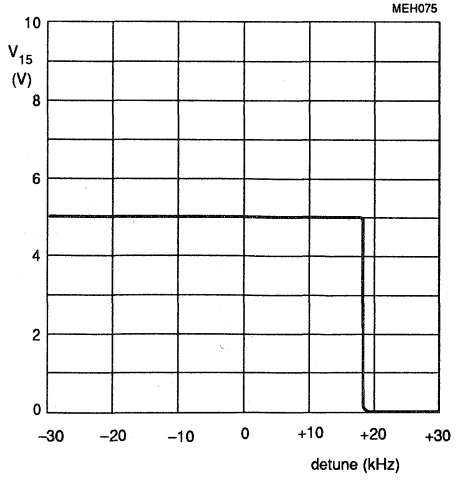


Fig.10 STOP-0 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

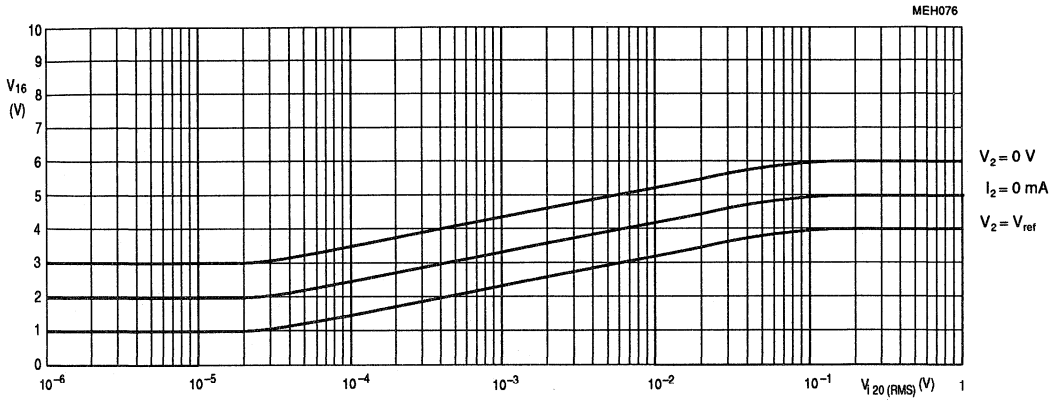


Fig.11 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range.

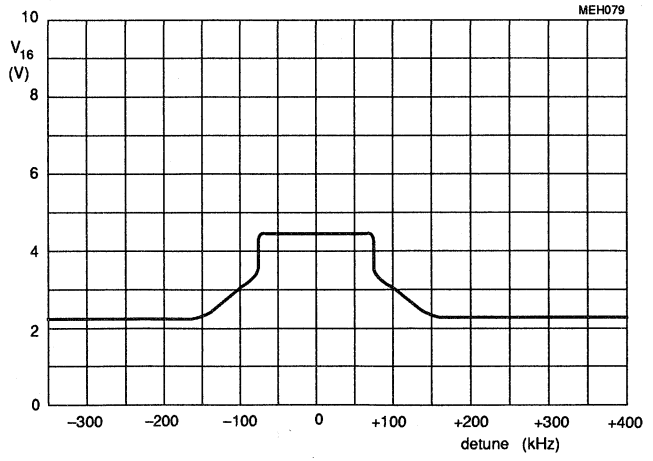


Fig.12 Mute voltage V_{16} dependent on detuning; V_{iIF} = 10 mV RMS.

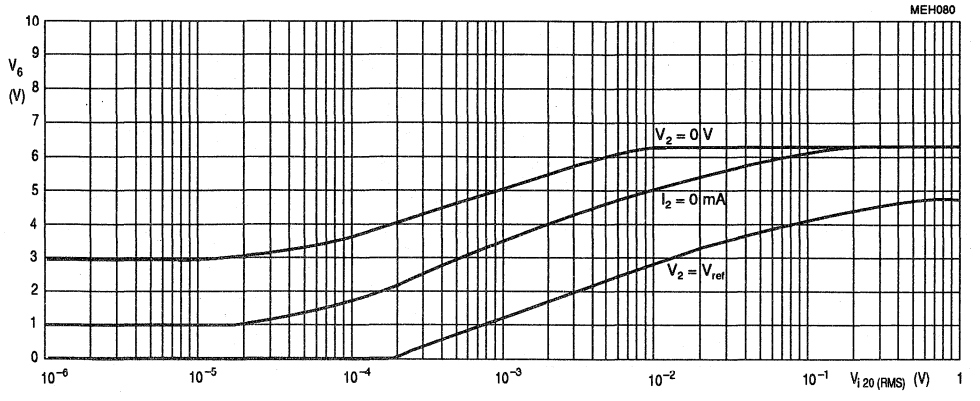


Fig.13 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

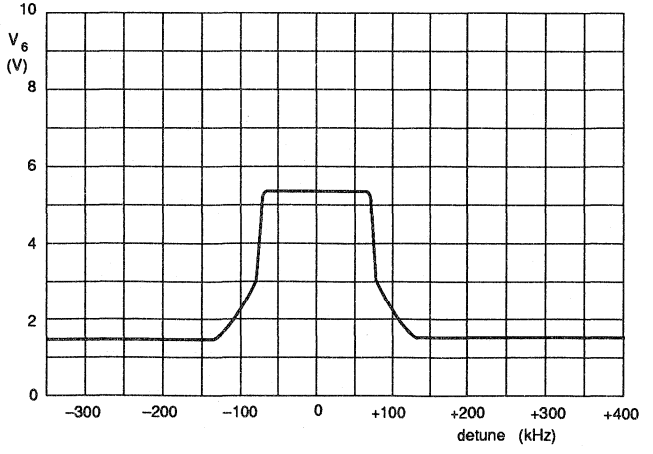


Fig.14 Control voltage V_6 dependent on detuning; V_{iIF} = 10 mV RMS.

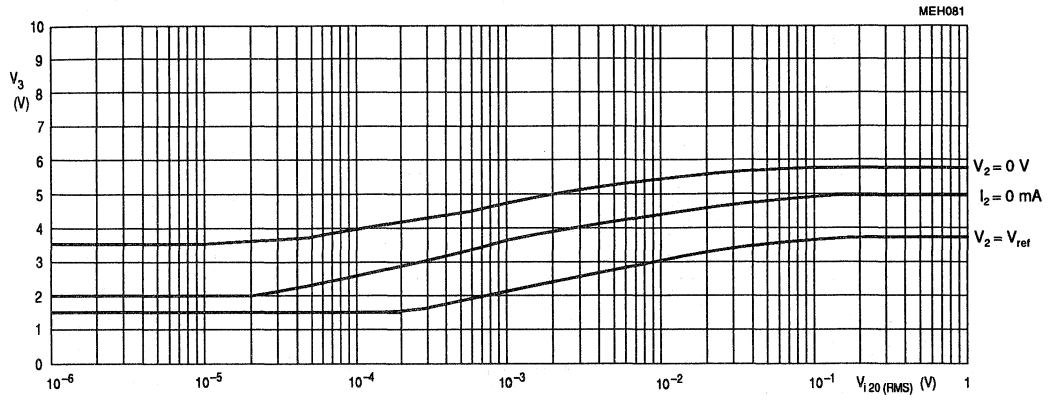


Fig.15 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

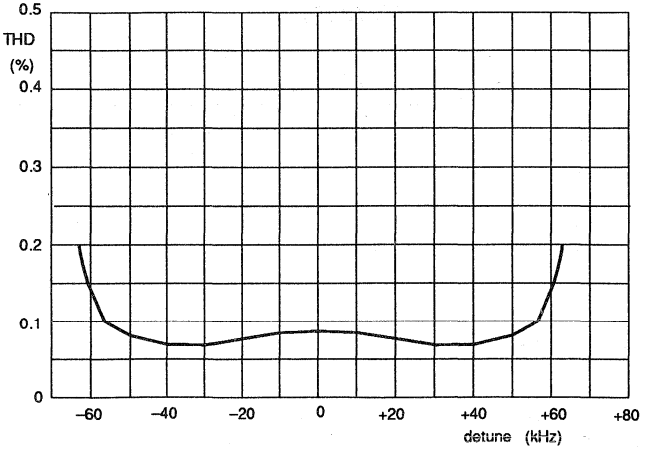


Fig.16 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

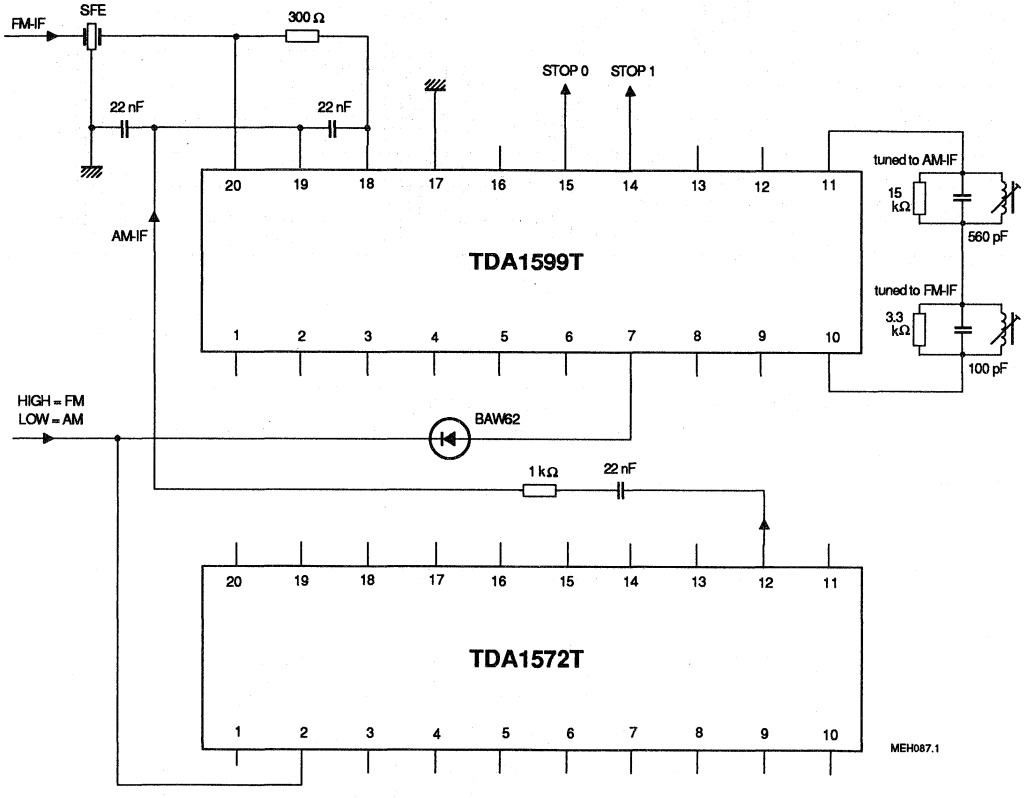


Fig.17 Interface for AM stop pulse application (mini-pack version).

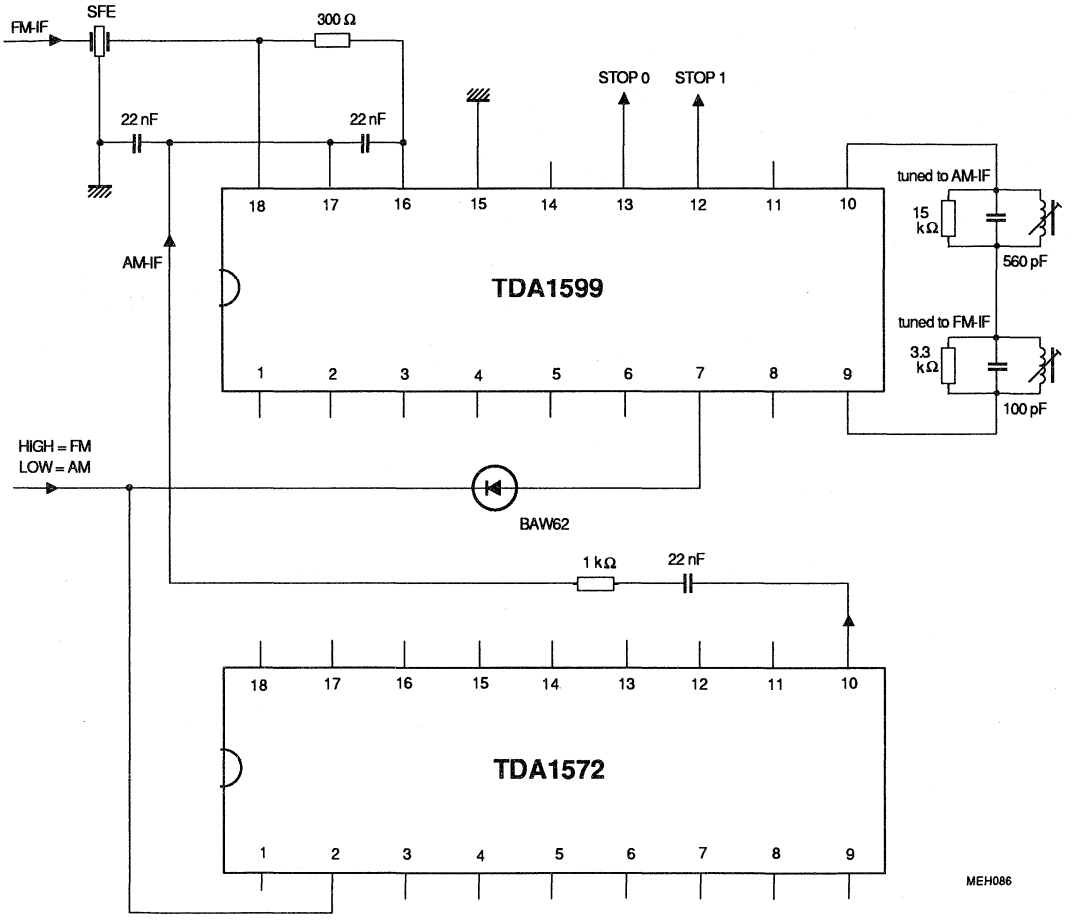


Fig.18 Interface for AM stop pulse application (DIL version).

Double-deck playback/record IC (DDPR)

TDA1602A

FEATURES

- Two stereo playback preamplifiers
- Stereo playback amplifier
- High speed dubbing headswitch for channel A
- Record/playback headswitch for channel B
- Dubbing switch
- Stereo record amplifier
- Automatic level control
- Erase and bias oscillator
- Tape selector
- Reference voltage source (1/2 V_P)
- Logic part

GENERAL DESCRIPTION

The TDA1602A is a Dolby B compatible recorder IC, which has been designed for use in double-deck recorders for Ferro/Chrome with high speed dubbing. The device performs all the basic recorder functions and needs only a very simple peripheral circuit of a few components. The DDPR may also be used in applications with automatic reverse.

All functions of the DDPR are selected by externally applied DC voltage levels. The circuit is designed for use with a mains-fed asymmetrical power supply but can also be used with a symmetrical power supply (because of its own 1/2 V_P reference voltage source).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1602A	40	DIL	plastic	SOT129

QUICK REFERENCE DATA

All voltages referenced to pin 12, all currents positive into the IC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		7.0	–	18.0	V
Playback amplifier						
G	gain	f = 315 Hz	–	57	–	dB
S/N	signal-to-noise ratio		–	53	–	dB
THD	total harmonic distortion	V_O = 150 mV	–	0.1	–	%
Headswitch						
$V_{ON(p-p)}$	maximum voltage (peak-to-peak value)	record mode	–	–	90	V
Record amplifier						
G	gain	f = 315 Hz	–	14	–	dB
S/N	signal-to-noise ratio		–	65	–	dB
THD	total harmonic distortion	$V_{Orecord}$ = 1.5 mV	–	0.3	–	%
Automatic level control						
ΔV_O	output voltage variation	ΔV_{line} = 20 dB	–	1	–	dB
Oscillator						
f_{OSC}	frequency range		60	–	120	kHz
$I_{O(peak)}$	output current (peak value)		140	–	–	mA
$V_{O(p-p)}$	output voltage (peak-to-peak value)		–	–	36	V
Reference voltage						
V_{ref}	output voltage		–	1/2 V_P	–	V
Logic part						
I_I	input current					
	pins 8 and 10		–	100	–	µA
	pins 7 and 9		–	–	900	µA

Double-deck playback/record IC (DDPR)

TDA1602A

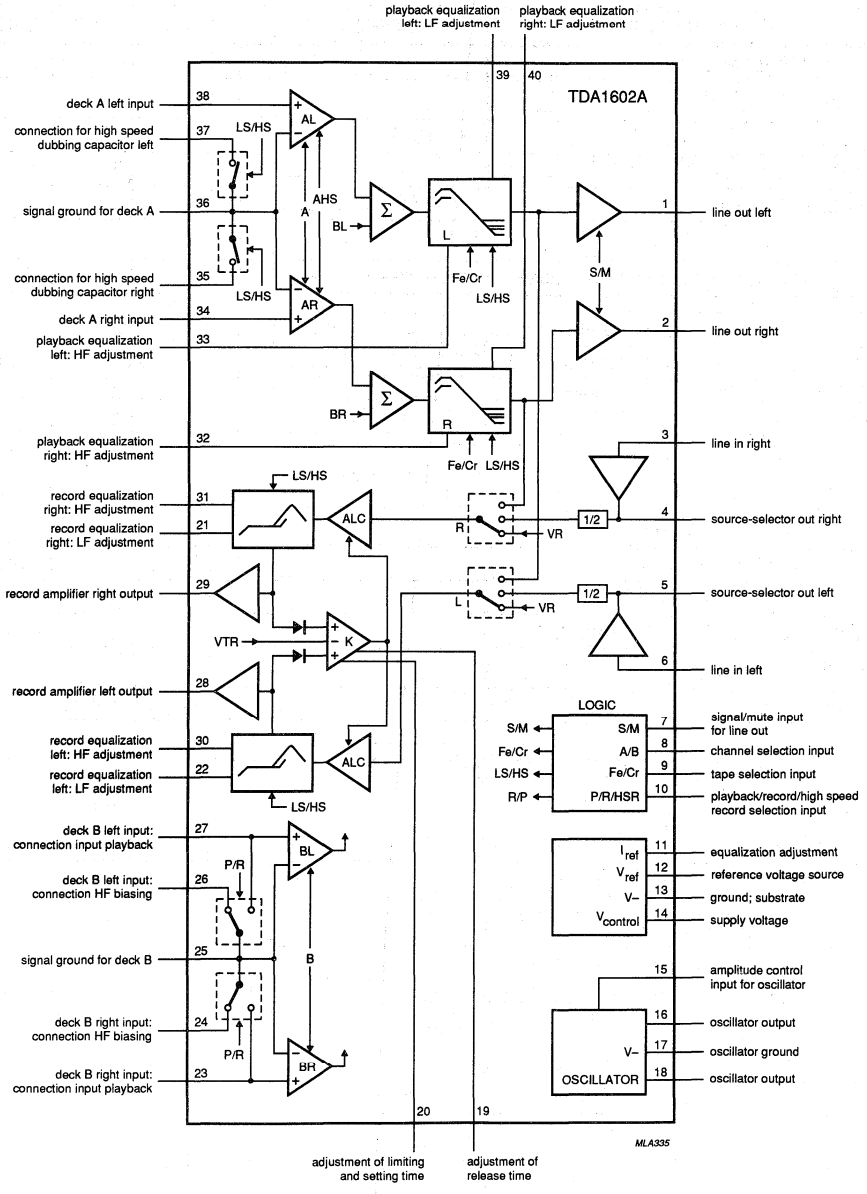


Fig.1 Block diagram.

Double-deck playback/record IC (DDPR)

TDA1602A

PINNING

SYMBOL	PIN	DESCRIPTION
LOL	1	line out left
LOR	2	line out right
LIR	3	line in right
SOR	4	source-selector out right
SOL	5	source-selector out left
LIL	6	line in left
S/M	7	signal/mute input for line out
A/B	8	channel selection input
TS	9	tape selection input
P/R/HSR	10	playback/record/high-speed record selection input
EQUADJ	11	equalization adjustment
V_{ref}	12	reference voltage source
GND	13	ground; substrate
V_P	14	supply voltage
OSCCON	15	amplitude control input for oscillator
OSCO1	16	oscillator output 1
OSCGND	17	oscillator ground
OSCO2	18	oscillator output 2
ADJRT	19	adjustment of release time
ADJLST	20	adjustment of limiting and setting time
RECERLF	21	record equalization right: LF adjustment
RECELLF	22	record equalization left: LF adjustment
BRIP	23	deck B right input: connection input playback
BRIBHF	24	deck B right input: connection HF biasing
SGNDB	25	signal ground for deck B
BLIBHF	26	deck B left input: connection HF biasing
BLIP	27	deck B left input: connection input playback
RECOL	28	record amplifier left output
RECOR	29	record amplifier right output
RECELHF	30	record equalization left: HF adjustment
RECERHF	31	record equalization right: HF adjustment
PERHF	32	playback equalization right: HF adjustment
PELHF	33	playback equalization left: HF adjustment
ARI	34	deck A right input
HSDR	35	connection for high speed dubbing capacitor right
SGNDA	36	signal ground for deck A
HSDL	37	connection for high speed dubbing capacitor left
ALI	38	deck A left input

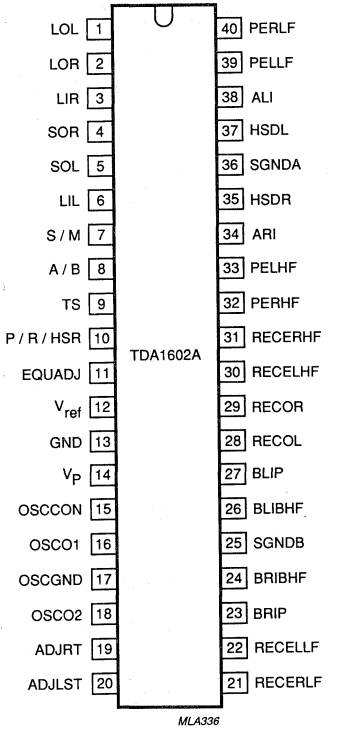


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
PELLF	39	playback equalization left: LF adjustment
PERLF	40	playback equalization right: LF adjustment

FUNCTIONAL DESCRIPTION

Playback pre-amplifier

The playback preamplifier is a linear low-noise amplifier with an internal fixed gain of 26.4 dB. The relevant preamplifier for playback of channel A or B can be selected externally.

Playback amplifier

The frequency response of the playback amplifier is determined by two external capacitors (Right: C6 and C21, Left: C5 and C20). The different equalization curves for Ferro and Chrome (with time constants of 120 µs and 70 µs respectively) are controlled by the logic part of the circuit.

High speed dubbing headswitch

This electronic switch is used to connect, or disconnect, an extra external capacitor (Right: C4, Left: C1) in parallel with the gap-loss correction capacitor.

Record/playback headswitch

This is a two position electronic switch which switches the relevant side of the head to the signal ground.

RECORD POSITION

In the record mode the input of the playback amplifier is switched to the signal ground. In this way the bias and audio signal current can be applied to the head.

PLAYBACK POSITION

In the playback mode the biasing side of the head is switched to the signal ground.

Record amplifier

The frequency response of the record amplifier is determined by means of two external capacitors (Right: C11 and C12; Left: C17 and C18).
By omitting these capacitors a flat frequency response is obtained for Dolby application.

Automatic level control

The automatic level control (ALC) has a control range of 20 dB. The variation in the output voltage is less than 2 dB (see Fig.5). The attack and recovery time of the ALC can be adjusted externally.

Erase and bias oscillator

The erase and bias oscillator provides the following:

A high frequency bias current to enable a linear magnetic recording process on the tape.
A sinusoidal voltage, the amplitude of which is determined by the applied voltage at pin 15 (see also Fig.6).
The necessary current for erasing the tape which is only activated when the circuit is switched to the record mode.

Reference voltage source

This circuit delivers an output voltage which is half the supply voltage. The output voltage can be taken as signal ground. In this way a symmetrical power supply is available for the total recorder application.

Logic part

The logic part converts the incoming information from the logic input into the necessary switching signals, used in the analog parts of the circuit. The conversion is determined by the level of the input signal (see Fig.7). The logic inputs (pins 8 and 10) are independent of signal rise and fall times. The inputs at pins 7 and 9 enable smooth switching between signal/mute and Ferro/Chrome respectively.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). All voltages referenced to pin 12; all currents positive into the iC

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
V_{7-10}	logic input voltage (pins 7 to 10)		0	V_P	V
V_{15}	control input voltage (pin 15)		0	V_P	V
$V_{16,18}$	oscillator output voltage (pins 16 and 18)		0	36	V
$V_{28,30}$	headswitch voltage (pins 28 and 30)		–45	+45	V
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		–	+150	°C
P_{tot}	total power dissipation	T_{amb} = +60 °C	–	1.8	W

DC CHARACTERISTICS

All voltages referenced to pin 12; all currents positive into the IC; All parameters are measured in the test circuit (Fig.11) at nominal supply voltage (V_P = 15 V); f = 315 Hz; tape selectors at Fe02 position; normal speed; non-Dolby application; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage range		7.0	–	18.0	V
I_P	supply current	note 1				
		playback mode	35	39	43	mA
		record mode	39	43	47	mA
Playback amplifier (Fe02/Cr02)						
G	gain at normal speed	f = 315 Hz	55	57	59	dB
B	frequency response with respect to gain	f = 30 Hz	10	12	14	dB
		Cr02, f = 10 kHz	−18	−17	−16	dB
		Fe02, f = 10 kHz	−13.5	−12.5	−11.5	dB
	left/right balance		−1	0	+1	dB
	A/B balance		−1	0	+1	dB
G	gain at double speed	f = 630 Hz	49	51	53	dB
B	frequency response with respect to gain	f = 60 Hz	10	12	14	dB
		Cr02; f = 20 kHz	−18	−17	−16	dB
		Fe02; f = 20 kHz	−13.5	−12.5	−11.5	dB
	left/right balance		−1	0	+1	dB
V_O	nominal output voltage	note 2; V_I = 200 μV	–	150	–	mV
THD	total harmonic distortion	V_I = 200 μV	–	0.1	0.3	%
		V_I = 280 μV	–	–	1	%
S/N	signal-to-noise ratio	note 3; weighted curve; 20 Hz to 20 kHz	51	53	–	dB
		weighted curve A(IEC179)	–	60	–	dB
	left/right separation	V_O = 150 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	25	–	dB
$\|Z_I\|$	input impedance		100	–	–	kΩ
I_{bias}	input bias current		–	0.5	–	μA
V_O	DC output voltage with respect to V_{ref} (V_{1-12} and V_{2-12})		−30	0	+30	mV
	A/B separation	note 4	–	340	–	μV
		note 5	–	tbf	–	mV
	suppression of output signal (channel A and B)	$V_7 = V_P$	–	90	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Record/playback headswitch						
$\|Z_{ON}\|$	impedance ON					
	playback mode	between pins 26 and 25 and pins 24 and 25; I = 100 μA(RMS)	–	35	100	Ω
	record mode	between pins 27 and 25 and pins 23 and 25; I = 1.5 mA(RMS)	–	25	50	Ω
I_{IL}	OFF-state leakage current	voltage on pins 24 and 26 of V_{DC} = ±45 V with respect to V_{ref} (pin 12)	–	1.0	2.5	μA
$\|Z_{ON}\|$	high-speed dubbing headswitch	normal speed, between pins 35 and 36 and pins 36 and 37; I = 100 μA(RMS)	–	100	1000	Ω
Record amplifier (ALC off)						
G	gain at normal speed	f = 315 Hz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
B	frequency response with respect to gain	f = 10 kHz	8.5	10.0	11.5	dB
		Dolby; f = 10 kHz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
	left/right balance		–1	0	+1	dB
G	gain at double speed	note 7; f = 630 Hz	19	20	21	dB
B	frequency response with respect to gain	f = 20 kHz	8	10	12	dB
	left/right balance		–1	0	+1	dB
V_O	maximum output voltage	V_{Osel} = 800 mV; f = 1 kHz; THD = 3%	–	4.0	–	V
THD	total harmonic distortion	ALC switch ON; f = 1 kHz				
		V_{Osel} = 1 V	–	–	0.7	%
		V_{Osel} = 3 V	–	0.5	–	%
S/N	signal-to-noise ratio	note 8; weighted curve 20 Hz to 20 kHz	–	60	–	dB
		weighted curve A(IEC179)	–	65	–	dB
		Dolby; weighted curve 20 Hz to 20 kHz	70	73	–	dB
	left/right separation	V_{Osel} = 300 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	30	–	dB
$\|Z_I\|$	input impedance		100	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Record amplifier (ALC off)						
V_O	DC output voltage with respect to V_{ref}	normal speed record, V_{28-12} and V_{29-12}	−30	0	30	mV
R_L	load impedance on the output		10	–	–	kΩ
$\|Z_O\|$	output impedance	note 9	–	tbf	–	Ω
	suppression of line input	dubbing mode; V_{Osel} = 300 mV	–	tbf	–	dB
		deck B in playback; V_{Osel} = 300 mV	–	tbf	–	dB
Source-selector						
I_{bias}	input bias current		–	15	–	nA
S/N	signal-to-noise ratio	note 10; weighted curve 20 Hz to 20 kHz	77	90	–	dB
		weighted curve A(IEC179)	–	96	–	dB
Automatic Level Control (ALC); see Fig.5						
V_{Iref}	input reference voltage for ALC start operation		–	300	–	mV
V_{Oref}	output reference voltage	ALC switched ON; V_{Osel} = 300 mV	1.35	1.5	1.65	V
ΔV	output voltage variation	V_{Osel} = 330 mV				
		ΔV_{Osel} = 10 dB	–	0.2	1	dB
		ΔV_{Osel} = 20 dB	–	1	–	dB
t_l	limiting time	ΔV_{Osel} = 10 dB	–	1	–	ms
t_s	setting time		–	2	–	ms
t_r	release time		–	10	–	s
Erase and bias oscillator						
f_{OSC}	oscillator frequency	note 11	–	80	–	kHz
$I_{O(p-p)}$	maximum output current pins 16 and 18 (peak-to-peak value)		140	–	–	mA
V_{OSC}	output voltage pins 16 to 17 and pins 17 to 18 (peak-to-peak value)	V_P = 18 V	–	–	36	V
V_{15}	voltage control range	note 12	2.0	–	13.0	V
V_{OSC}	peak output voltage	see Fig.6; $V_{control} = V_P - 8$ V between pins 16 and 18	–	8.0	–	V
I_I	input current of control inputs		–	0.1	–	μA
THD	total harmonic distortion between pins 16 and 18	I_O = 80 mA	–	0.5	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltage source						
V_{12}	output voltage	note 13; no external load	7.25	7.5	7.75	V
ΔV_{12}	output voltage deviation	ΔI_{ref} = 1 mA	−100	–	+100	mV
Logics inputs (pins 7 to 10); see Figs 7, 8 and 9						
I_7	signal/mute input current	$V_7 = V_P$	–	–	900	µA
V_7	signal/mute input voltage					
		signal	0	–	0.3	V
		mute	6.0	–	15.0	V
I_8	input current for channel A/B selection	$V_8 = V_P$	–	100	150	µA
	input voltage for channel A/B selection					
		deck A	0	–	3.0	V
		mute	5.0	–	10.0	V
		deck B	12.0	–	15.0	V
I_9	input current for tape selection	$V_9 = V_P$	–	–	900	µA
V_9	input voltage for tape selection					
		Cr02	0	–	0.3	V
		Fe02	6.0	–	15.0	V
I_{10}	input current for mode selection	$V_{10} = V_P$	–	100	150	µA
V_{10}	input voltage for mode selection					
		playback	0	–	4.0	V
		record	6.0	–	9.0	V
		high-speed record	11.0	–	15.0	V

Notes to the characteristics

1. The supply current is measured in the test circuit without an additional load of the 1/2 V_P reference voltage source. In the record mode the tape selector is at position Cr02; the oscillator is OFF.
2. The output impedance of the output buffer is typical Z_O = 1 kΩ.
3. The signal-to-noise ratio is related to an output signal V_O = 150 mV with R_S = 1 kΩ. The circuit is switched at normal speed and the tape selector is at position Cr02.
4. Channel A is switched in the playback mode, at deck B a signal of V_I = 200 µV (f = 315 Hz) is applied. The output voltage at the playback amplifier is not measured selectively (bandwidth = 20 Hz to 20 kHz).
5. Deck B is switched in the record mode, at pins 24 and 26 a signal of I_I = 1 mA (f = 80 kHz) is applied.
6. Line input selected, measured relative to source selector output.
7. Switched in dubbing mode, measured relative to line output.
8. The signal-to-noise ratio is related to an output signal V_O = 1.5 V. The circuit is switched at normal speed.
9. Measured with f = 80 kHz and I_I = 1 mA.
10. The signal-to-noise ratio is related to an output signal V_O = 300 mV.
11. The oscillator frequency is determined by L_L and C_L and may be adjusted between 60 kHz and 120 kHz.
12. For stable oscillator operation the control voltage must be greater than 1 V.
13. The output voltage is independent of the operating mode (playback/record).

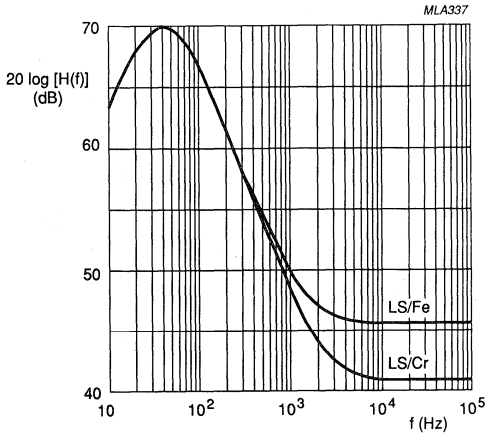


Fig.3 Typical playback frequency response.

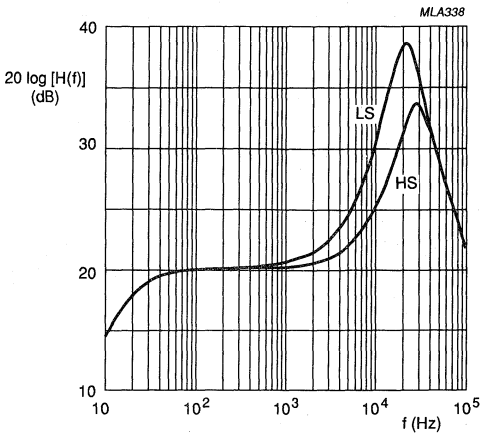


Fig.4 Typical record frequency response.

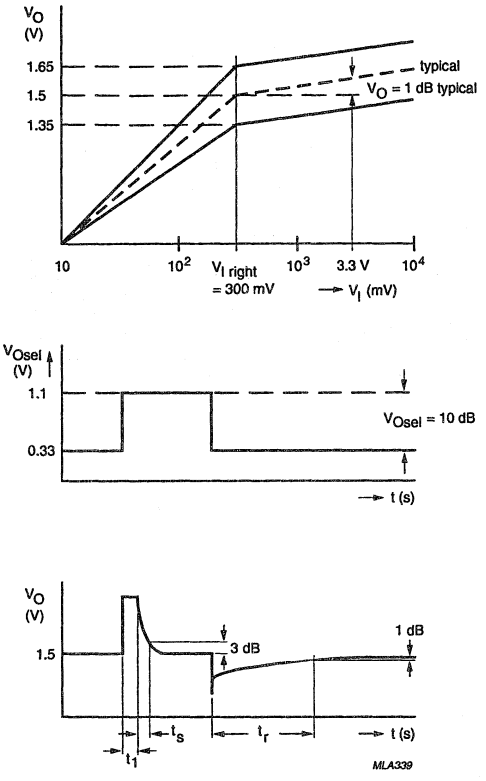


Fig.5 Typical ALC curve.

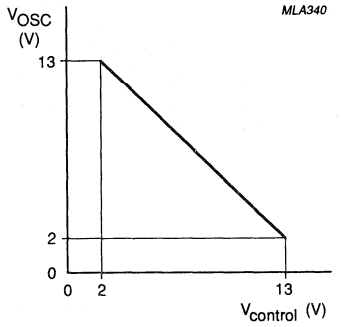


Fig.6 Control voltage/oscillator output voltage (V peak).

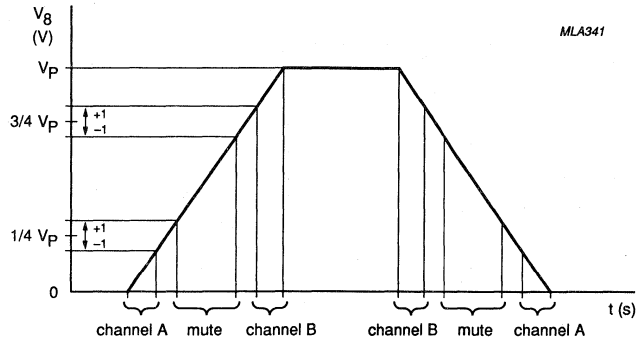
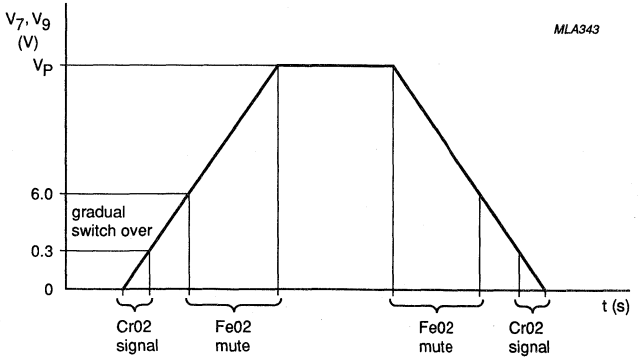


Fig.7 Channel selection input.



Cr02 and Fe02 = pin 9; signal and mute = pin 7

Fig.8 Tape selection input and signal/mute input.

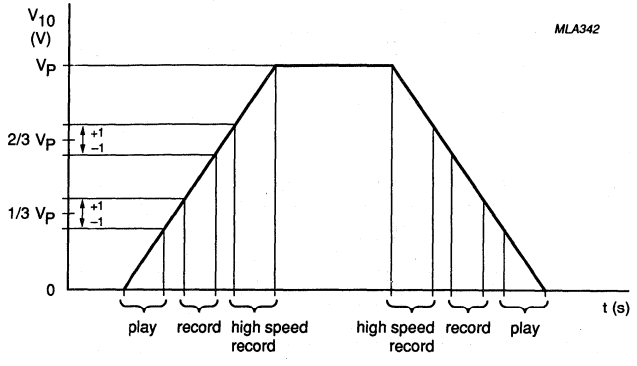


Fig.9 Playback/record/high-speed record selection input.

Table 1 Logic DDPR (S/M input not included)

LOGIC INPUTS A/B	LOGIC INPUTS Fe/CrA	CHANNEL SELECT	R/P SWITCH	HS SWITCH	Fe/Cr PB	PB AMP.	DUB. SWITCH	REC. AMP.	ALC OP.	BIAS OSC.
Playback										
A	Fe	A	P	ON	Fe	ON	mute	OFF	OFF	OFF
A	Cr	A	P	ON	Cr	ON	mute	OFF	OFF	OFF
B	Fe	B	P	ON	Fe	ON	mute	OFF	OFF	OFF
B	Cr	B	P	ON	Cr	ON	mute	OFF	OFF	OFF
Record										
A	Fe	A	R	ON	Fe	ON	dubbing	ON	OFF	ON
A	Cr	A	R	ON	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON
High speed record										
A	Fe	AHS	R	OFF	Fe	ON	dubbing	ON	OFF	ON
A	Cr	AHS	R	OFF	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON

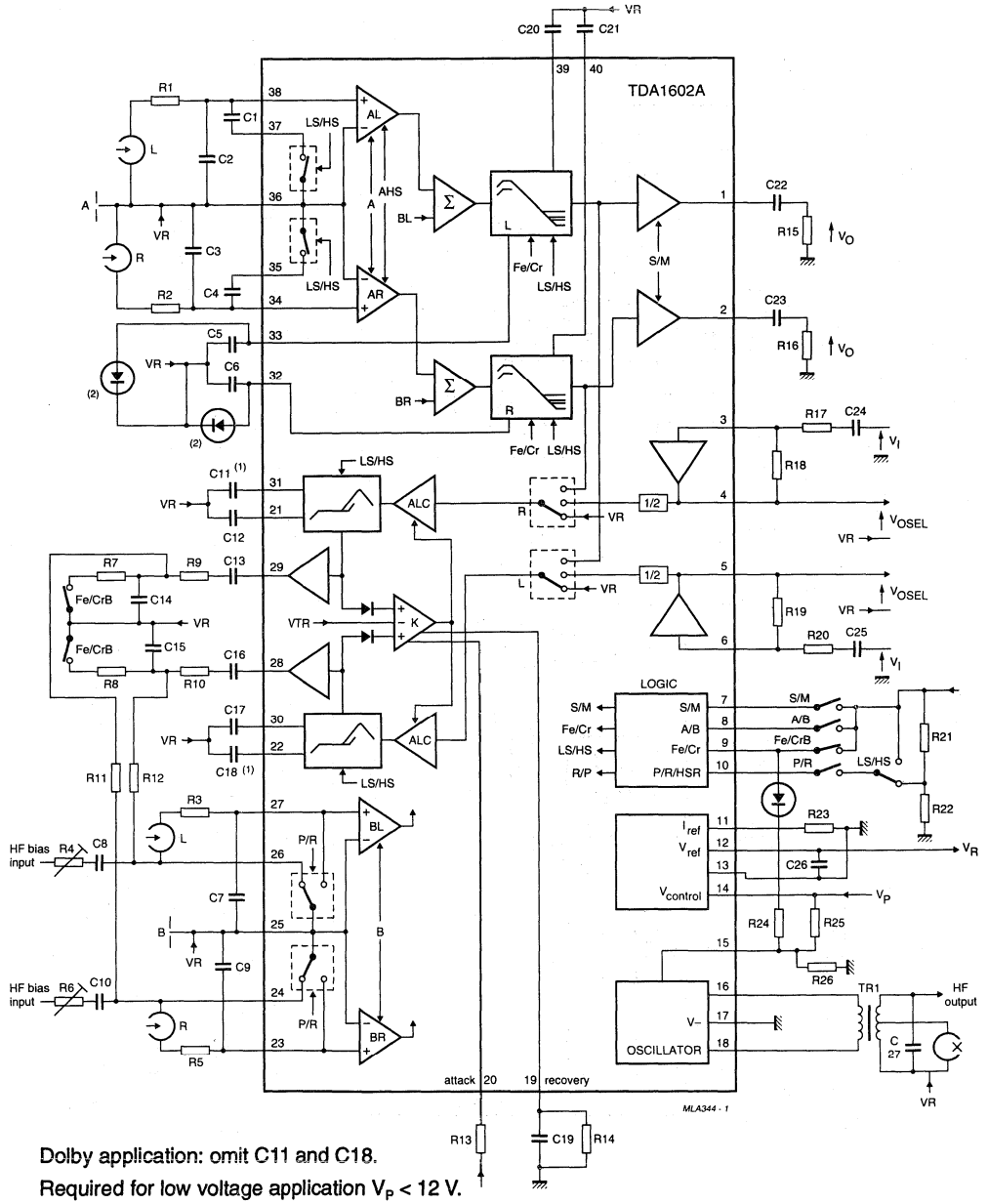
Table 2 Double deck application

DECK SELECT A(P)	DECK SELECT B(R/P)	A/B INPUT	S/M INPUT	CHANNEL SELECT	HS SWITCH	PB AMP.	DUB. SWITCH	ALC OP.
Playback								
$\overline{A}$	$\overline{B}$	don't care	M	A or B	OFF	OFF	mute	OFF
$\overline{A}$	B	B	S	B	OFF	ON	mute	OFF
A	$\overline{B}$	A	S	A	OFF	ON	mute	OFF
Record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	S	A	OFF	ON	dubbing	OFF
High speed record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	M (1)	AHS	ON	OFF (1)	dubbing	OFF

Notes to Table 2

1. Fe/Cr selection not included.
2. S is also possible; play buffer = ON.

APPLICATION INFORMATION



(1) Dolby application: omit C11 and C18.

(2) Required for low voltage application $V_P < 12$ V.

Fig.10 Application diagram.

TEST INFORMATION

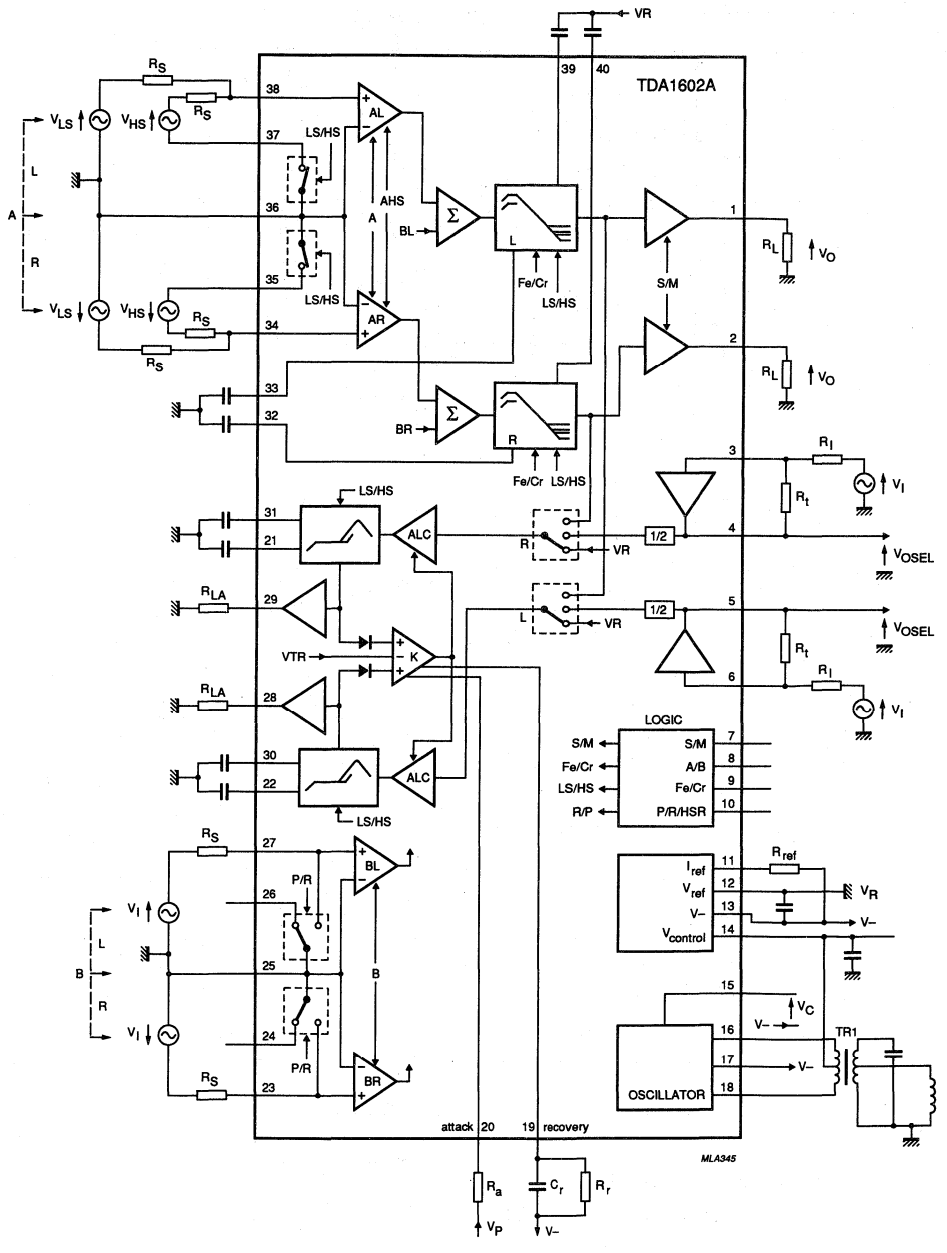


Fig.11 Test circuit diagram.

Table 3 Component values used in the application diagram

COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R1, R2		47	Ω
R3, R5		47	Ω
R4, R6	potentiometer	47	kΩ
R7, R8		tbf	
R9, R10		6.8	kΩ
R11, R12		8.2	kΩ
R13		100	Ω
R14		1	MΩ
R15, R16		100	kΩ
R17, R20		tbf	
R18, R19		tbf	
R21, R22		10	kΩ
R23		2	kΩ
R24, R25, R26		5.1	kΩ
Capacitors			
C1, C4		330	pF
C2, C3		330	pF
C5, C6		47	nF
C7, C9		680	pF
C8, C10		820	pF
C11, C18		68	nF
C12, C17		100	µF
C13, C16		4.7	µF
C14, C15		tbf	
C19		47	µF
C20, C21		100	nF
C22, C23		4.7	µF
C24, C25		4.7	µF
C26		100	µF
C27		3.9	nF

Table 4 Component values used in the test circuit

COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R_S		1	kΩ
R_L		100	kΩ
R_{LA}		10	kΩ
R_I		4.7	kΩ
R_t		22.6	kΩ
R_{ref}		2	kΩ
R_a		1	kΩ
R_r		3.3	MΩ
Capacitors			
C_r		1	μF

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
Repetitive peak output current	I_{ORM}	< 1,5	A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ. 5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ. 0,3	%
Input impedance	$\|Z_i\|$	typ. 45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ. 25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ. 55	mV
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

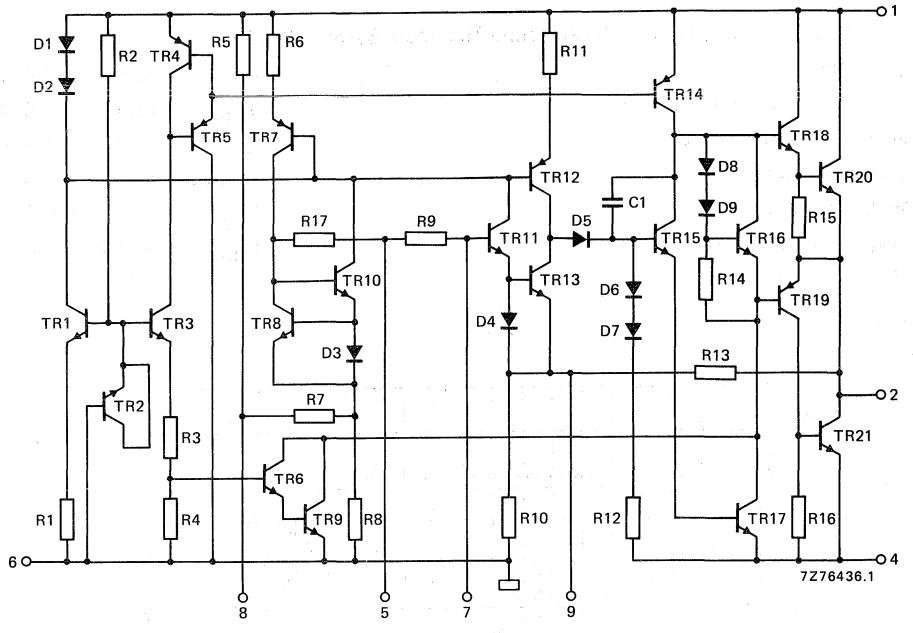


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

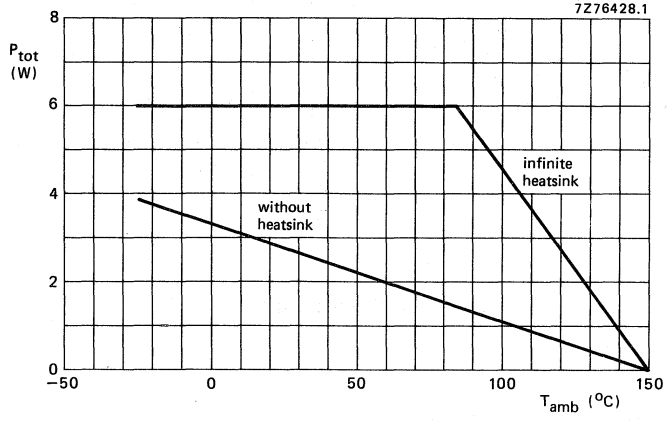


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2{,}2} = 41\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

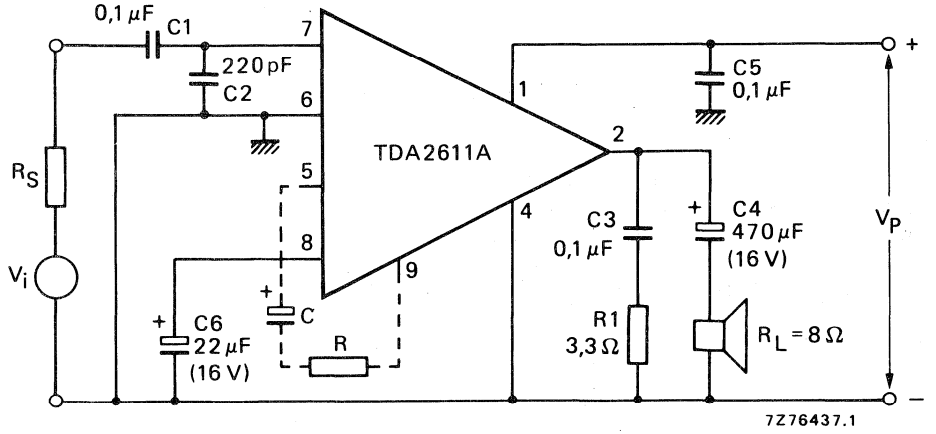


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

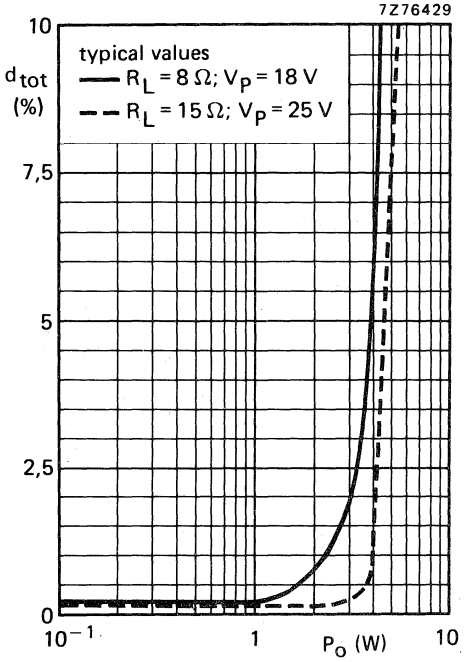


Fig. 4 Total harmonic distortion as a function of output power.

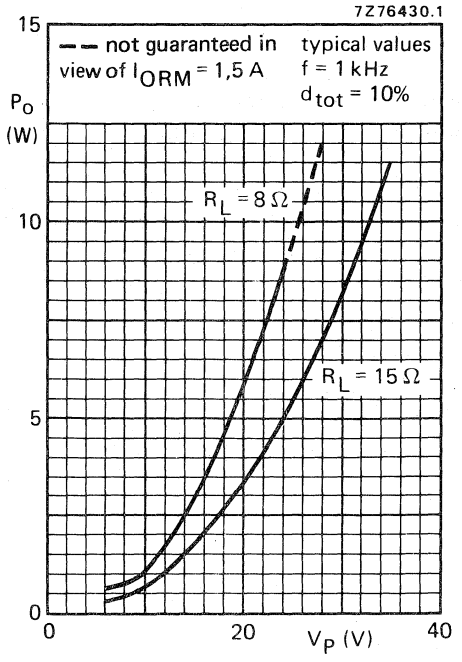


Fig. 5 Output power as a function of supply voltage.

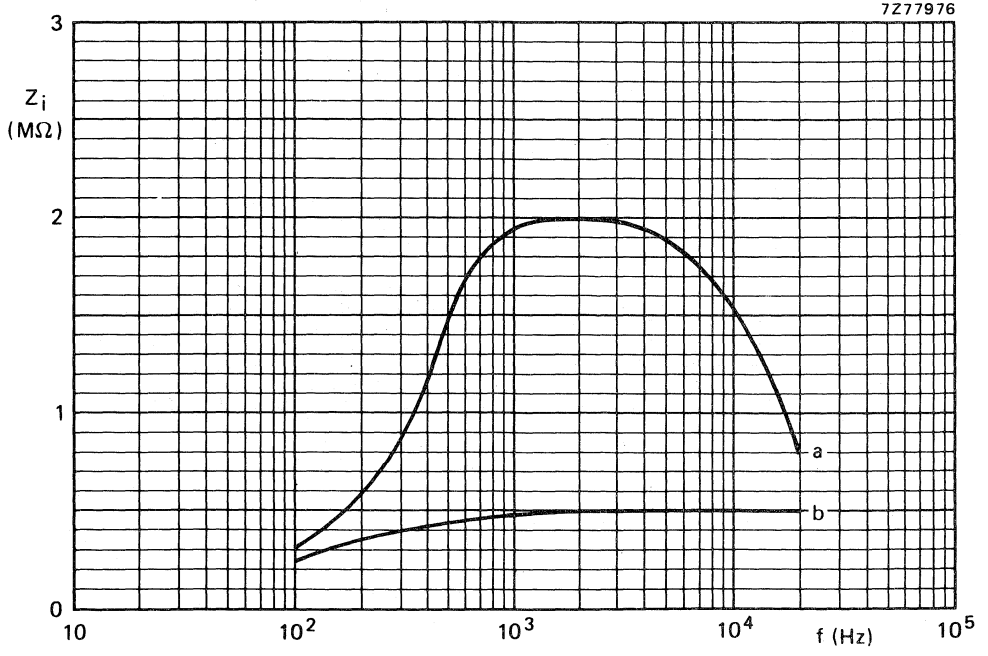


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

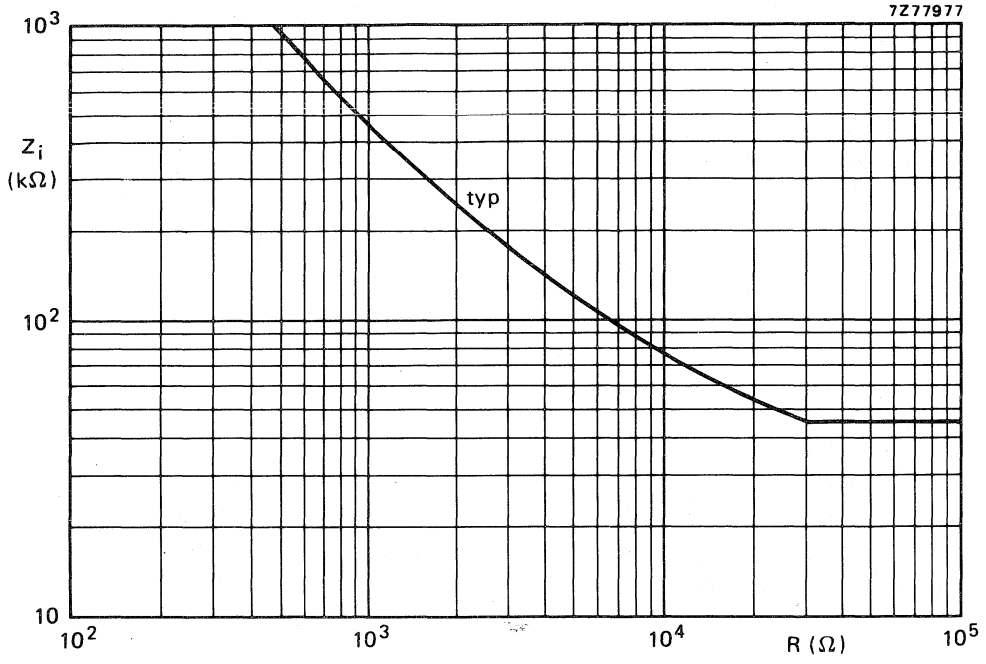


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

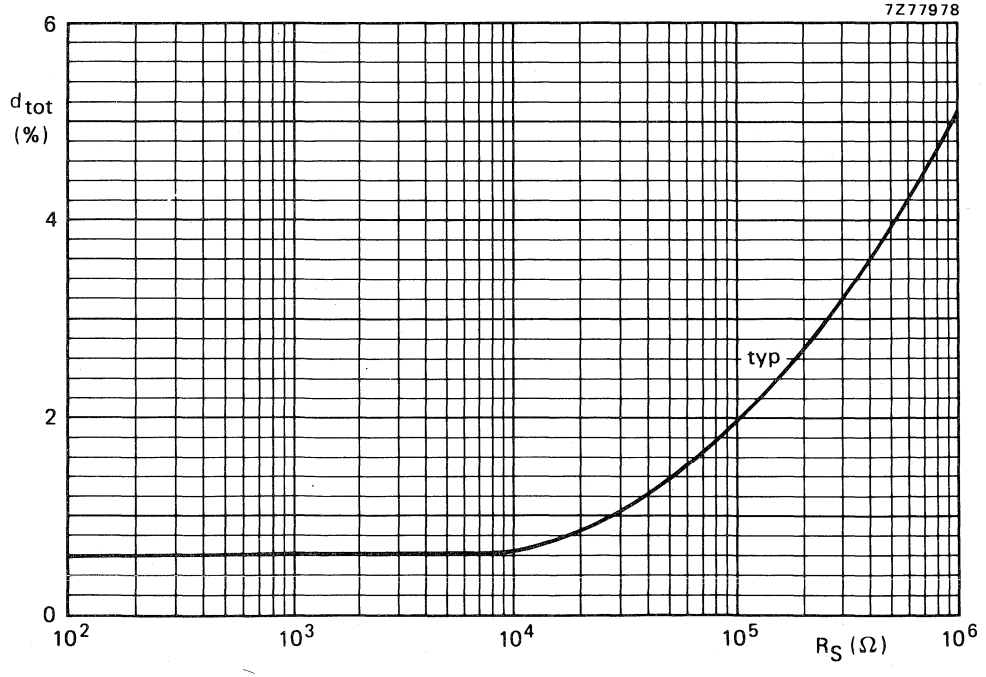


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

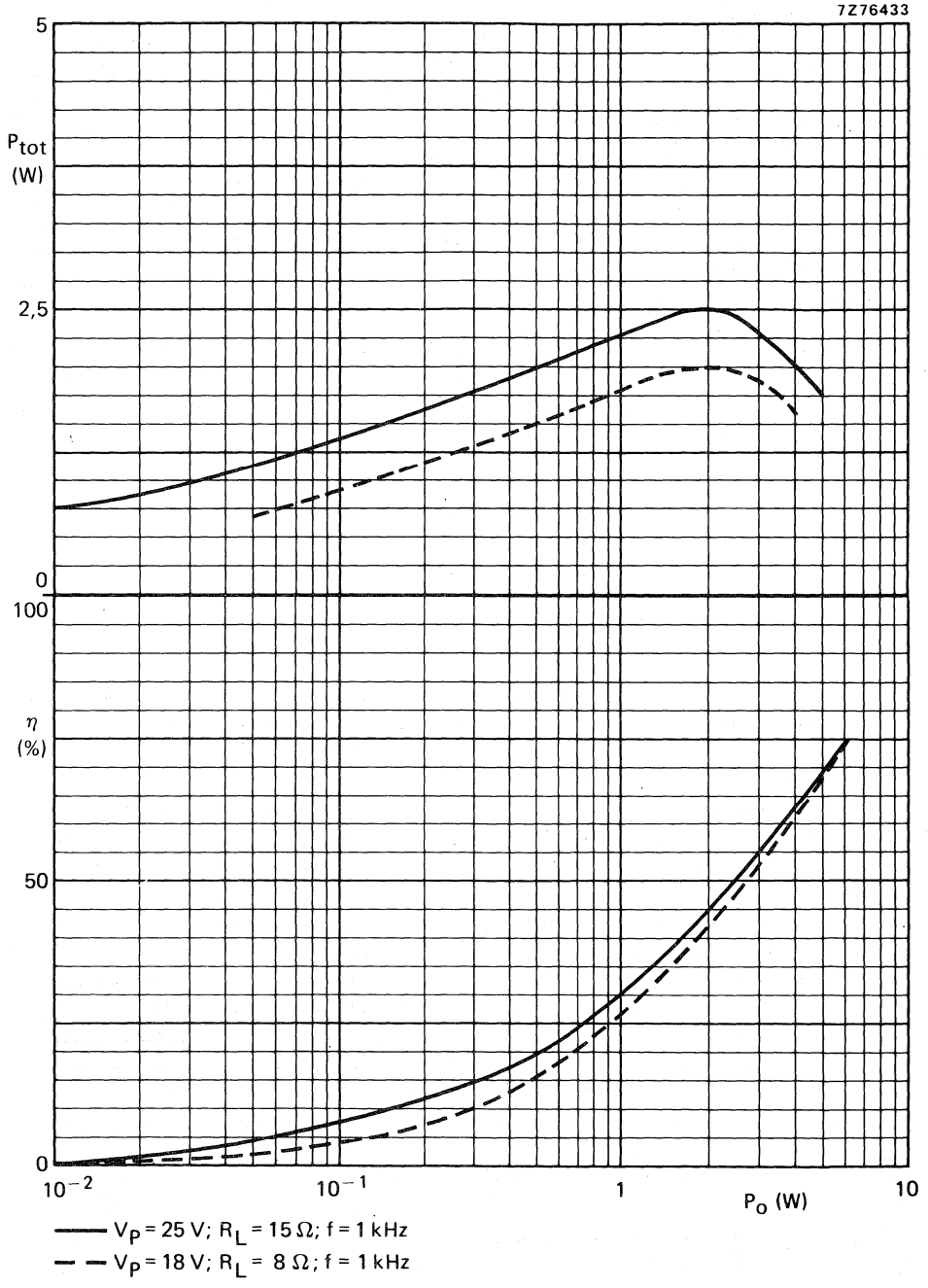


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

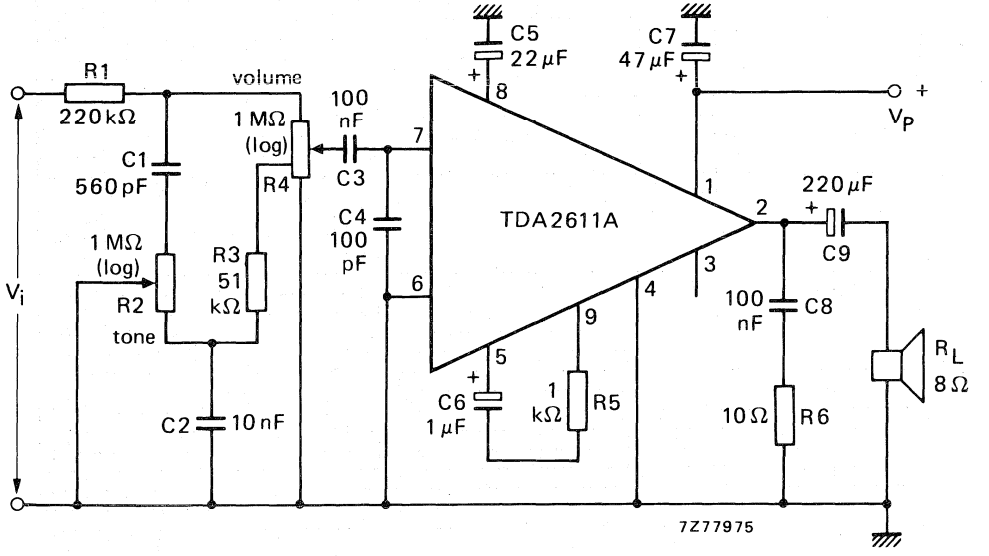


Fig. 10 Ceramic pickup amplifier circuit.

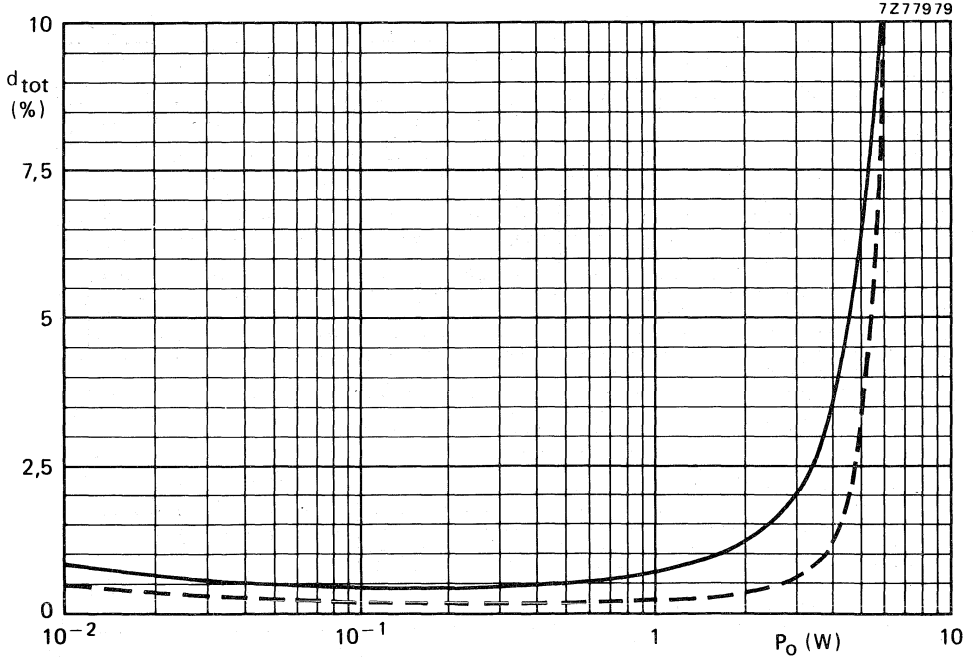


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

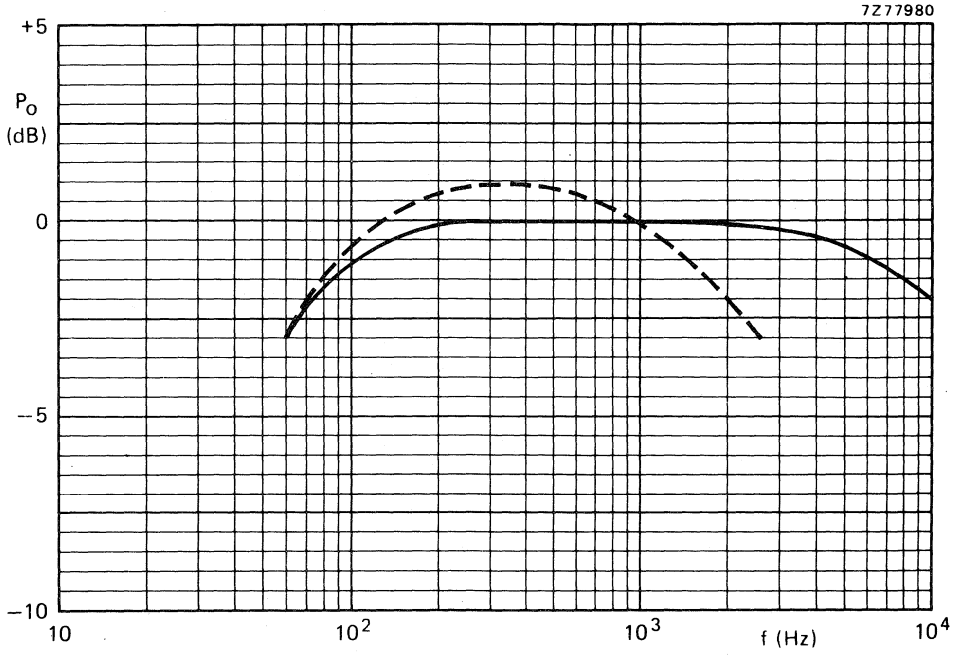


Fig. 12 Frequency characteristics of the circit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

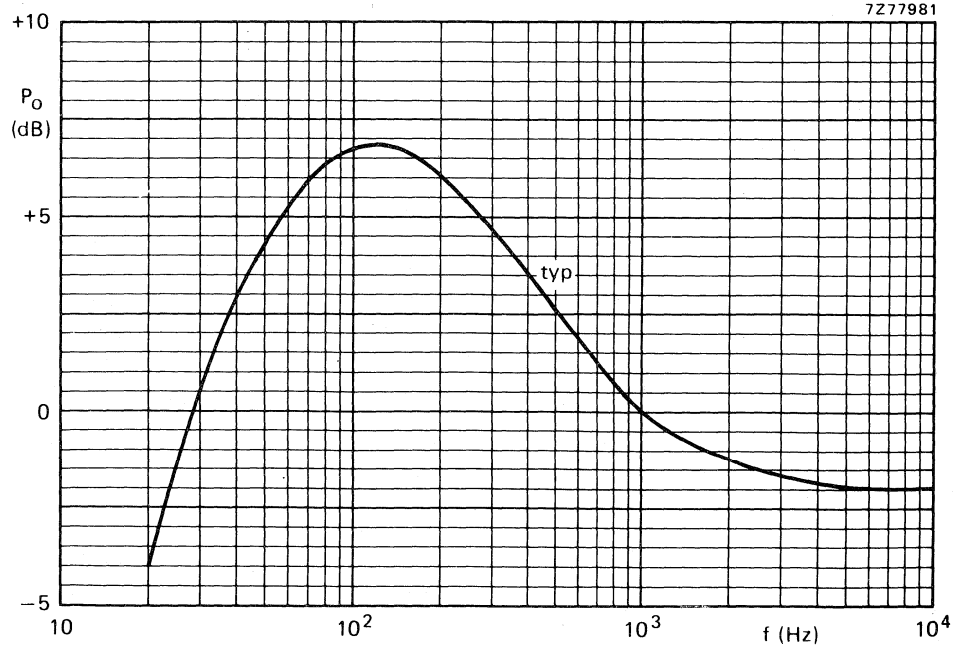


Fig. 13 Frequency characteristic of the circit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

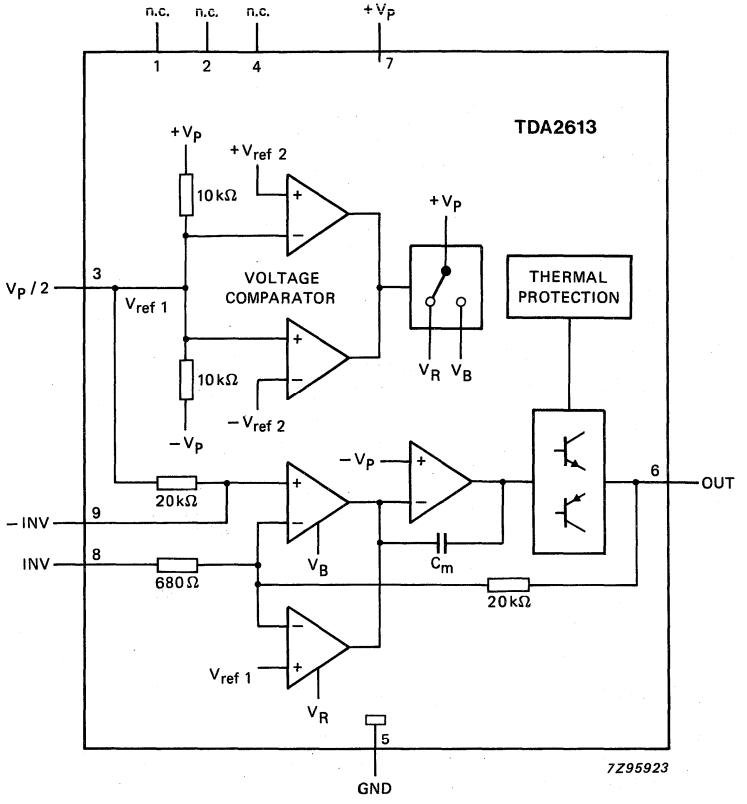


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected	5.	GND	ground (asymmetrical) / negative supply (symmetrical)
2.	n.c.	not connected	6.	OUT	output
3.	VP/2	½ VP (asymmetrical) / ground (symmetrical)	7.	+VP	positive supply
4.	n.c.	not connected	8.	INV	inverting input
			9.	−INV	non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	40	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) ⩾ 4 Ω, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to V_P = ± 20 V.

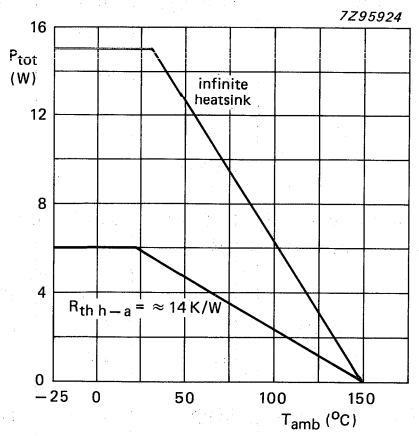


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case

$R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	40	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	35	44	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	2,0	2,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,5	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2\ k\Omega$	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ –3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

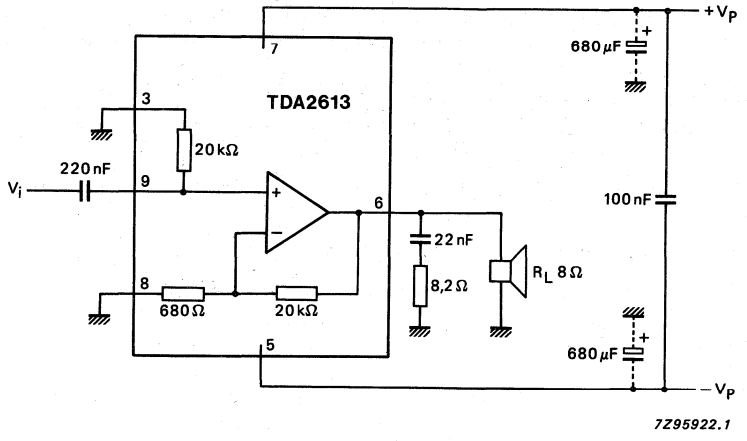


Fig. 3 Test and application circuit; symmetrical power supply.

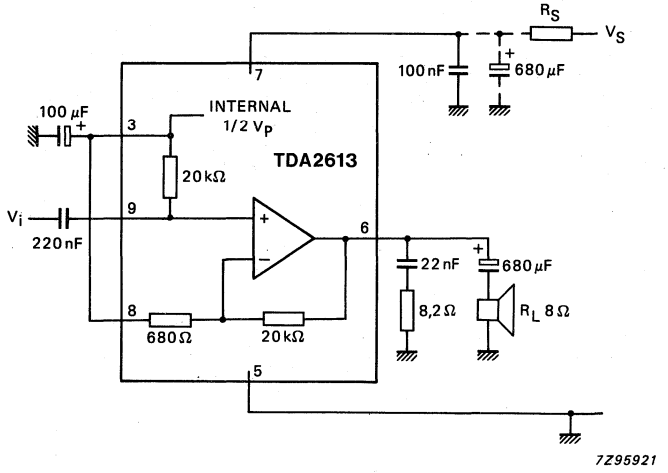


Fig. 4 Test and application circuit; asymmetrical power supply.

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

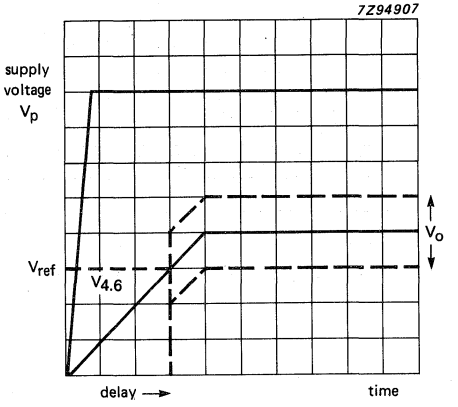


Fig. 5 Input mute circuit; time delay.

6 W hi-fi audio power amplifier TDA2614

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2614 is a power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as TV and radio.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		15	–	42	V
P_O	output power	V_S = 24 V; THD = 0.5%	–	6.5	–	W
G_v	internal voltage gain		–	30	–	dB
SVRR	supply voltage ripple rejection		–	45	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2614	9	SIL	plastic	SOT110

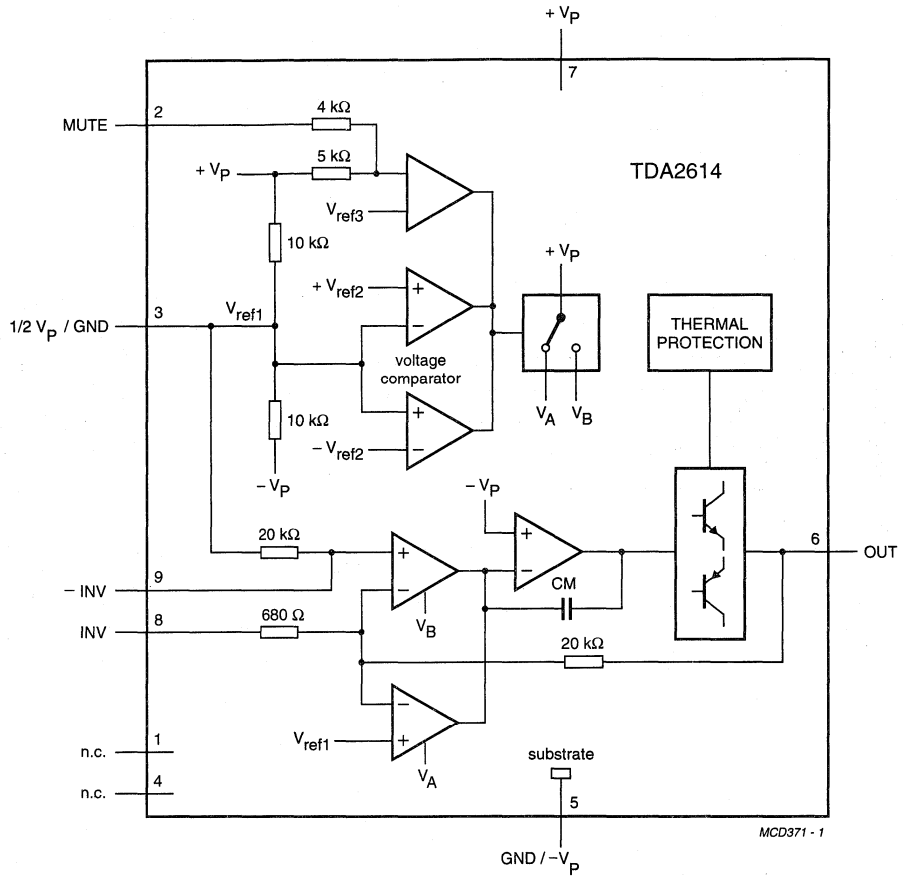


Fig.1 Block diagram.

6 W hi-fi audio power amplifier TDA2614

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply (or ground at symmetrical power supplies)
n.c.	4	not connected
GND/–V_P	5	ground (or negative supply rail at symmetrical power supplies)
OUT	6	output
V_P	7	supply voltage
INV	8	inverting input
–INV	9	non-inverting input

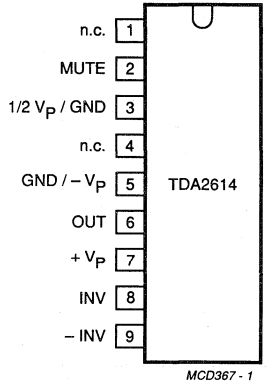


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2614 is a hi-fi power amplifier designed for mains fed applications, such as radio and TV. The circuit is optimally designed for asymmetrical power supplies, but is also well-suited to symmetrical power supply systems.

An output power of 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a supply of 24 V. The gain is internally fixed at 30 dB, thus offering a low gain spread.

A special feature is the input mute circuit. This circuit disconnects the non-inverting input when the supply voltage drops below 10 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the input, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of 150 °C, so a crystal operating temperature of max. 150 °C can be used without extra distortion.

With the derating value of 8 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = 24 V, dissipation is 4.1 W.

With a maximum ambient temperature of 60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{4.1} - 8 = 14 \text{ K/W}.$$

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	42	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	+150	°C
t_{sc}	short circuit time	short circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V, and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies, the circuit is short-circuit-proof up to V_P = ±21 V.

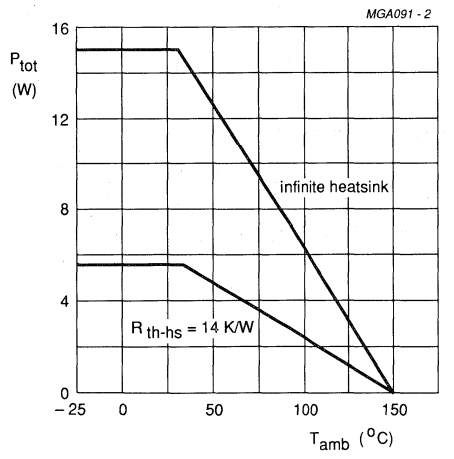


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range		–	24	42	V
I_{ORM}	repetitive peak output current		–	–	2.2	A
Operating position; note 1						
V_P	supply voltage range		15	24	42	V
I_P	total quiescent current		10	20	35	mA
P_O	output power					
		THD = 0.5%	5	6.5	–	W
		THD = 10%	6.5	8.5	–	W
		THD = 0.5%; R_L = 4 Ω	–	10	–	W
		THD = 10%; R_L = 4 Ω	–	14	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	30 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	30	200	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	35	45	–	dB
I_{bias}	input bias current		–	0.3	–	μA
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
$Z_{2\text{-}7}$	mute input impedance		–	9	–	kΩ
I_P	total quiescent current		10	20	35	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	40	200	mV
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
V_P	positive supply voltage range		4	–	10	V
I_P	total quiescent current	$R_L = \delta$	5	15	20	mA
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{3\text{-}6}\rvert$	DC output offset voltage		–	40	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating position; note 6						
$\pm V_P$	supply voltage range		7.5	12	21	V
I_P	total quiescent current		10	20	35	mA
P_O	output power					
		THD = 0.5%	5	6.5	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_o = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
V_{no}	noise output voltage	note 3	–	70	140	µV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		40	55	–	dB
I_{bias}	input bias current		–	0.3	–	µA
$\lvert V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ µA)						
V_O	output voltage	V_I = 600 mV	–	0.1	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current	$R_L = \infty$	10	20	35	mA
V_{no}	noise output voltage	note 3	–	70	140	µV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes to the characteristics

1. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 µA. See Fig.5
2. The power bandwidth is measured at an output power of $P_{O\,max}$ – 3 dB.
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz, at a ripple voltage of 200 mV. With symmetrical power supplies, the ripple (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz.
5. V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply. See Fig.5
6. $\pm V_P$ = 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} < 30 µA. See Fig.4

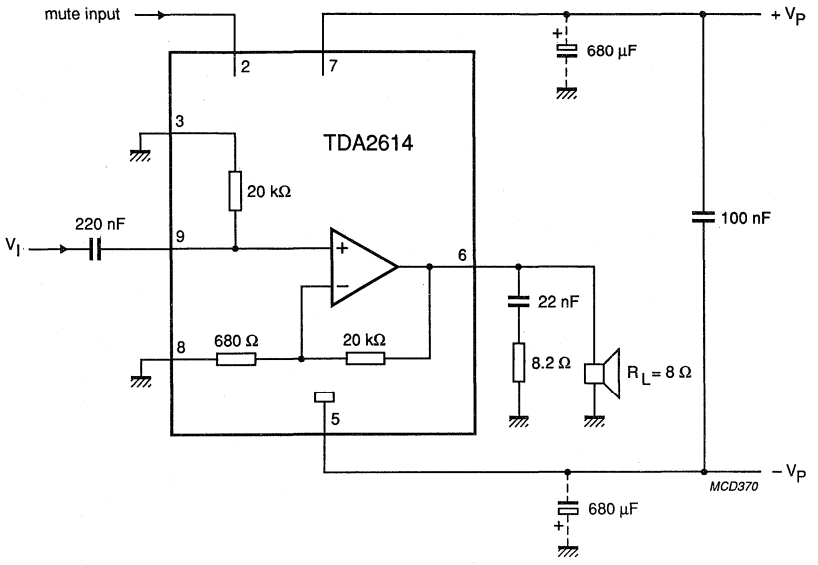


Fig.4 Test and application circuit with symmetrical power supply.

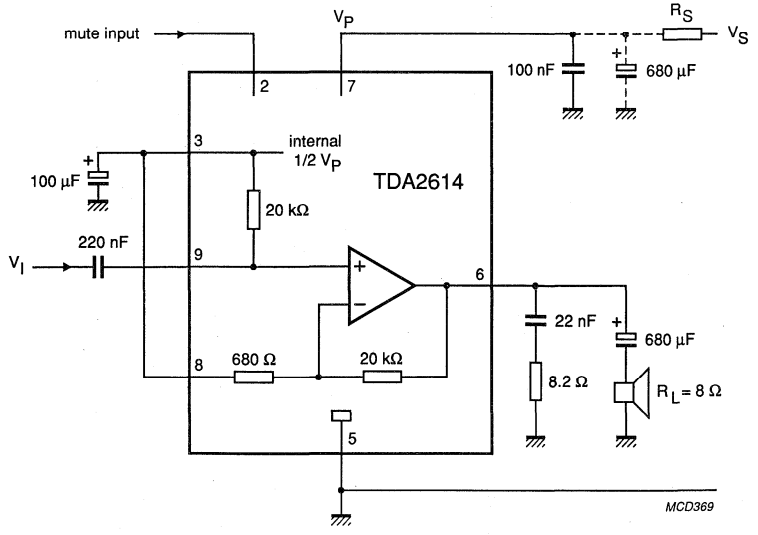


Fig.5 Test and application circuit with asymmetrical power supply.

2 x 6 W hi-fi audio power amplifier TDA2615

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	positive supply voltage range		7.5	–	21	V
P_O	output power	$V_S = \pm 12$ V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2615	9	SIL	plastic	SOT110

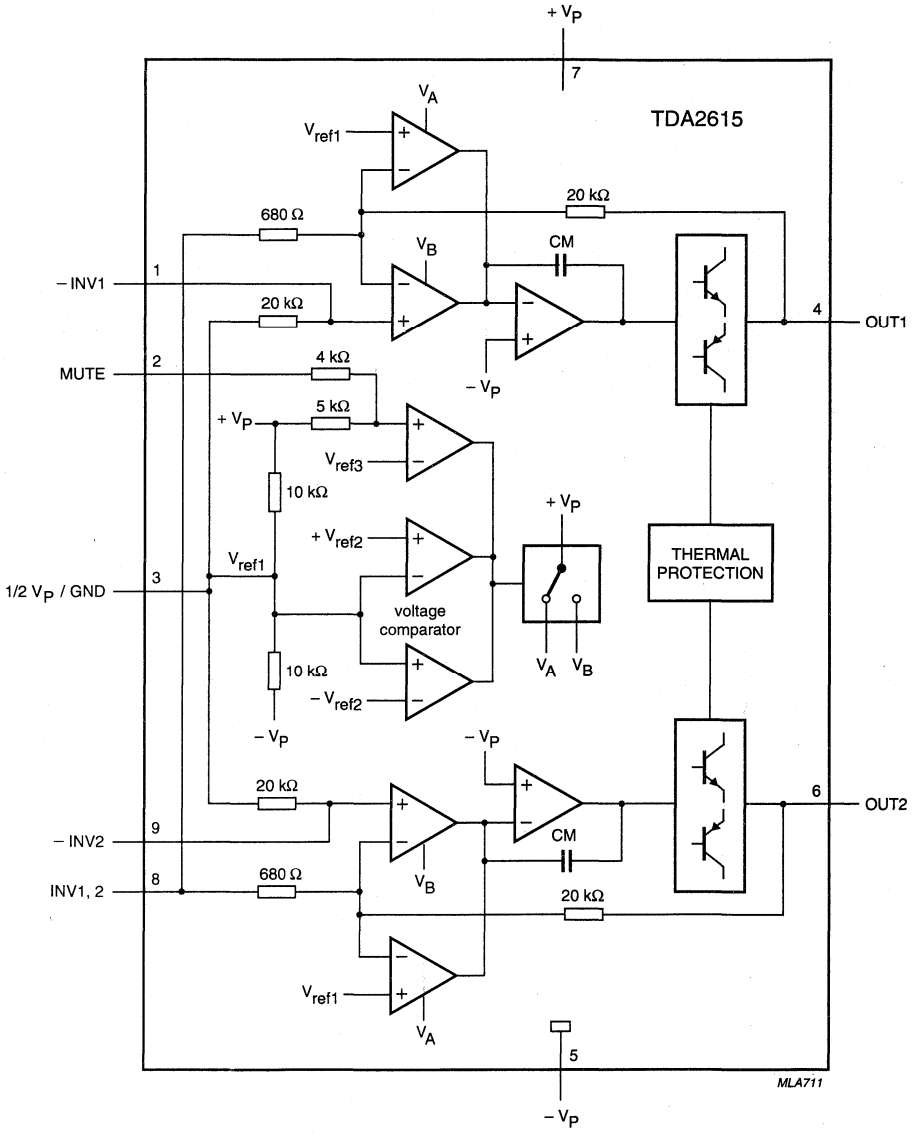


Fig.1 Block diagram.

2 x 6 W hi-fi audio power amplifier TDA2615

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
V_P	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

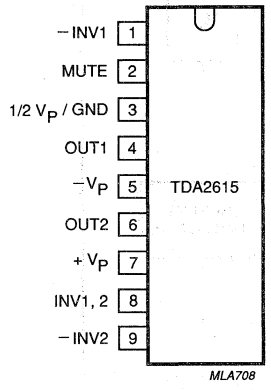


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2615 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and stereo TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±12 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 6 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = ±12 V, the measured maximum dissipation is 7.8 W.

With a maximum ambient temperature of +60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{7.8} - 6 = 5.5 \text{ K/W}.$$

The metal tab has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	+150	°C
t_{sc}	short-circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symetrical power supplies the circuit is short-circuit-proof up to V_P = 21 V

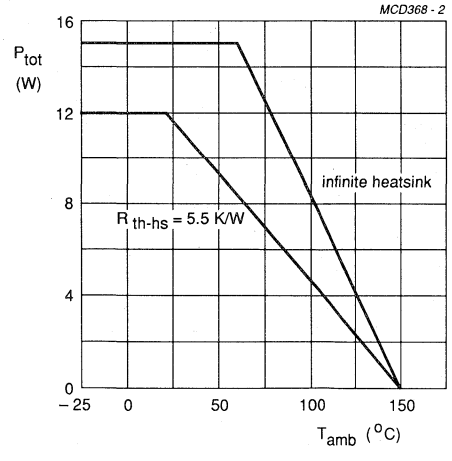


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	6 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	12	21	V
I_{ORM}	repetitive peak output current		–	–	2.2	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	12	21	V
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α	channel separation	$R_S = 0$	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert\Delta V_{GND}\rvert$	DC output offset voltage		–	40	200	mV
Operating position; note 6						
I_P	total quiescent current		18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 1	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v\rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes to the characteristics

1. $V_P = \pm 12$ V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} = < 30 μA. See Fig.4
2. The power bandwidth is measured at an output power of $P_{O\ max}$ –3 dB.
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz.
5. $\pm V_P$ = 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply. See Fig.4
6. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5

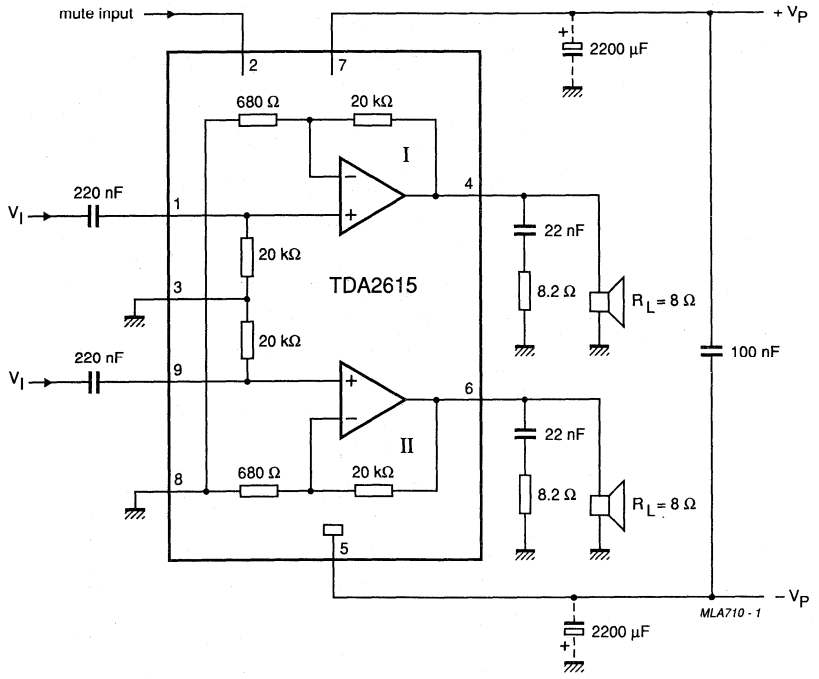


Fig.4 Test and application circuit with symmetrical power supply.

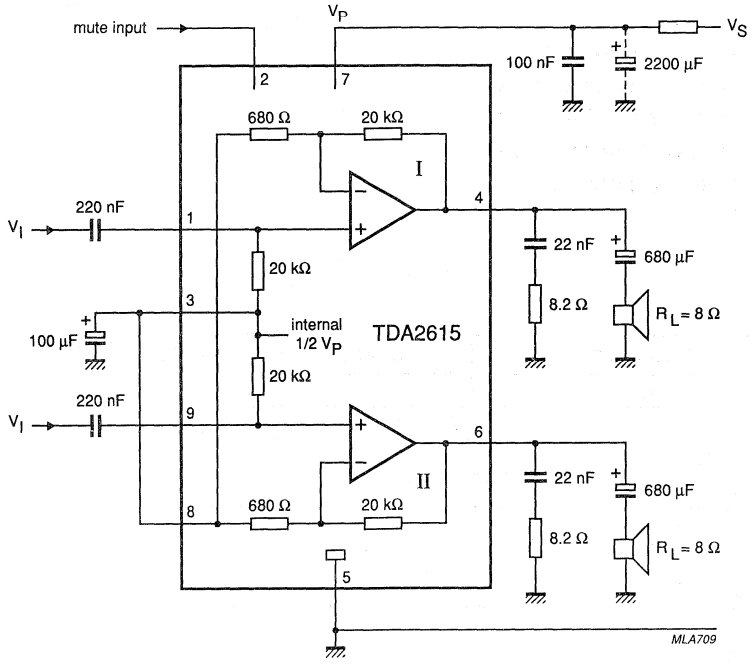


Fig.5 Test and application circuit with asymmetrical power supply.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_P = \pm 16$ V; THD = 0.5%	–	12	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157

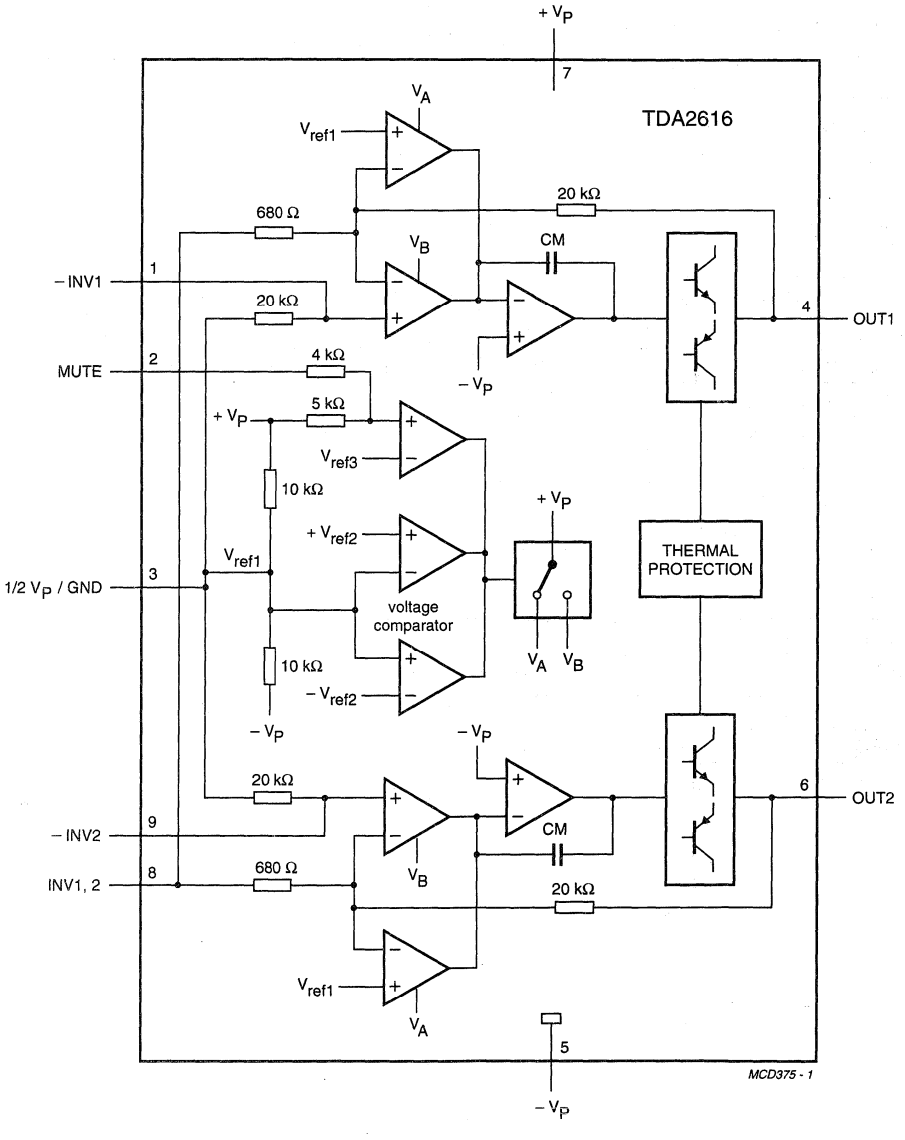


Fig.1 Block diagram.

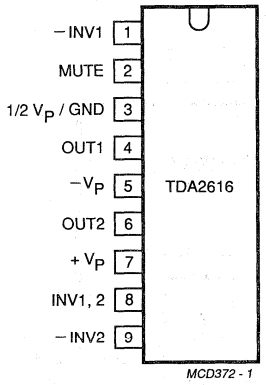


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
$+V_P$	7	supply voltage (positive)
INV1, 2	8	inverting inputs 1 and 2
−INV2	9	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA2616 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 12 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±16 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 µA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 2.5 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14.6 W.

With a maximum ambient temperature of +65 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 65}{14.6} - 2.5 = 3.3 \text{ K/W}.$$

The internal metal block has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	25	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	150	°C
t_{sc}	short circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies the circuit is short-circuit-proof up to V_P = ±21 V.

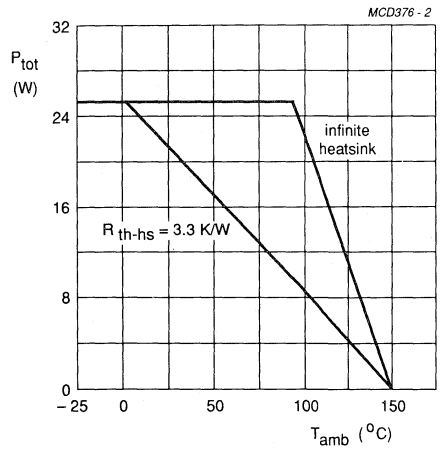


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	2.5 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	16	21	V
I_{ORM}	repetitive peak output current		–	–	2.2	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	16	21	V
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power					
		THD = 0.5%	10	12	–	W
		THD = 10%	12	15	–	W
THD	total harmonic distortion	P_O = 6 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α	channel separation	R_S = 0	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert\Delta V_{GND}\rvert$	DC output offset voltage		–	40	200	mV
Operating position; note 6						
I_P	total quiescent current		18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
		THD = 0.5%; R_L = 4 Ω	–	10	–	W
		THD = 10%; R_L = 4 Ω	–	14	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v\rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
I_P	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA

Notes to the characteristics

1. V_P = ±16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} < 30 μA. See Fig.4
2. The power bandwidth is measured at an output power of $P_{O\,max}$ – 3 dB
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz)
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz
5. ±V_P = 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply. See Fig.4
6. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5

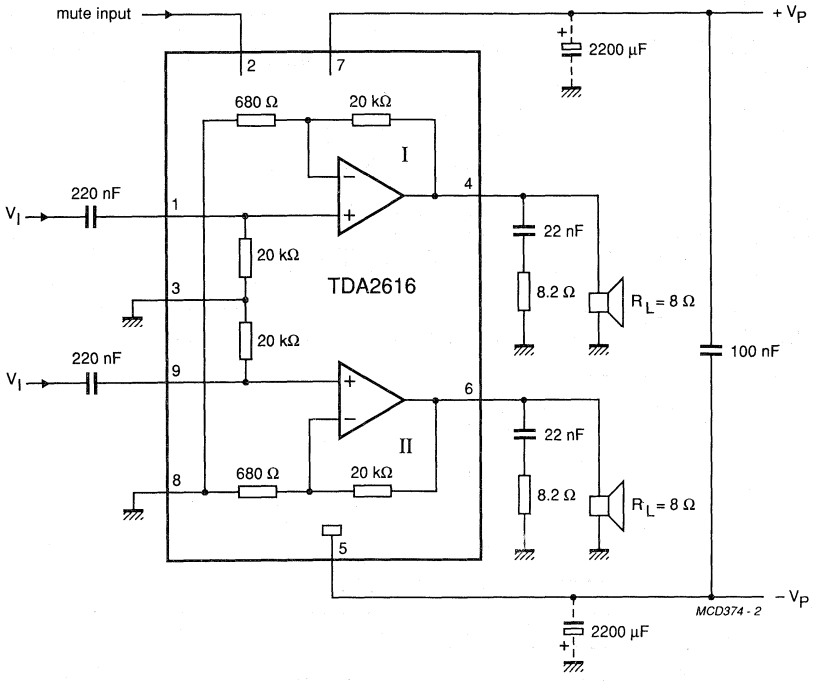


Fig.4 Test and application circuit with symmetrical power supply.

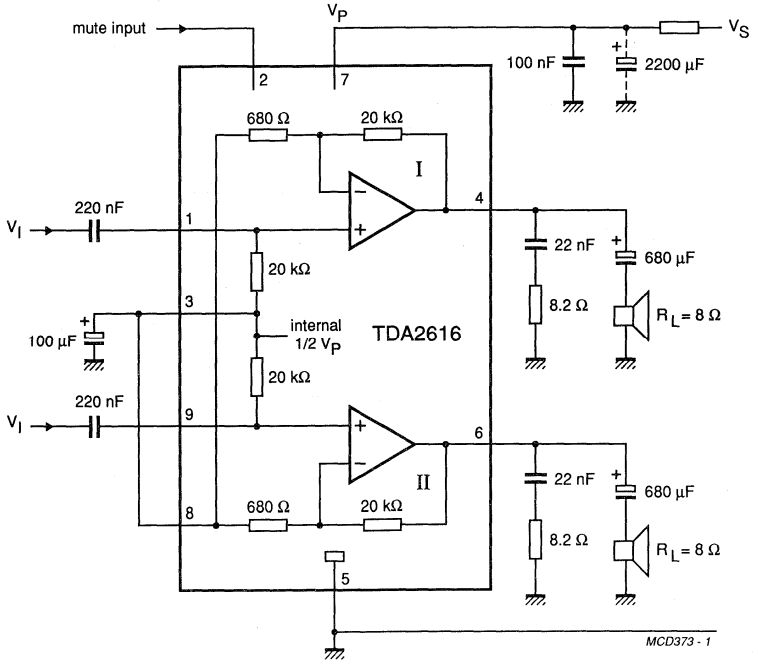


Fig.5 Test and application circuit with asymmetrical power supply.

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$	0,03 to	200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

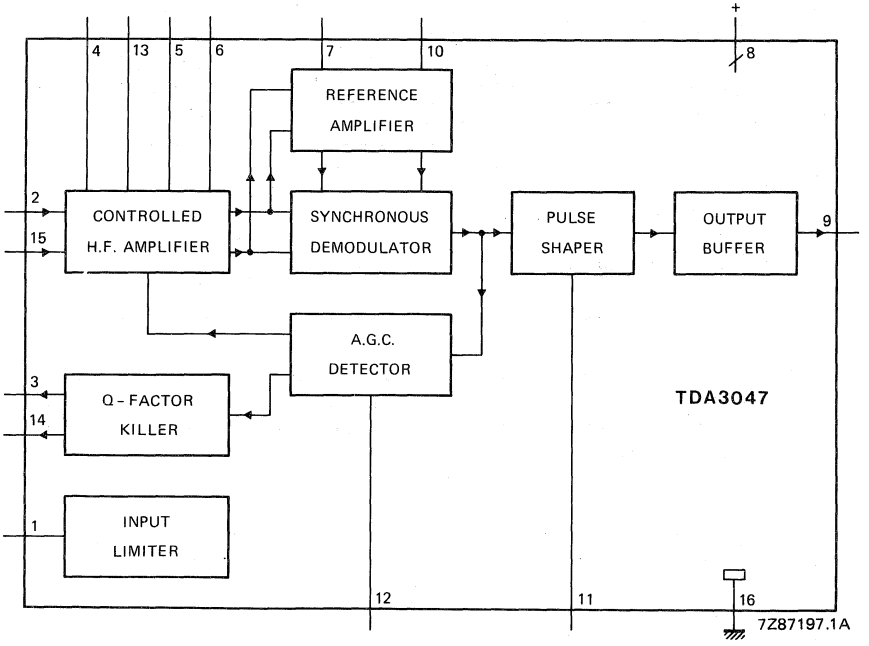


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at $V_{9-16} = 4{,}5$ V	$-I_9$	75	120	–	μA
at $V_{9-16} = 3{,}0$ V	$-I_9$	75	130	–	μA
at $V_{9-16} = 1{,}0$ V	$-I_9$	75	140	–	μA
Output current; output voltage *low*					
at $V_{9-16} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

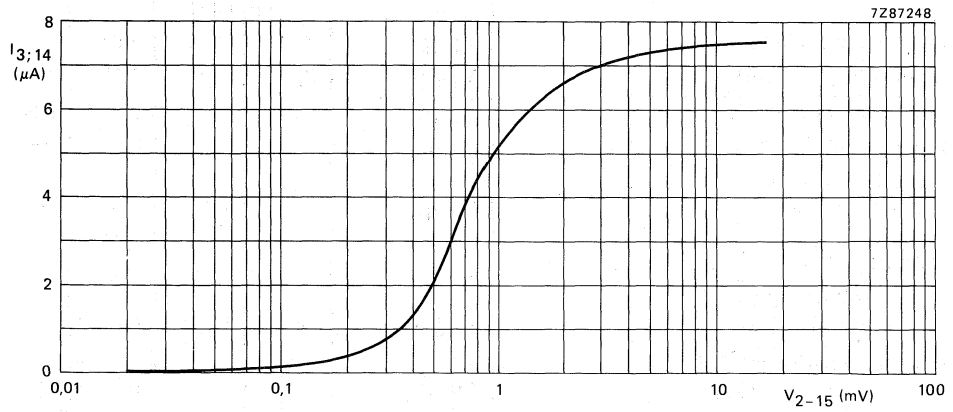
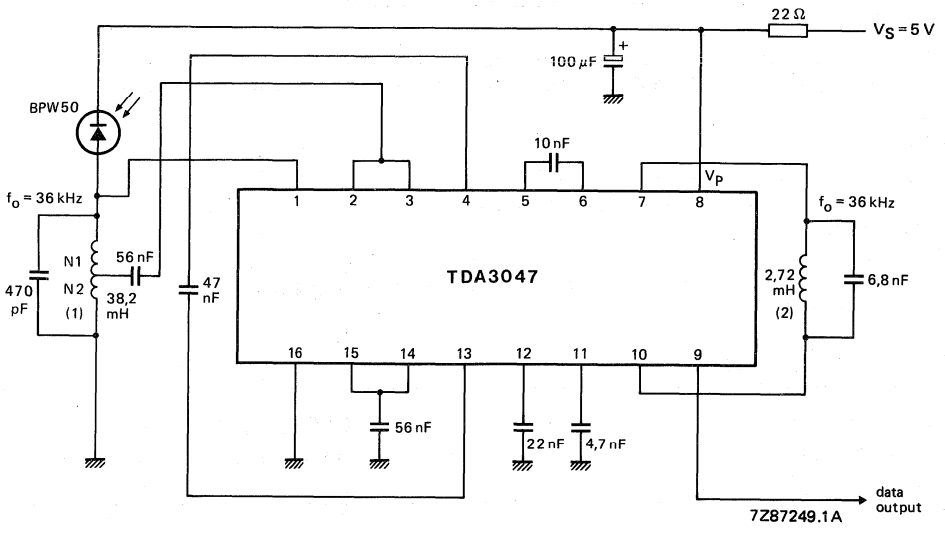


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

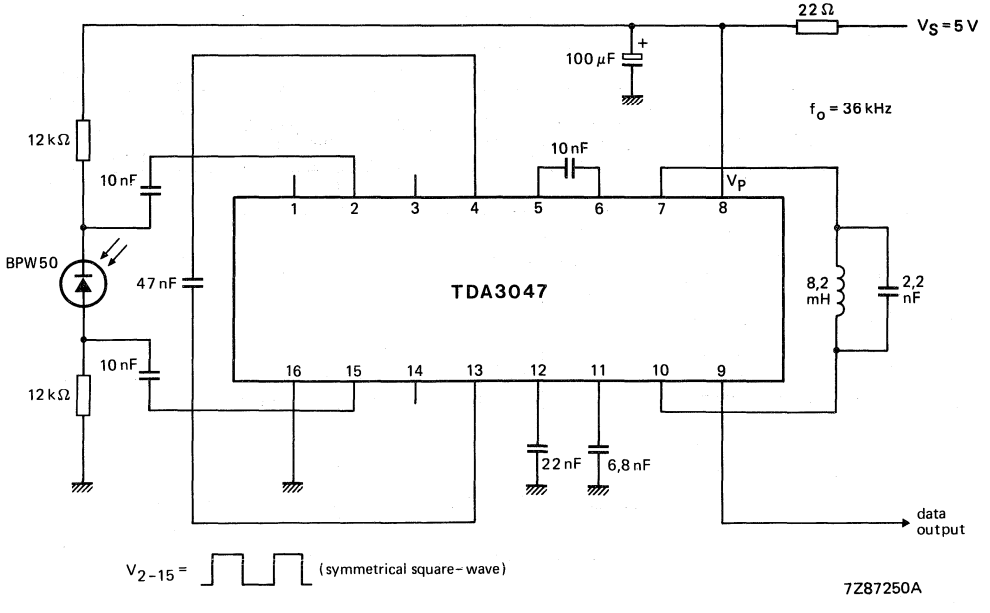


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

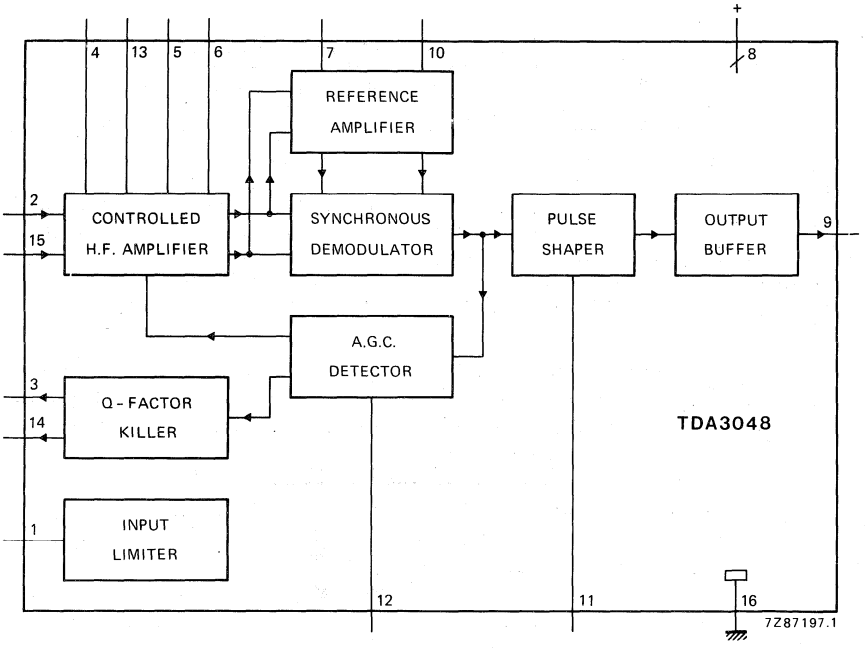


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2	V
Output current pulse shaper (pin 11)	I_{11}	max.	10	mA
Voltages between pins*				
pins 2 and 15	V_{2-15}	max.	4,5	V
pins 4 and 13	V_{4-13}	max.	4,5	V
pins 5 and 6	V_{5-6}	max.	4,5	V
pins 7 and 10	V_{7-10}	max.	4,5	V
pins 9 and 11	V_{9-11}	max.	4,5	V
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 125	°C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9$ = 75 μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at I_9 = 75 μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8}$ = 4,5 V	I_9	75	120	–	μA
$-V_{9-8}$ = 3,0 V	I_9	75	130	–	μA
$-V_{9-8}$ = 1,0 V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8}$ = 0,5 V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; I_9 = 75 μA.
2. Voltage pin 9 remains *high.*
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at V_{12-16} = 2 V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at V_{12-16} = 2 V	$-I_{14}$	2,5	7,5	20	μA

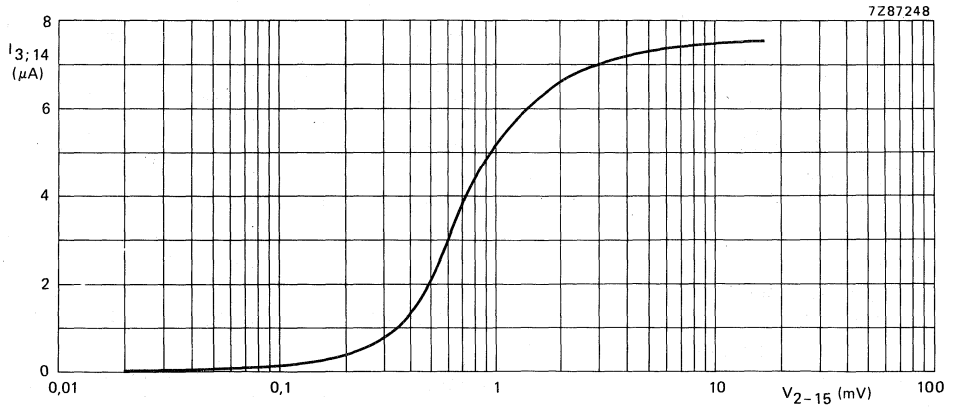
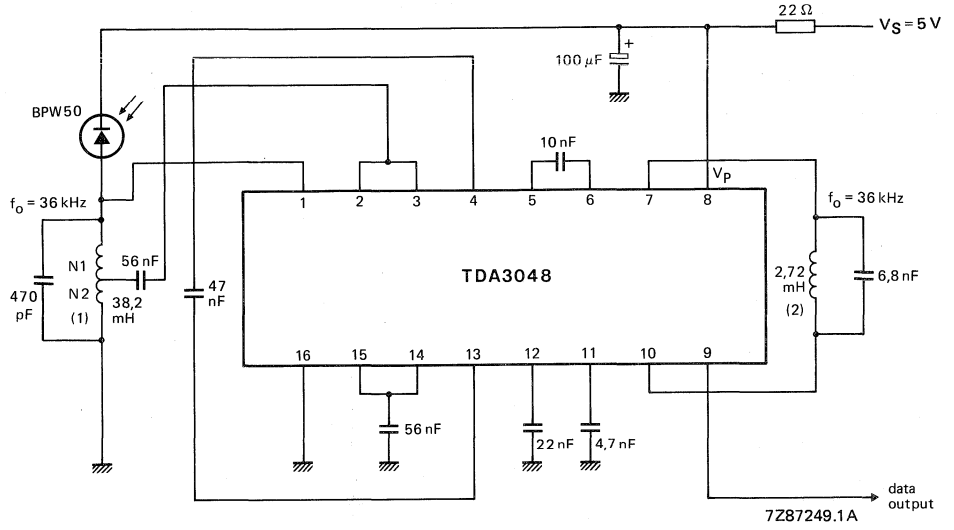


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; V_P = 5 V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

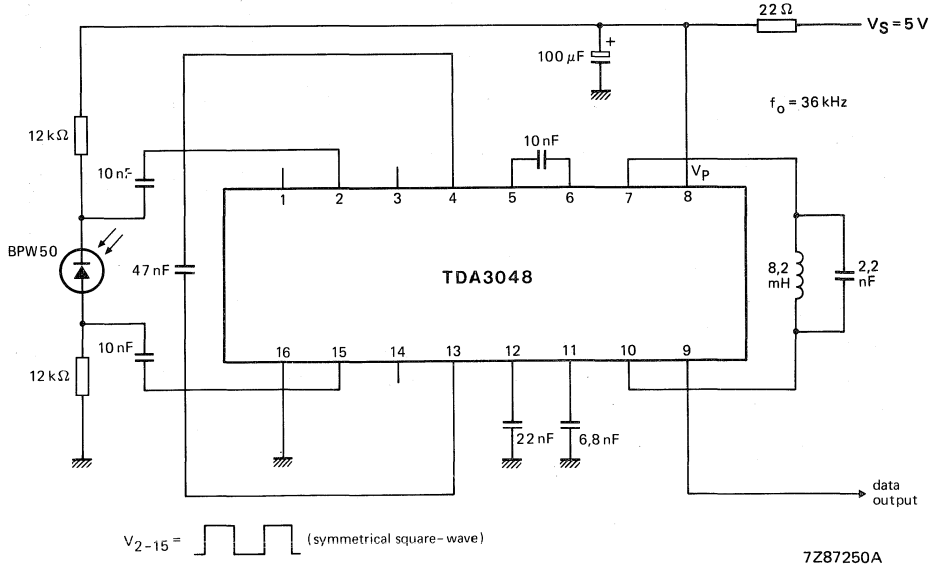


Fig. 4 Wide-band receiver with TDA3048.

For better sensitivity both 12 kΩ resistors may have a higher value.

Multiple output voltage regulators TDA3601Q/TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (LOW current pin)
- V_{P2} supply pin (HIGH current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 µs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulators 1 and 2
- Foldback current limit protection (regulators 3 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	positive supply voltage range					
		operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	positive supply voltage range					
		operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
I_{1tot}	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_{XTAL}	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes to the quick reference data

1. Load dump, during 50 ms, t_r > 2.5 ms
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA
3. V_{P1} = 13.2 V, V_{P2} = R4-sel = R5-sel = 0, I_{R1} = 0

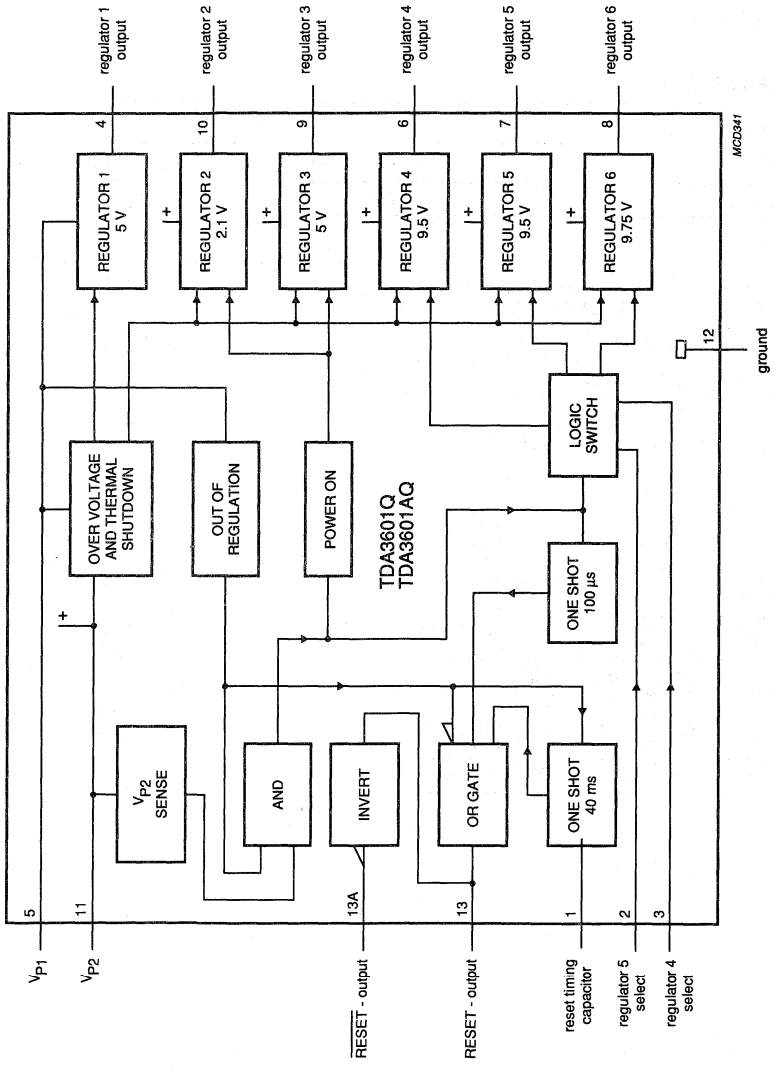


Fig.1 Block diagram.

Multiple output voltage regulators TDA3601Q/TDA3601AQ

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators, four with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3601Q/AQ	13	DIL	plastic	SOT141

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	positive supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.1 V)
V_{P2}	11	positive supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

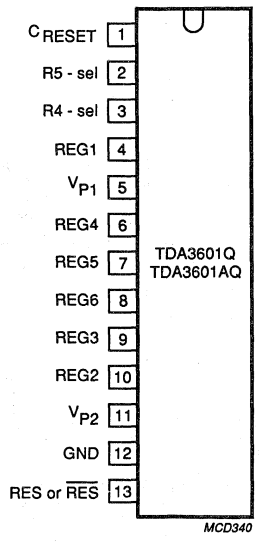


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3601Q is a multiple output voltage regulator with six fixed voltage regulators. Three, logical switch controlled, voltage regulators (numbers 4 to 6) are available, and one non-switchable voltage regulator (number 1). In addition, there are two further regulators (numbers 2 and 3), which are controlled by supply voltages V_{P1} and V_{P2} (Schmitt trigger).

Regulator 1 is not affected by load dump or thermal shutdown. Regulators 2 to 6 are supplied by V_{P2}; they can therefore be switched of by an ignition switch, for example. An internal bandgap voltage reference, which provides a reference voltage for each independent regulator, is supplied by V_{P1}. This supply voltage V_{P1} also supplies regulator 1.

A V_{P2} sense circuit outputs a logical high when the V_{P2} voltage rises through V_{thr}, which remains high until the V_{P2} voltage falls through V_{thf}.

The supply voltage V_{P1} is sensed by an out-of-regulation Schmitt trigger. When this voltage drops below 5.95 V typical, the reset output is disabled, to prevent a microprocessor being disturbed by a too-low supply voltage. An out-of-regulation condition is indicated by a logical low and an in-regulation condition indicated by a logical high.

The 'Power On' switch low will disable regulator 2 and 3 outputs. In addition, the logic switch will be disabled, so that regulators 4 to 6 are switched off. When both V_{P2}-sense and out-of-regulation are high, the 'Power On' will be high, so that the logic multiplexer and regulators 2 and 3 are enabled. Regulators 4 to 6 can now be selected by the multiplexer.

Re-triggerable one-shot circuits produce a RESET (open collector output) when V_{P1} is available (40 ms delay signal), or when both V_{P1} and V_{P2} are available (100 µs pulse). RESET will be held in a constant high state when the supply voltage V_{P1} is less than 5.5 V (5.95 V typical).

The TDA3601 has a RESET output, but the TDA3601A has an inverted RESET output ($\overline{\text{RESET}}$).

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}, V_{P2}	positive supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		note 1; load dump protected; during 50 ms; rise time > 2.5 ms	–	50	V
P_{tot}	total power dissipation	T_{case} < 30 °C	–	15	W
T_{stg}	storage temperature range	non-operating	–55	+150	°C
T_{vj}	virtual junction temperature	operating	–40	+150	°C
V_{pr}	reverse polarity	non-operating	–	6	V

Note to the limiting values

1. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 13.2$ V, $T_{amb} = 25$ °C, $C_{out} = 10$ µF unless otherwise specified. See Fig.5

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	positive supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	positive supply voltage range	operating	11	13.2	18	V
		load dump; note 1	–	–	50	V
I_{P1}	quiescent current	$V_{P2} = 0$; note 3	–	1.1	1.4	mA
Schmitt triggers						
V_{P2} SENSE THRESHOLD						
V_{thr}	rising threshold voltage		7.6	8	8.4	V
V_{thf}	falling threshold voltage		6.2	6.5	6.8	V
V_{hy}	hysteresis		1.35	1.5	1.65	V
OUT-OF-REGULATION THRESHOLD						
V_{thr}	rising threshold voltage		6.8	7.35	7.9	V
V_{thf}	falling threshold voltage		5.5	5.95	6.4	V
V_{hy}	hysteresis		1.2	1.4	1.6	V
Reset circuits (for timing, see Fig.3)						
t_{rst1}	reset delay time	$C_{rst} = 100$ nF	20	40	100	ms
t_{rst}	reset hold time		50	100	150	µs
V_{rl}	reset low	$I_{sync} = 1$ mA	–	0.15	0.8	V
I_{cr}	delay current (pin 1 to C_{rst})		–	5	–	µA
t_r	reset rise time	note 4	–	–	1	µs
t_f	reset fall time	note 4	–	–	1	µs
Regulators						
SELECTOR CONTROL INPUTS R4-SEL AND R5-SEL						
V_{sl}	LOW level input voltage		0.5	–	0.8	V
V_{sh}	HIGH level input voltage		2	–	–	V
I_{hs}	HIGH level input current	$V_{RXsel} > 2$ V	–	–	1	µA
I_{ls}	LOW level input current	$V_{RXsel} < 0.8$ V	–1	–	–	µA
REGULATOR 1 (I_{R1} = 1 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R1}	output voltage	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
		6.25 V ≤ V_{P1} ≤ 18 V	4.75	5	5.25	V
V_{R1L}	output voltage	18 V ≤ V_P ≤ 50 V	4.75	5	5.25	V
ΔV_{R1}	line regulation	6.25 V ≤ V_P ≤ 18 V	–	–	50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{RL1}	load regulation	0.5 mA ≤ I_{R1} ≤ 20 mA	–	–	60	mV
SVRR1	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
V_{Rd1}	drop-out voltage	I_{R1} = 20 mA	–	–	1	V
I_{Rm1}	current limit		30	–	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 2 (I_{R2} = 5 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R2}	output voltage					
		5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
		7 V ≤ V_P ≤ 18 V	1.9	2.1	2.3	V
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
ΔV_{R2}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL2}	load regulation	5 mA ≤ I_{R2} ≤ 200 mA	–	–	70	mV
SVRR2	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
I_{Rm2}	current limit	V_{R2} > 1.75 V; note 6	250	–	–	mA
I_{Rsc2}	short-circuit current	R_L ≤ 0.5 Ω; note 6	–	tbn	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 3 (I_{R3} = 5 mA UNLESS OTHERWISE SPECIFIED)						
V_{R3}	positive output voltage					
		5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5	5.25	V
ΔV_{R3}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL3}	load regulation	5 mA ≤ I_{R3} ≤ 150 mA	–	–	70	mV
SVRR3	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
I_{Rm3}	current limit	V_{R3} > 4.5 V; note 6	200	–	–	mA
I_{Rsc3}	short-circuit current	R_L ≤ 0.5 Ω; note 6	–	200	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 4 (I_{R4} = 5 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R4}	positive output voltage					
		5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R4}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL4}	load regulation	5 mA ≤ I_{R4} ≤ 150 mA	–	–	70	mV
SVRR4	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
V_{Rd4}	drop-out voltage	I_{R4} = 150 mA	–	–	1	V
I_{Rm4}	current limit	V_{R4} > 8.5 V; note 6	200	–	–	mA
I_{Rsc4}	short-circuit current	R_L ≤ 0.5 Ω; note 6	–	200	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 5 (I_{R5} = 5 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R5}	positive output voltage					
		5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
		11 V ≤ V_P ≤ 18 V	9	9.5	10	V
ΔV_{R5}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL5}	load regulation	5 mA ≤ I_{R5} ≤ 200 mA	–	–	70	mV
SVRR5	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
V_{Rd5}	drop-out voltage	I_{R5} = 200 mA	–	–	1	V
I_{Rm5}	current limit	V_{R5} > 8.5 V; note 6	250	–	–	mA
I_{Rsc5}	short-circuit current	R_L ≤ 0.5 Ω; note 6	–	200	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C
REGULATOR 6 (I_{R6} = 5 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R6}	positive output voltage					
		5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.25	V
		11 V ≤ V_P ≤ 18 V	9.3	9.75	10.25	V
ΔV_{R6}	line regulation	11 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL6}	load regulation	5 mA ≤ I_{R6} ≤ 200 mA	–	–	70	mV
SVRR6	supply voltage ripple rejection	f_o = 120 Hz; $V_{P1} = V_{P2}$; note 5	60	–	–	dB
V_{Rd6}	drop-out voltage	I_{R6} = 200 mA	–	–	0.5	V
I_{Rm6}	current limit	V_{R6} > 8.5 V; note 6	300	–	–	mA
I_{Rsc6}	short-circuit current	R_{bel} ≤ 0.5 Ω; note 6	–	250	–	mA
$\Delta V/\Delta T$	thermal drift	–40 ≤ T ≤ 80 °C	–	tbn	–	mV/°C

Notes to the characteristics

1. During 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V, V_{P2} = R4-sel = R5-sel = 0, I_{R1} = 0.
4. External pull-up resistor of 10 kΩ to 5 V required, and C_{load} ≤ 10 pF.
5. $V_{P1} = V_{P2}$ = 13.2 V, ripple on $V_{P1} = V_{P2}$ of: 1 $V_{(p-p)}$, f_o = 120 Hz.
6. Foldback current protection behaviour: see Fig.4

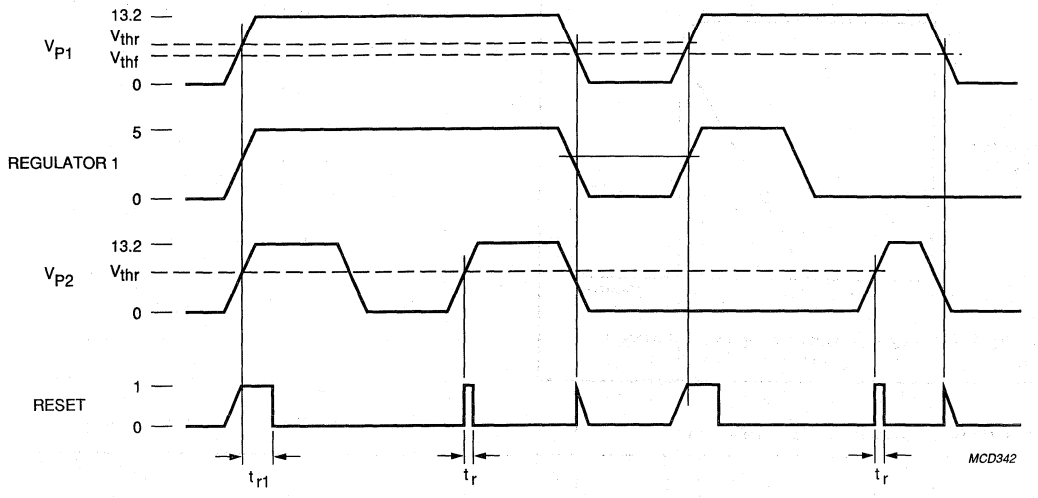


Fig.3 Timing reset.

Regulators truth table

INPUTS		0 = LOW/OFF		OUTPUTS				
		1 = HIGH/ON		X = don't care				
V_{P1}	V_{P2}	R4-sel	R5-sel	REG.1	REGS. 2 & 3	REG.4	REG.5	REG.6
0	X	X	X	0	0	0	0	0
1	0	X	X	1	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	0	1	1
1	1	1	1	1	1	0	0	1

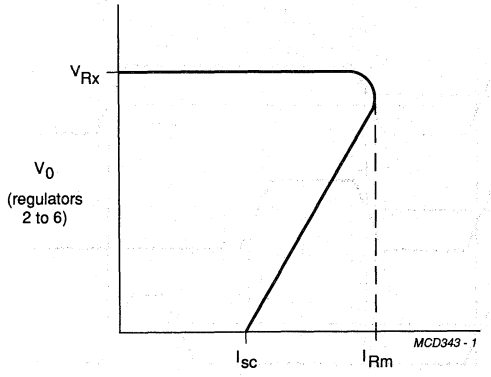
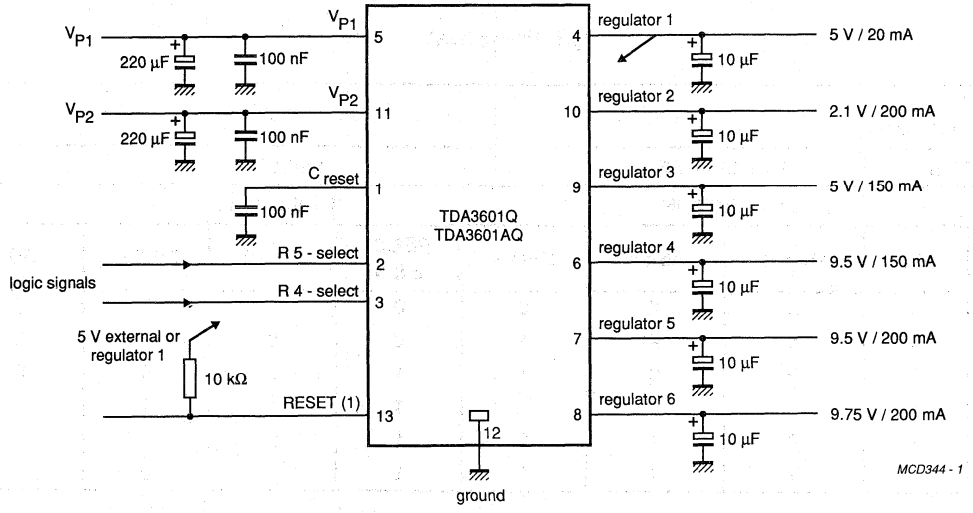


Fig.4 Foldback current protection behaviour.

TEST AND APPLICATION INFORMATION



(1) RESET output for TDA3601Q; $\overline{\text{RESET}}$ output for TDA3601AQ.

Fig.5 Application circuit.

Multiple output voltage regulator TDA3602

FEATURES

- Two V_P-state controlled regulators (1 and 2)
- Regulator 3 operates during load dump or thermal shutdown
- Multi-function control pin
- A back-up circuit for Regulator 3, via a single capacitor
- Low reverse current Regulator 3
- Low quiescent current in coma mode
- HOLD output
- RESET output
- High ripple rejection.

PROTECTION

- Foldback current limit protection (Regulators 1 and 2)
- Load dump protection
- Thermal protection
- DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

GENERAL DESCRIPTION

The TDA3602 is a multiple output voltage regulator, intended for use in car radios with or without a microprocessor. It contains two fixed voltage regulators with foldback current protection (Regulators 1 and 2), and one fixed voltage regulator that also operates during load dump and thermal shutdown. This regulator can be used to supply a microprocessor.

A back-up circuit supplies Regulator 3 during a short period after the power is cut off (negative field decay or engine start procedure). A state control pin (Pin 4) controls the device, which can be switched through four stages using the information at this pin. The switching levels at this pin contain hysteresis.

RESET and HOLD outputs can be used to interface with a microprocessor. The RESET signal can be used to call up or initialize a microprocessor (power on reset). The HOLD signal can be used to control the power stages (mute signal in a low end application), or to generate a HOLD interrupt (microprocessor application).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_P	positive supply voltage range					
		operating	9.2	14.4	18	V
		Regulator 3 ON	6.0	14.4	18	V
		jump start	–	–	30	V
		load dump; Regulator 3 ON	–	–	50	V
I_P	total quiescent current	coma mode	–	290	–	µA
T_{vj}	virtual junction temperature		–	–	+150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	$0.5\ mA \leq I_{R1} \leq 250\ mA$	8.2	8.5	8.8	V
V_{R2}	output voltage regulator 2	$0.5\ mA \leq I_{R2} \leq 140\ mA$	4.8	5	5.2	V
V_{R3}	output voltage regulator 3	$0.5\ mA \leq I_{R3} \leq 50\ mA$	4.8	5	5.2	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3602	9	SIL	plastic	SOT110

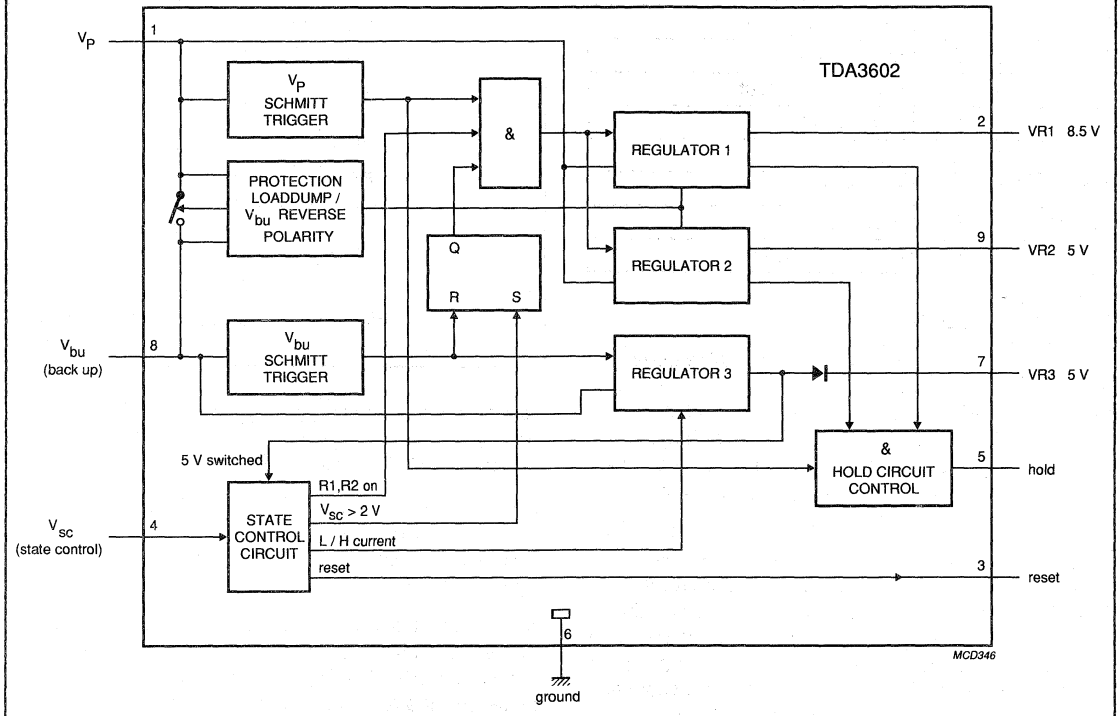


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
REG1	2	regulator 1 output
RESET	3	reset output
SCI	4	state control input
HOLD	5	hold output
GND	6	ground
REG3	7	regulator 3 output
V_{bu}	8	back-up
REG2	9	regulator 2 output

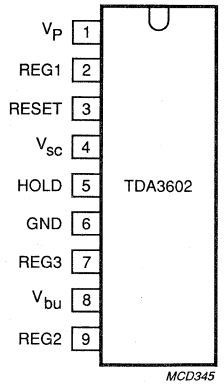


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

This multiple output voltage regulator contains three fixed voltage regulators, numbered 1, 2 and 3. Two of these can be switched between the on and off states using the state control pin (Pin 4). The third (Regulator 3), which is continuously in, can be switched by the state control pin between a low and a high current mode.

In addition to Regulators 1 and 2, the device is supplied by an internal switch that is open when the supply voltage falls below the back-up voltage (negative field decay or engine start procedure), or during a load dump. (During this load dump, Regulators 1 and 2 are switched off.) This switched voltage (the so-called back-up voltage (V_{bu})), is available at Pin 8. An electrolytic capacitor can be connected to this pin, and the charge on this capacitor can be used to supply the device for a short period after the voltage is removed.

For interfacing with a microprocessor, three pins are provided:

- state control pin
- hold output pin
- reset output pin.

When the supply voltage (V_P) is connected to the device, V_{bu} will rise. When V_{bu} reaches 7.9 V, the device is in the power on mode. The RESET output goes high and Regulator 3 is switched on. In a microprocessor application, the RESET output can be used to call up the CPU and to initialize the program. What follows depends on the voltage at the state control pin (V_{sc}). In most applications, when the supply voltage is connected, V_{sc} will rise slowly (e.g. by charging a capacitor).

The device will come out of the power on mode into the reset mode when V_{sc} rises above 2.2 V. In both the power on and reset modes, Regulator 3 will be in the high current mode, Regulators 1 and 2 will be switched off and the RESET output will be high.

The device will enter the wake mode when V_{sc} reaches 2.8 V. The RESET pin will go low and the CPU must be switched to the sleep mode. Regulator 3 is still in the high current mode.

As V_{sc} continues rising and the voltage reaches 3.6 V, the device will be switched into the sleep mode. It will be in a coma mode when V_{sc} is greater than 3.8 V. In this mode, only the relevant circuits remain operating; this is to keep the power consumption as low as possible - typically 290 µA.

If the device is switched on with V_{sc} already higher than 3.8 V, the device will be switched directly from the power on mode into the coma mode.

When V_{sc} is lowered gradually from 3.6 V (or higher) to 2 V, the device will go from sleep to reset again.

V_{sc} must be lower than 1.1 V to bring the device into the on mode; note that this is not the same as the **power on** mode. In this condition, Regulator 3 is in the high current mode, both Regulators 1 and 2 are switched on and the HOLD output will be high (depending on the state of V_P and the in-regulation condition of Regulators 1 and 2). When the device is in the on mode, it will switch back to the reset mode when V_{sc} rises to 2 V, or when the supply voltage drops below 7.6 V.

When V_{bu} drops below 3 V, the device will return to the power off mode, no matter what condition the device was in.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
		operating	–	18	V
		jump start; $t \leq 10$ min	–	30	V
		load dump protected; $t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
V_{pr}	reverse polarity	non-operating	–	6	V
P_{tot}	total power dissipation		–	15	W
T_{stg}	storage temperature range	non-operating	–55	+150	°C
T_{vj}	virtual junction temperature range	operating	–40	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	50 K/W
$R_{th\ j\text{-}c}$	from junction to case (see Fig.6)	12 K/W

CHARACTERISTICS

V_P = 14.4 V, T_{amb} = 25 °C, unless otherwise specified. See Fig.6.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range					
		operating	9.2	14.4	18	V
		Regulator 3 operating; note 1	6.0	14.4	18	V
		jump start; t ≤ 10 min	–	–	30	V
		load dump; t ≤ 50 ms; t_r ≥ 2.5 ms	–	–	50	V
I_P	quiescent current					
		V_{sc} > 4 V; V_P = 12.4 V; note 2	–	280	360	µA
		V_{sc} > 4 V; V_P = 14.4 V; note 2	–	290	–	µA
Schmitt triggers						
V_{P2} SCHMITT TRIGGER (FOR HOLD AND REGULATORS 1 AND 2)						
V_{thr}	rising voltage threshold		7.3	7.6	8.0	V
V_{thf}	falling voltage threshold		6.8	7.1	7.5	V
V_{hy}	hysteresis		–	0.5	–	V
REGULATOR 1 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	V_{R1} – 0.2	–	V
V_{thf}	falling voltage threshold		–	V_{R1} – 0.3	–	V
V_{hy}	hysteresis		–	0.1	–	V
REGULATOR 2 SCHMITT TRIGGER (FOR HOLD)						
V_{thr}	rising voltage threshold		–	V_{R2} – 0.2	–	V
V_{thf}	falling voltage threshold		–	V_{R2} – 0.3	–	V
V_{hy}	hysteresis		–	0.1	–	V
VBU SCHMITT TRIGGER (REGULATOR 3)						
V_{thr}	rising voltage threshold V_{bu}		7.3	7.9	8.4	V
V_{thf}	falling voltage threshold V_{reg3}		2.5	3	3.5	V
V_{hy}	hysteresis		–	4.9	–	V
State control pin						
V_{th}	voltage threshold between sleep and coma	note 2	–	V_{thr1} + 0.2	–	V
V_{thr1}	voltage threshold wake to sleep		3.4	3.6	3.8	V
V_{thf1}	voltage threshold sleep to wake		2.5	2.7	2.9	V
V_{hy1}	hysteresis wake/sleep		0.85	0.92	1.0	V
V_{thr2}	voltage threshold reset to wake		2.6	2.8	3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{thf2}	voltage threshold wake to reset		1.8	1.9	2	V
V_{hy2}	hysteresis reset/wake		0.85	0.92	1.0	V
V_{thr3}	voltage threshold on to reset		1.9	2	2.1	V
V_{thf3}	voltage threshold reset to on		1	1.1	1.2	V
V_{hy3}	hysteresis on/reset		0.85	0.92	1.0	V
I_{scl}	input current					
		$V_{sc} \leq 0.8$ V	–	–	−1	µA
		$V_{sc} \geq 4$ V	–	–	1	µA
HOLD and RESET outputs						
RESET CIRCUIT						
V_{OL}	LOW level output voltage	$I_O = 0$	0	0.2	0.8	V
V_{OH}	HIGH level output voltage		2	5	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V	0.3	0.8	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	0.3	2	–	mA
HOLD CIRCUIT						
V_{OL}	LOW level output voltage	$I_O = 0$	0	0.2	0.8	V
V_{OH}	HIGH level output voltage		2.0	5.0	5.25	V
I_{OL}	LOW level output current	$V_{OL} \leq 0.8$ V; note 3	0.3	1	–	mA
I_{OH}	HIGH level output current	$V_{OH} > 3$ V	0.3	2	–	mA
Regulators						
REGULATOR 1 (I_{R1} = 5 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R1}	output voltage OFF	$V_{sc} > 2.1$ V	–	1	400	mV
V_{R1}	output voltage					
		$0.5\text{ V} \leq I_{R1} \leq 250$ mA	8.2	8.5	8.8	V
		$10\text{ V} \leq V_P \leq 18$ V	8.2	8.5	8.8	V
ΔV_{R1}	line regulation	$10\text{ V} \leq V_P \leq 18$ V	–	–	50	mV
ΔV_{RL1}	load regulation	$0.5\text{ mA} \leq I_{R1} \leq 250$ mA	–	–	50	mV
SVRR1	supply voltage ripple rejection	f = 200 Hz; 2 $V_{(p-p)}$	60	–	–	dB
V_{Rd1}	drop-out voltage	$I_{R1} = 250$ mA	–	–	0.4	V
I_{Rm1}	current limit	$V_{r1} > 7$ V; note 5	0.4	–	1.2	A
I_{Rsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 5	–	250	–	mA

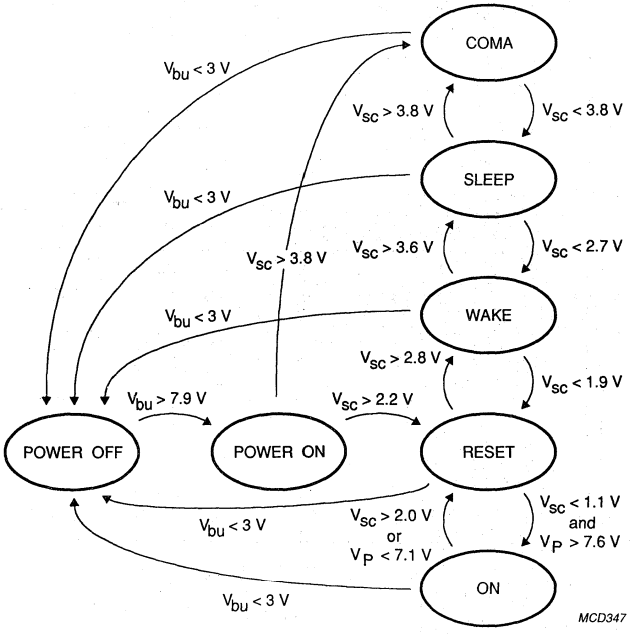
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATOR 2 (I_{R2} = 10 mA UNLESS OTHERWISE SPECIFIED.)						
V_{R2}	output voltage OFF	$V_{sc} > 2.1$ V	–	1	400	mV
V_{R2}	output voltage					
		0.5 mA ≤ I_{R2} ≤ 140 mA	4.8	5	5.2	V
		8 V ≤ V_P ≤ 18 V	4.8	5	5.2	V
ΔV_{R2}	line regulation	8 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL2}	load regulation	0.5 mA ≤ I_{R2} ≤ 140 mA	–	–	50	mV
SVRR2	supply voltage ripple rejection	f = 200 Hz; 2 $V_{(p-p)}$	60	–	–	dB
V_{Rd2}	drop-out voltage	I_{R2} = 140 mA	–	1.2	–	V
I_{Rm2}	current limit	$V_{R2} > 4.5$ V; note 5	200	–	600	mA
I_{Rsc2}	short-circuit current	R_L ≤ 0.5 Ω; note 5	–	130	–	mA
REGULATOR 3 (I_{R3} = 5 MA UNLESS OTHERWISE SPECIFIED.)						
V_{R3}	output voltage					
		0.5 mA ≤ I_{R3} ≤ 50 mA	4.8	5	5.2	V
		7 V ≤ V_P ≤ 18 V	4.8	5	5.2	V
		18 ≤ V_P ≤ 50 V	4.8	5	5.2	V
ΔV_{RL3}	output voltage	sleep mode; I_{R3} ≤ 1 mA; note 2	4.5	5	5.5	V
I_{Lo1}	leakage output current	V_P=0; V_{bu} = 6 V; V_{R3} = 6 V	–	–	1	µA
ΔV_{R3}	line regulation	7 V ≤ V_P ≤ 18 V	–	–	50	mV
ΔV_{RL3}	load regulation	0.5 mA ≤ I_{R1} ≤ 50 mA	–	–	50	mV
SVRR3	supply voltage ripple rejection	f = 200 Hz; 2 $V_{(p-p)}$	60	–	–	dB
V_{Rd3}	drop-out voltage	I_{R3} = 50 mA; note 6	–	–	0.4	V
I_{Rm3}	current limit	$V_{r3} > 4.5$ V; note 4	140	–	500	mA
Switch						
V_{swd}	drop-out voltage	I_{sw} = 50 mA	–	–	0.45	V
I_{swm}	maximum current		140	–	–	mA

Notes to the characteristics

1. Minimum operating voltage only if V_P has exceeded 8 V
2. In the sleep mode, Regulators 1 and 2 are OFF. In the coma mode, the state control circuit is also switched off, to make the quiescent current as low as possible
3. Hold circuit can sink this current in the RESET state and the ON state
4. At current limit, I_{Rm} is held constant (behaviour according to the broken line in Fig.5)
5. The foldback current protection limits the dissipated power at short-circuit (see Fig.5)
6. The drop-out voltage of Regulator 3 is measured between V_{bu} and V_{reg3} (pins 8 and 7).

Table 1 State control pin

V_{P1} SCHMITT TRIGGER IS TRUE				
STATE	**REG3 (5 V)**	**REG1 + REG2**	**RESET**	**REMARKS**
Coma	LOW current	OFF	0	Stabilizer consumes low quiescent current. The state control circuit is switched off, to lower the quiescent current.
Sleep	LOW current	OFF	0	State control circuit on.
Wake	HIGH current	OFF	0	CPU in sleep mode.
Reset	HIGH current	OFF	1	CPU called up.
On	HIGH current	ON	1	Normal operation.
Power on	HIGH current	OFF	1	V_{P1} rises from 0 to 8.5 V or higher (first start-up).
Power off	OFF	OFF	0	V_{P2} falls from V_P to less than 3 V (V_{R3} = 2.5 V).



V_{bu} = back-up voltage.

V_{sc} = state control voltage.

Fig.3 State diagram.

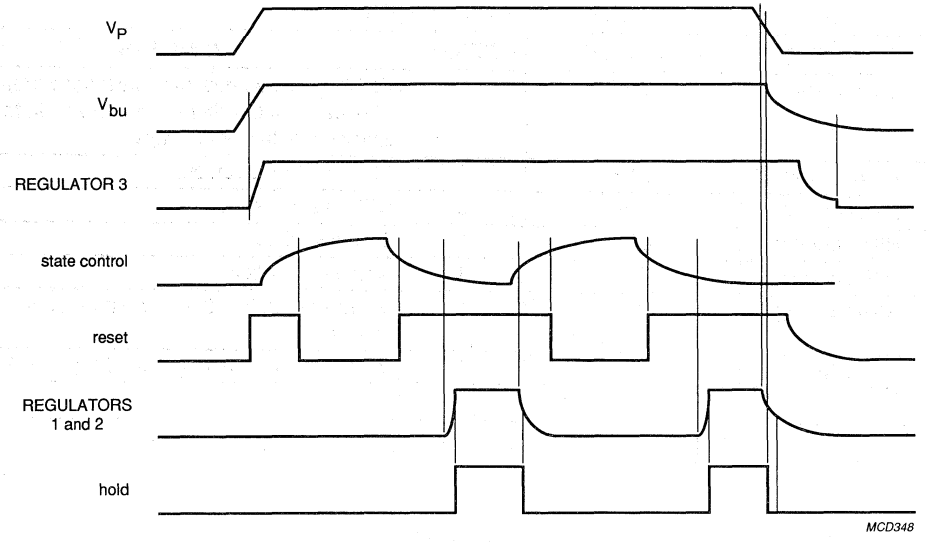


Fig.4 Timing diagram.

Table 2 Logic table HOLD function

INPUTS FOR HOLD (Note 1)					OUTPUT
V_{bu}	V_P SCHMITT TRIGGER	ON STATE	REG1	REG2	HOLD
1	0	X	0	0	0
0	1	X	0	0	0
1	1	0	0	0	0
1	1	1	0	X	0
1	1	1	X	0	0
1	1	1	1	1	1

Where: 0 = off; 1 = on; X = don't care.

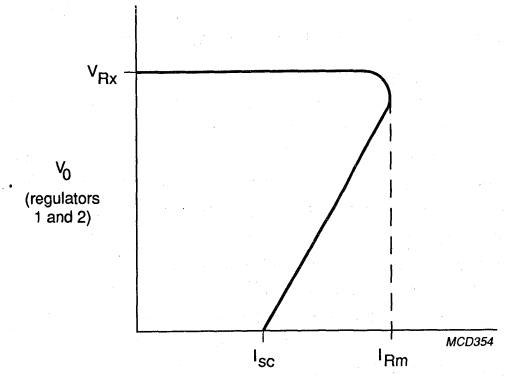


Fig.5 Foldback current protection behaviour.

QUALITY SPECIFICATION

Quality according to UZW-BO/FQ-0601.

Pins 3 and 5 (Reset and Hold) do not meet the ESD norm for positive pulses (both human body and machine model) because of application.

Reset (pin 3): +1200 V (human body), +150 V (machine model)
Hold (pin 5): +1200 V (human body), +150 V (machine model)

TEST AND APPLICATION INFORMATION

Test information

The outputs of the regulators are measured by means of a selector switch (one by one). In addition, switch SW2 is only closed when V_{bu} is greater than V_P; then the TDA3602's internal switch is opened.

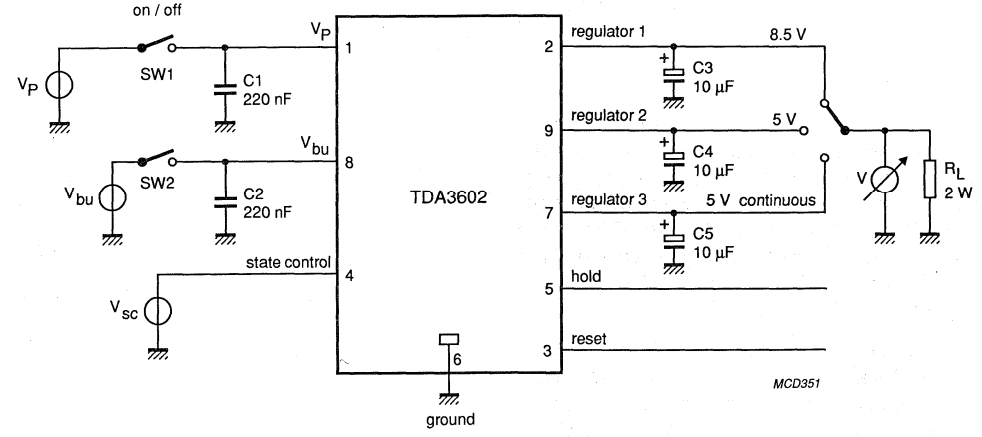


Fig.6 Test circuit.

Application circuits

Three possible application circuits are covered in this section:

1. A low end application, with the device connected to the switched supply voltage.
2. A low end application, with the device connected to the continuous supply voltage (battery). The device can be switched on and off by means of two simple push switches to ground, or an ordinary on/off switch.
3. The last is a microprocessor-controlled radio set application, with the microprocessor connected to regulator 3.

Device without microprocessor (1)

The low end application is illustrated in Fig.7. When switch SW1 is closed, a pulse is generated at the state control input by C5 and R1, and the regulator is switched from power off to the on mode (all three regulators are on). The HOLD signal can be used to control the mute signal for the power amplifiers. This signal is high when all the regulators are in regulation and V_{P1} Schmitt trigger is true.

Device without microprocessor (2)

Fig.8 illustrates the application circuit for a low end radio set with push-switches when no microprocessor is used. The device can be switched to the on mode by pressing SW1. In this mode, Regulators 1 and 2 are switched on, so transistor T1 takes over from switch SW1. The device can only be switched off by connecting the base of T1 to ground (SW1 not pressed). This can be achieved by pressing SW2.

The hold signal is only high when the device is in the on mode and both V_P and the regulators are available, so that this signal can be used to control the power stages (mute). During a fault condition, this signal turns low immediately.

When the device is connected to the supply for the first time, the initial state will be the power on stage, so Regulators 1 and 2 are not switched on.

Device used with microprocessor

For a good understanding of the high end application, shown in Fig.9, consult also the flow chart in Fig.10.

When the set is off, a reset can be generated by connecting the set to the supply for the first time (device in power on), or by pressing any key on the key matrix (device in reset mode). When the reset is generated, the device is held in the reset mode for a short period by T1. The microprocessor has to take over control by making reset mode equal to 0. The microprocessor can then proceed with the initializing process. After this action, the microprocessor has to check if the correct key has been pressed. If so, the radio can be switched on by making on equal to 0; if not, the microprocessor must switch the device to the coma mode again, by making reset mode and on both equal to 1; (wake mode is entered after a short time constant, determined by r1 x C7 x const), and switch itself to sleep mode.

When the reset is generated for the first time (power on mode), the mode of the device can be detected by the hold signal. If on = 0 and hold remains low, then the microprocessor is in the power on mode. In this case, the microprocessor must go to the switch-off routine (making on and reset mode both equal to 1).

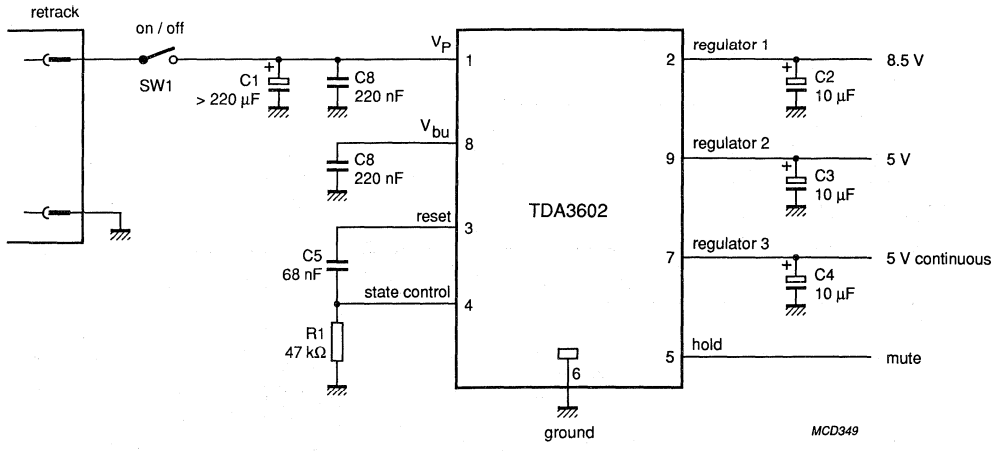


Fig.7 Application circuit 1.

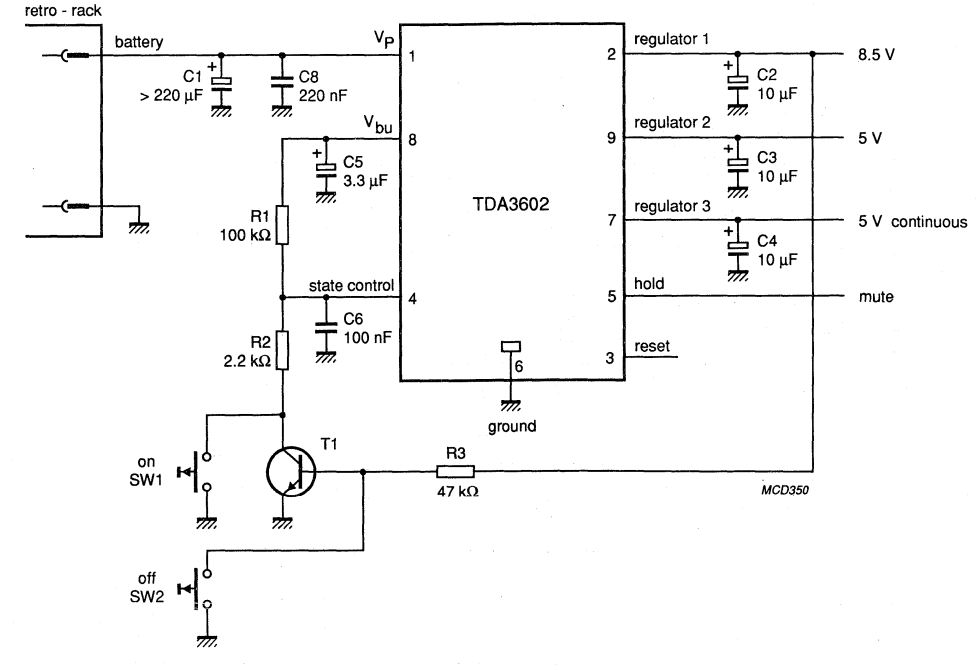


Fig.8 Application circuit 2.

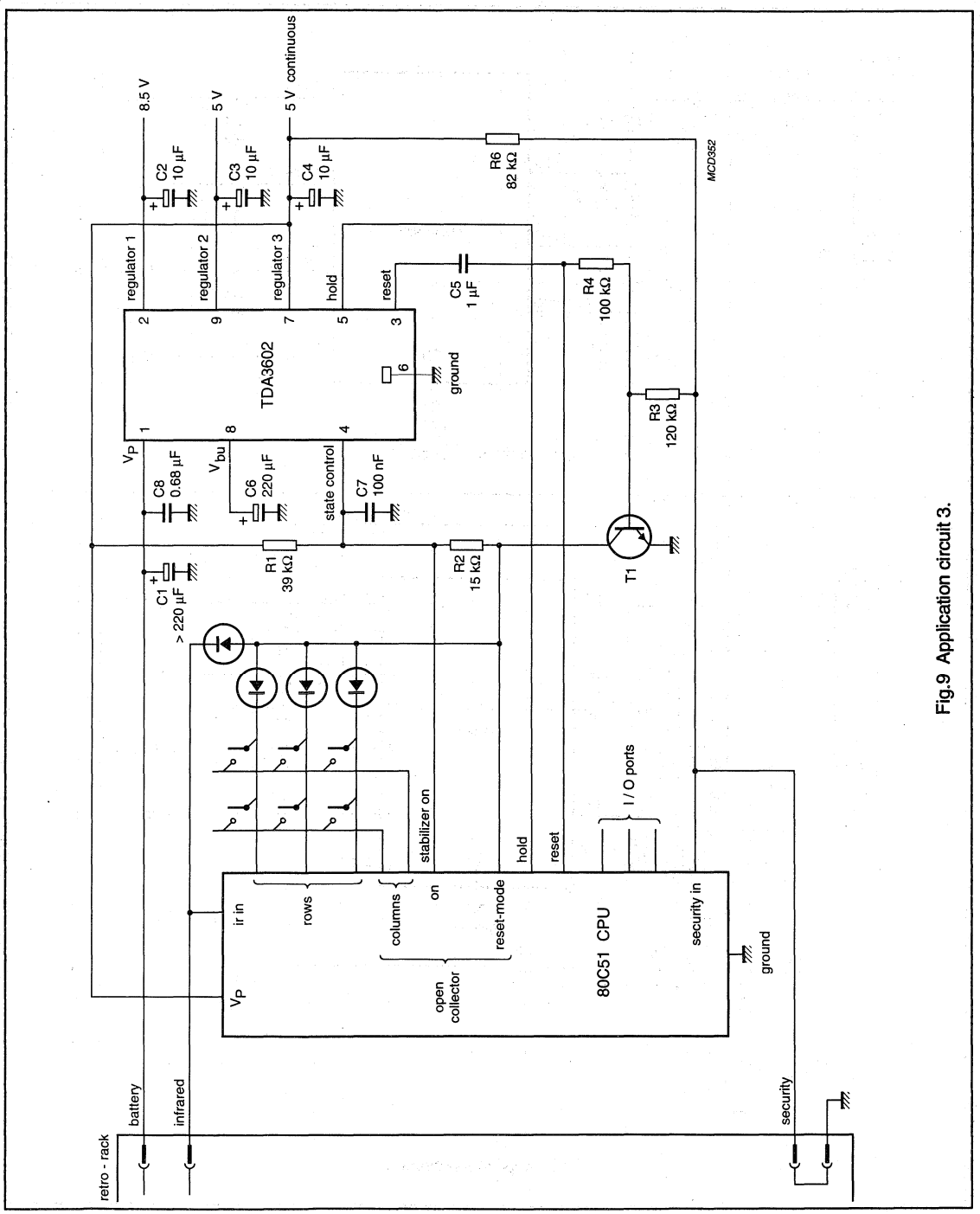


Fig.9 Application circuit 3.

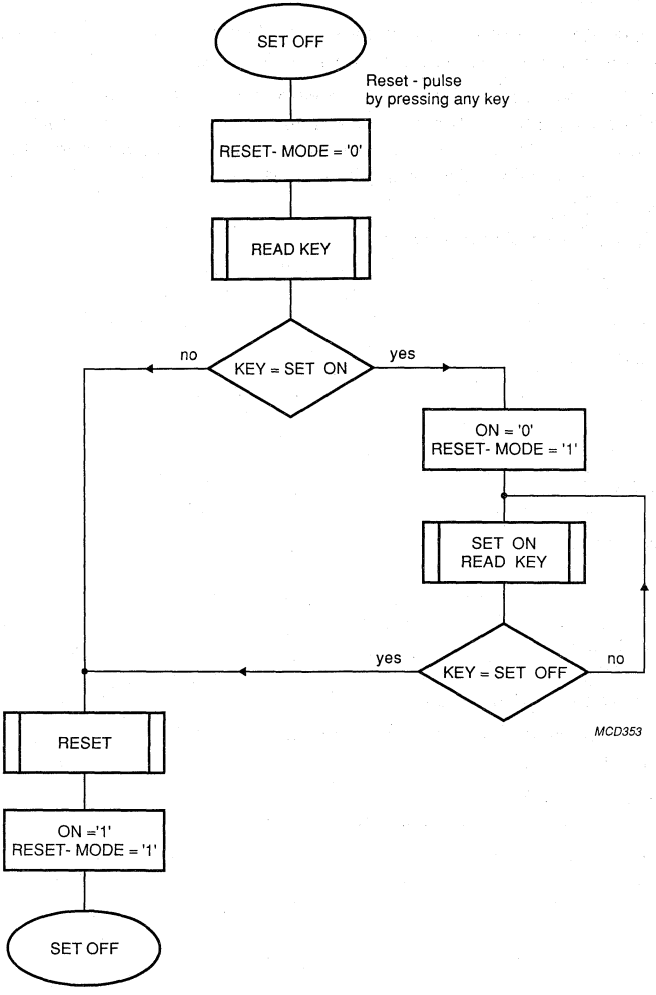


Fig.10 Flow chart for application circuit 3.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102HE).

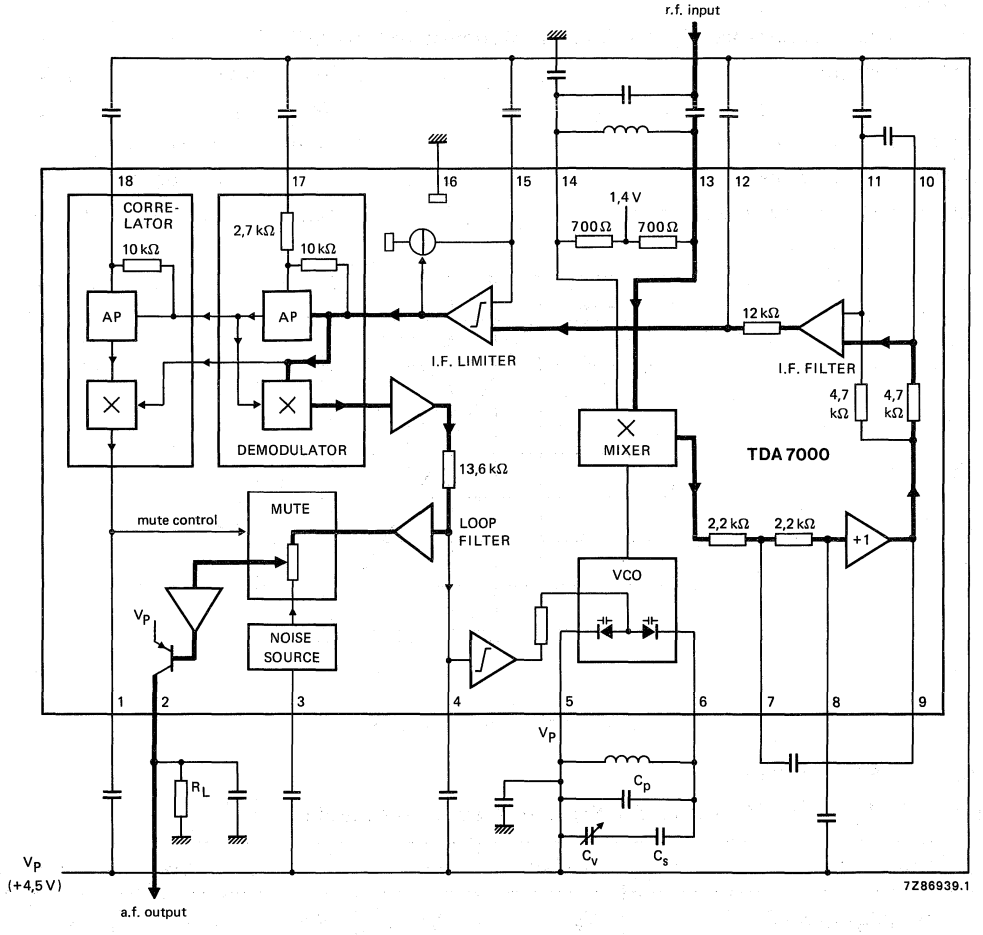


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	–55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 60	°C

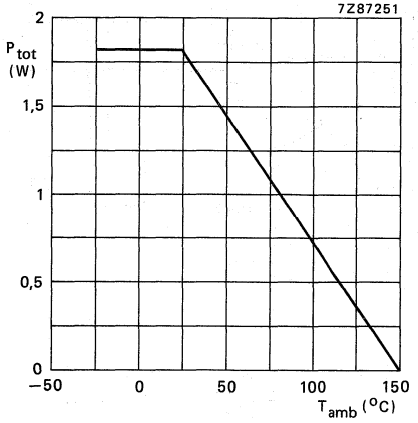


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	V_{14-16}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-16}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

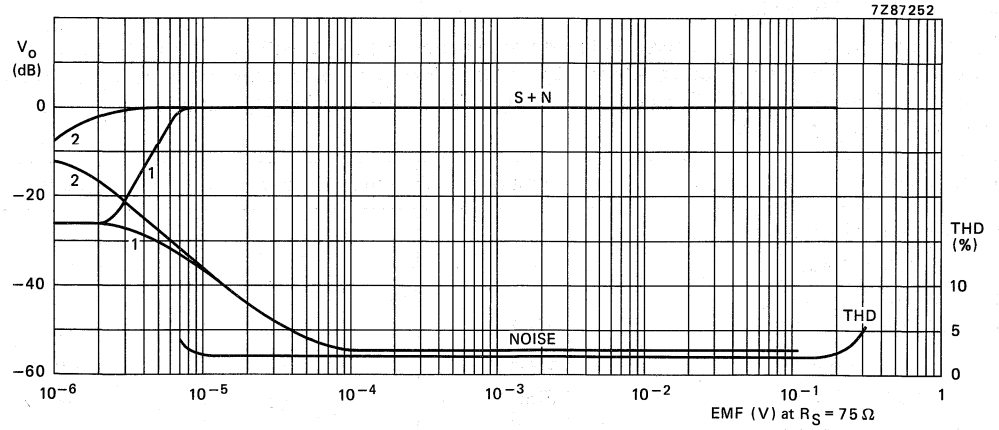


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm 22{,}5$ kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm 75$ kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

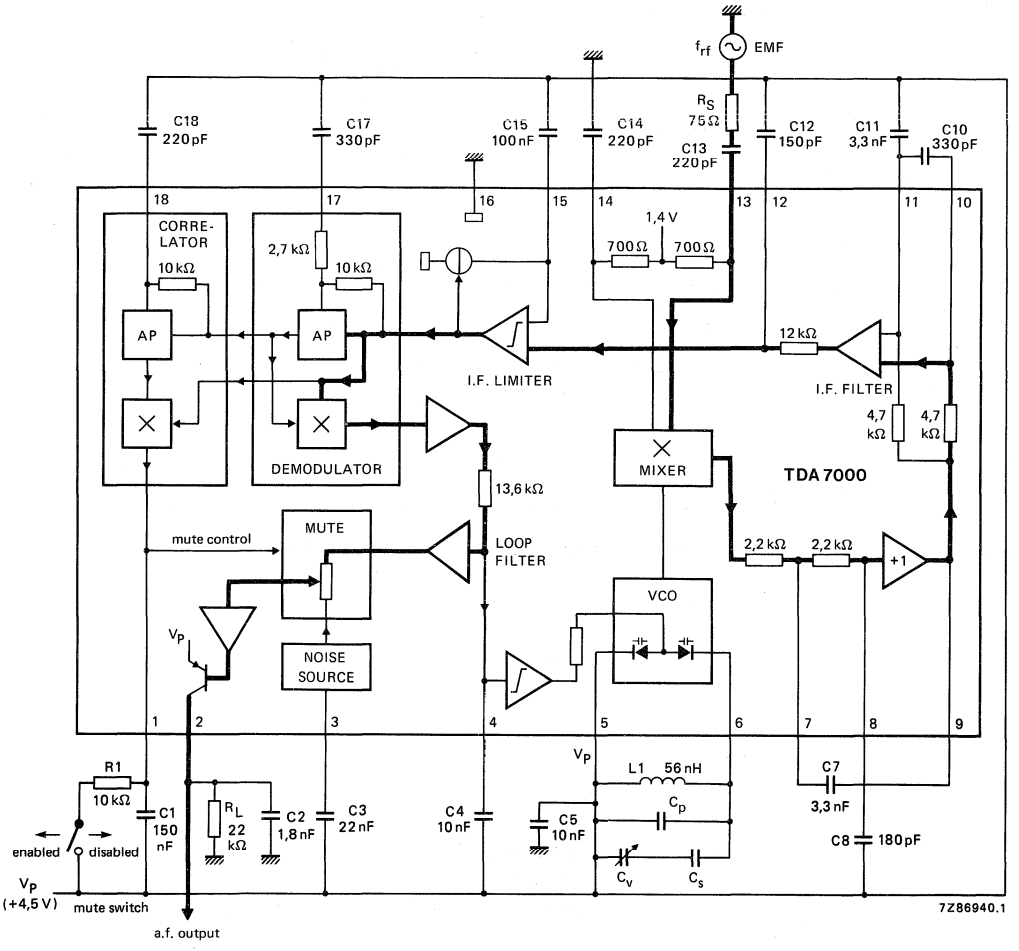


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

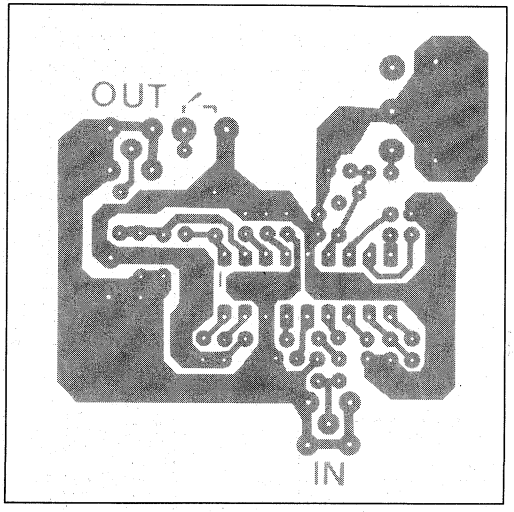


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

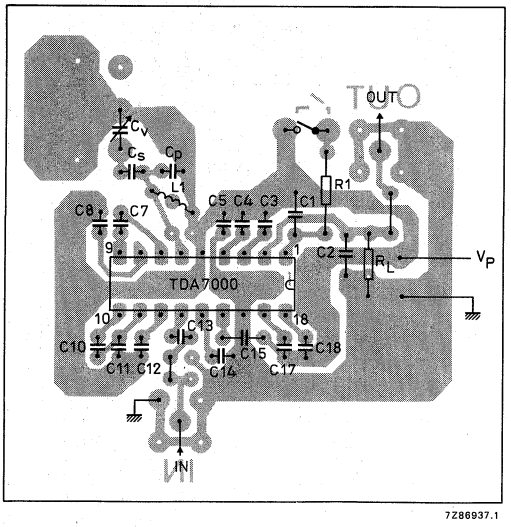


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 4)	V_P		2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ.	8	mA
R.F. input frequency range	f_{rf}		1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ.	1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ.	200	mV
A.F. output voltage at R_L = 22 kΩ	V_O	typ.	75	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

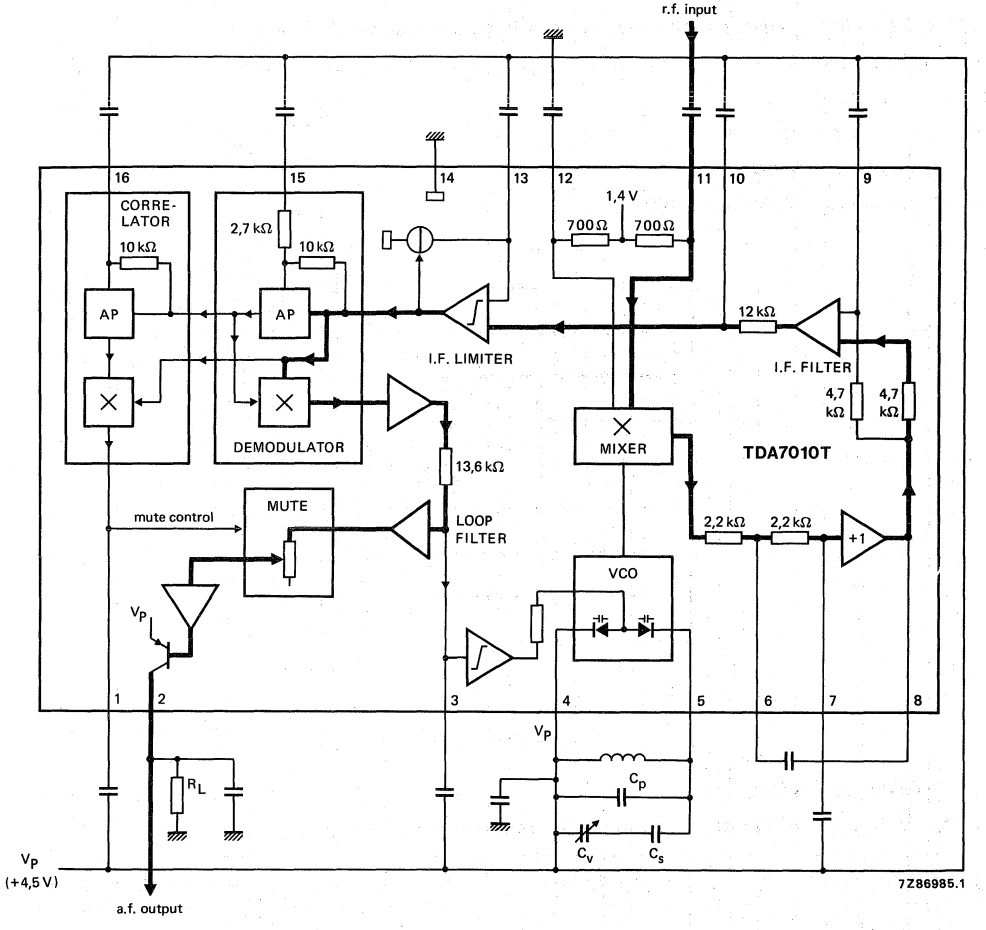


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	V_P	max.	12 V
Oscillator voltage (pin 5)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	–55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 60	°C

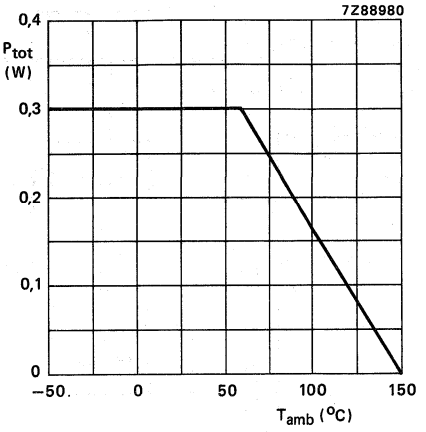


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 5)	I_5	–	280	–	μA
Voltage at pin 12	V_{12-14}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-14}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 5	$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	43	–	dB
	S_{-300}	–	28	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

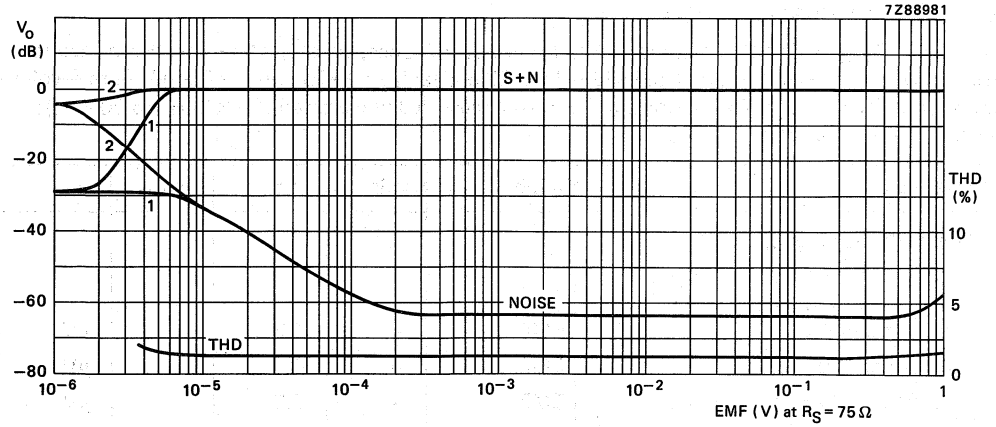


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm 22{,}5$ kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm 75$ kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.

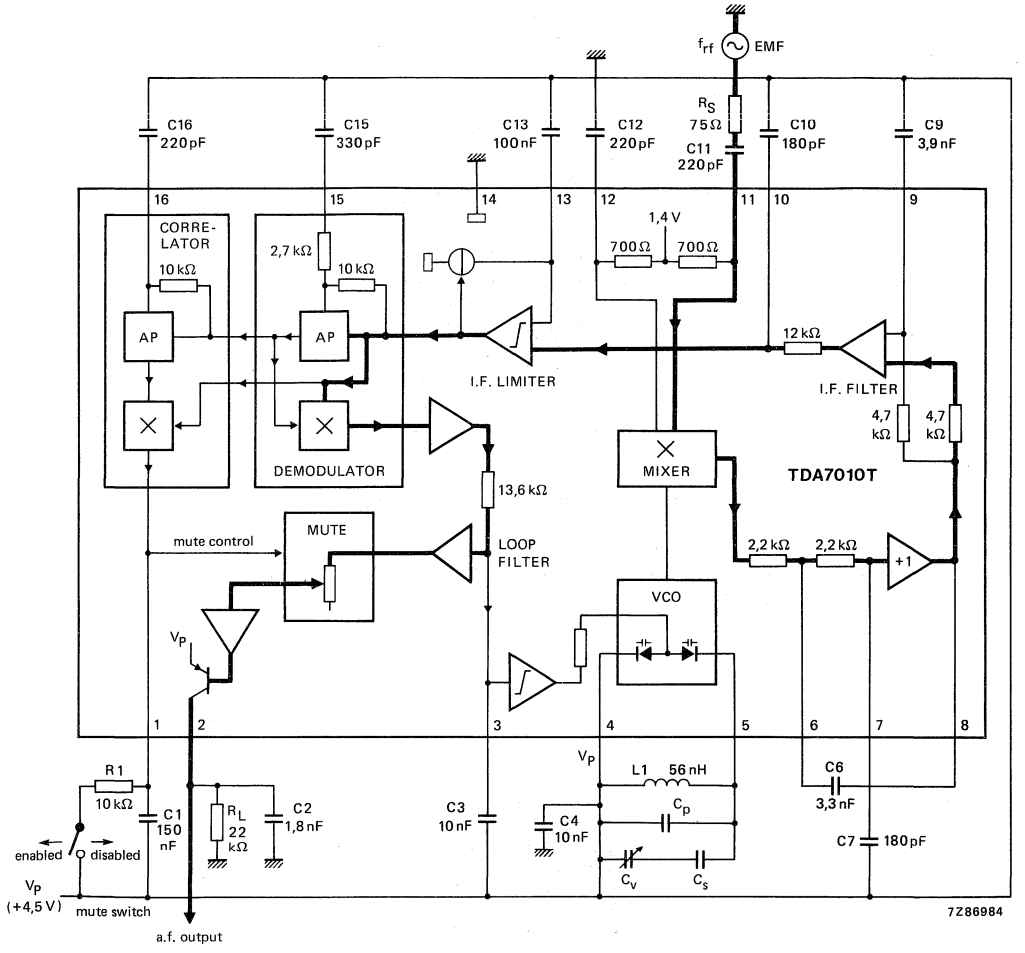


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

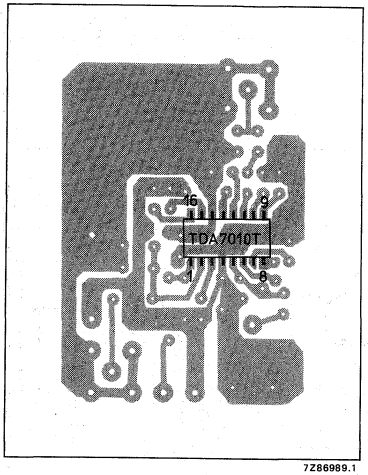


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

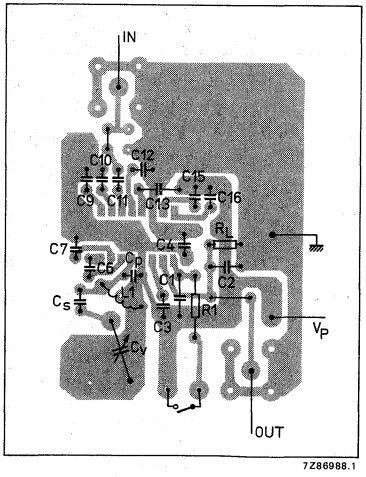


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT FOR MTS

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  - mono earphone amplifier or
  - MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	–	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
RF input frequency		f_{rf}	1,5	–	110	MHz
Sensitivity (e.m.f.) for –3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	–	4	–	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	–	200	–	mV
AF output voltage		V_o	–	90	–	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

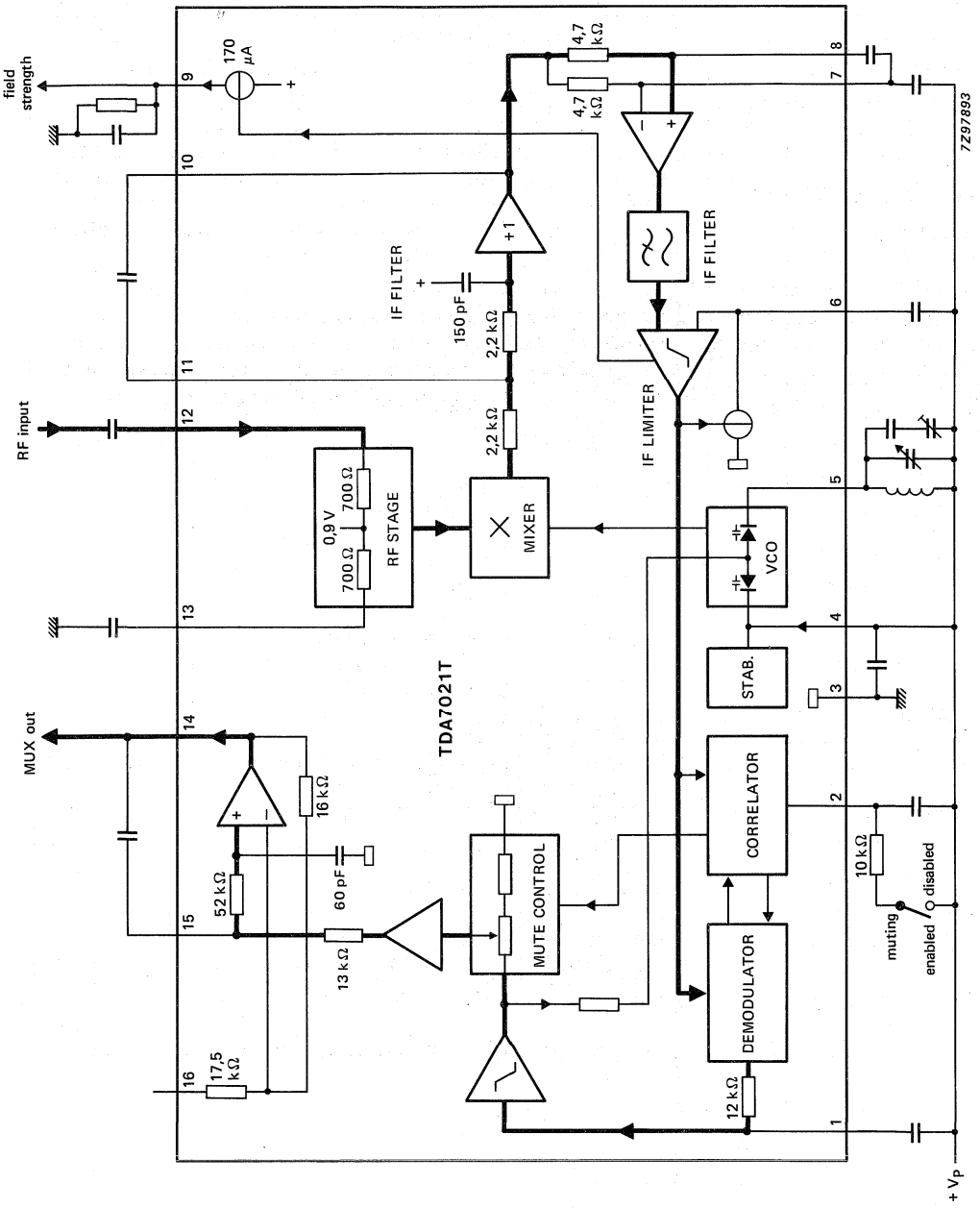


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	–	7,0	V
Oscillator voltage		V_{5-4}	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–10	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 °C, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	μA
Voltage at pin 13		V_{13-3}	–	0,9	–	V
Output voltage (pin 14)		V_{14-3}	–	1,3	–	V

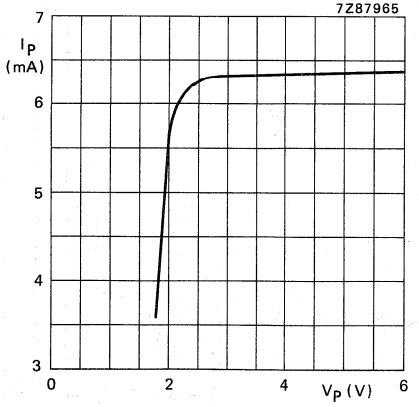


Fig. 2 Supply current as a function of the supply voltage.

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for −3 dB limiting	muting disabled	EMF	–	4,0	–	μV
for −3 dB muting		EMF	–	5,0	–	μV
for (S+N)/N = 26 dB		EMF	–	7,0	–	μV
Signal handling (e.m.f.)	THD < 10%;					
	Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	Δf = ± 22,5 kHz	THD	–	0,7	–	%
	Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5-4(rms)}$	–	250	–	mV
Variation of oscillator frequency with temperature	V_P = 1 V	$\frac{\Delta f_{osc}}{\Delta T_{amb}}$	–	5	–	kHz/°C
Selectivity	see Fig. 9; no modulation	S_{+300}	–	46	–	dB
		S_{-300}	=	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 μs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	−100	–	+100	μA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

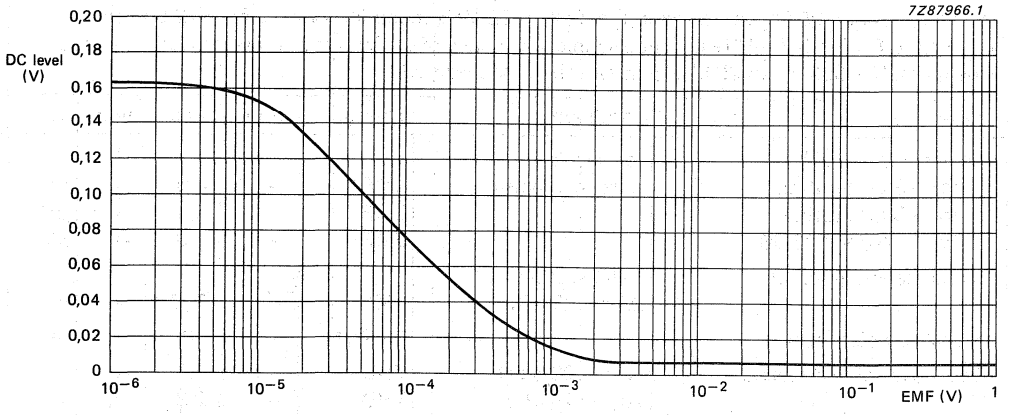


Fig. 3 Field strength voltage (V_{g-3}) at R_{source} = 1 kΩ; f = 96,75 MHz; Vp = 3 V.

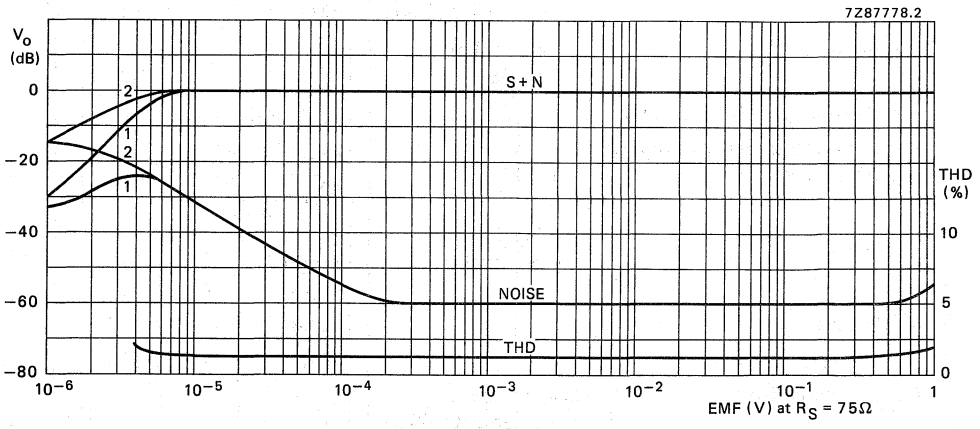
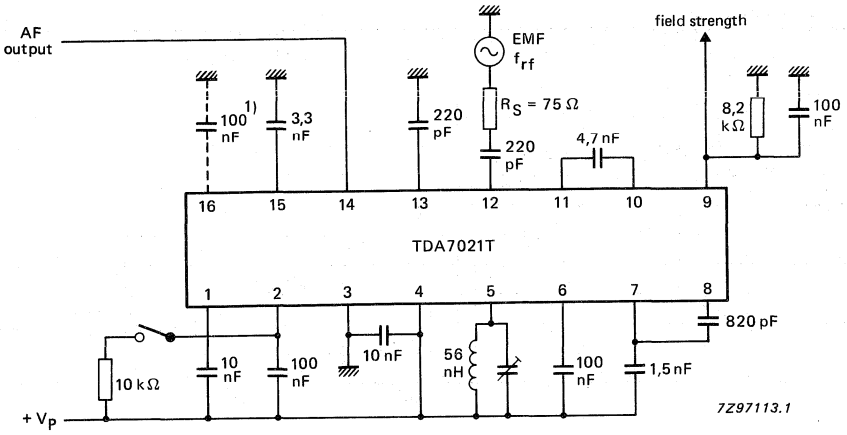


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S+300	–	40	–	dB
		S–300	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on:					
	at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

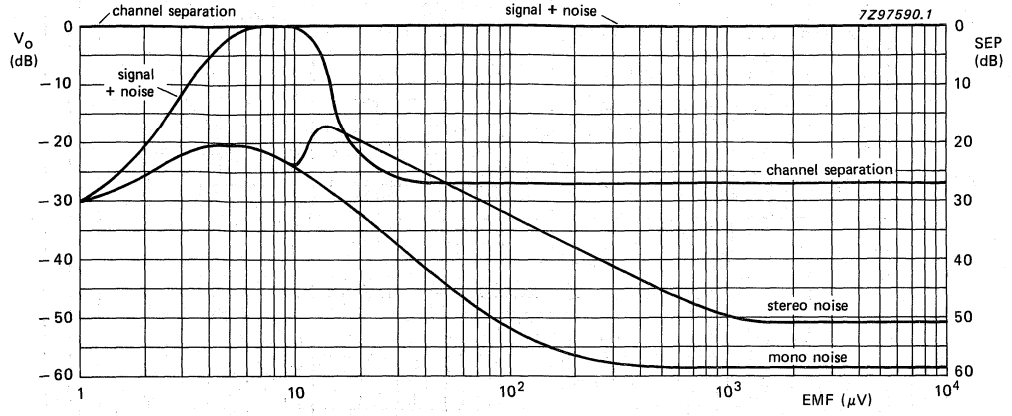


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

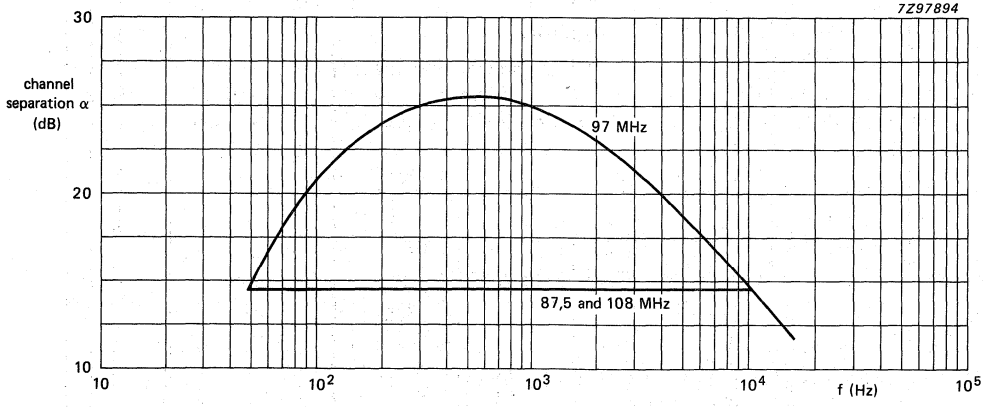


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

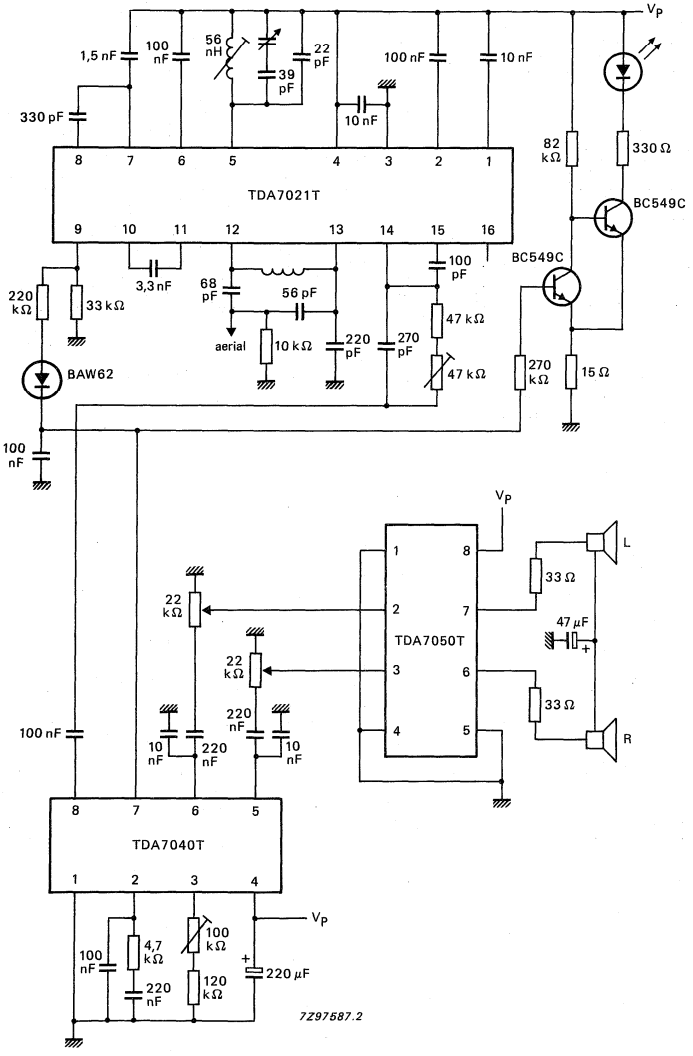


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

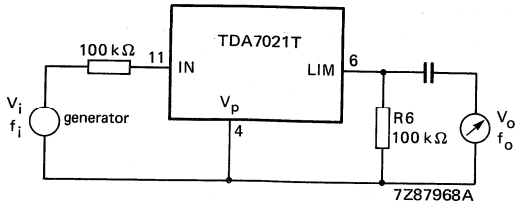


Fig. 9 Test set-up; V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\ \text{kHz} - f_i)}{V_o \mid f_i}$$

$$S_{-300} = 20 \log \frac{V_o \mid (300\ \text{kHz} + f_i)}{V_o \mid f_i}$$

LOW VOLTAGE MICRO TUNING SYSTEM (MTS)

GENERAL DESCRIPTION

The TDA7030T low voltage tuning system incorporates all analogue and digital functions necessary for complete control of a TDA7021T FM radio receiver. The tuning system coverage is precisely defined by an integrated 100 kHz crystal oscillator.

The complete low voltage radio receiver system comprises:

TDA7021T	Single-chip FM radio receiver;
TDA7030T	Low voltage micro tuning system;
TDA7040T	Low voltage stereo decoder;
TDA7050T	Low voltage stereo power amplifier.

Features

- Memory function with four presets and last-input recall
- Search tuning
- Integrating AFC
- 16-step stereo volume control
- On/off power switch driver
- On-chip interface for 16-point frequency scale LCD

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

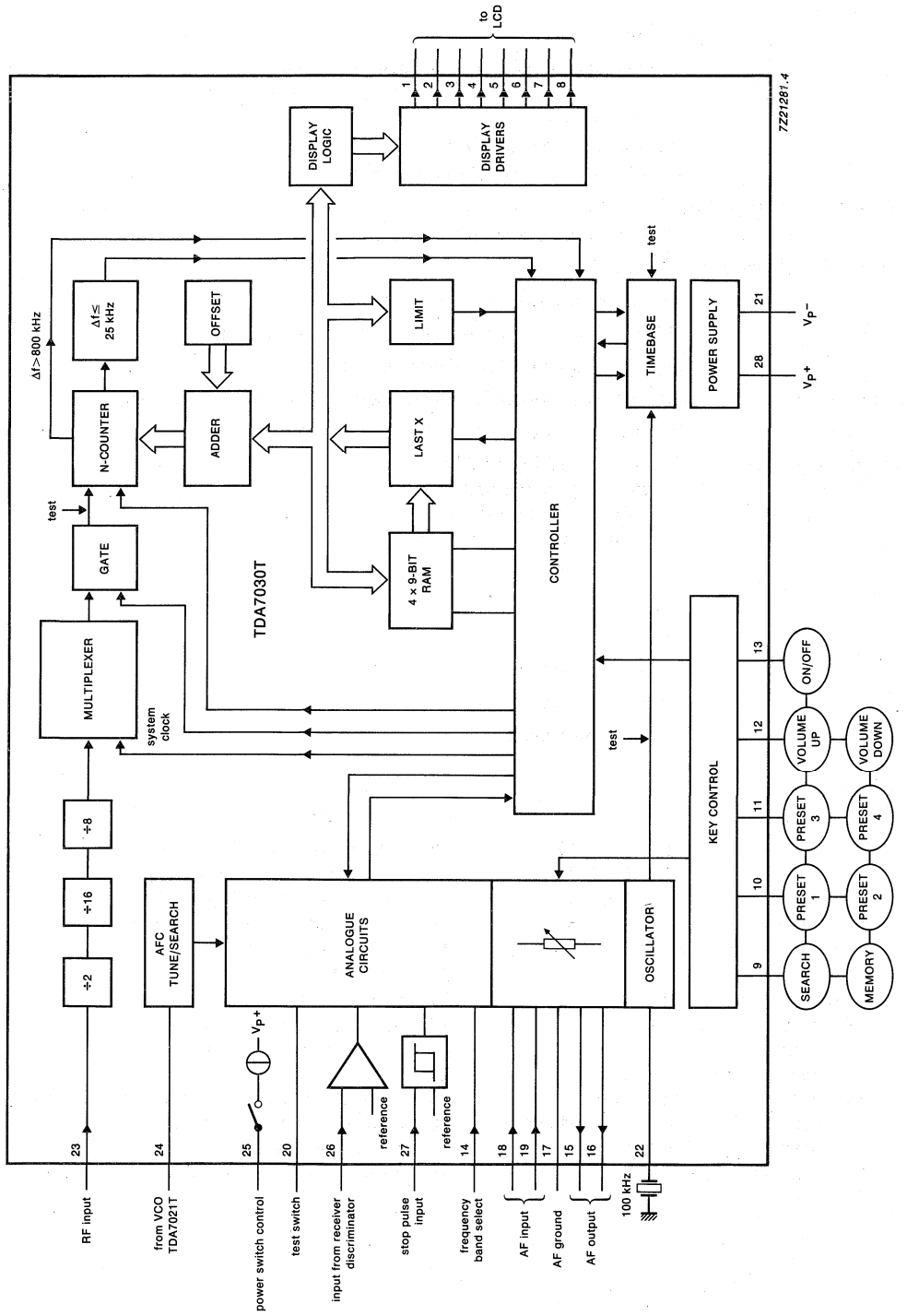


Fig. 1 Block diagram.

DEVELOPMENT DATA

Notes to Fig.1

Prescaler first stage (divide-by-2):

input frequency 75.925 to 89.925 MHz (Japan)
87.425 to 107.925 (Europe and USA)
sensitivity 80 mV
input impedance 2.5 kΩ/6 pF
prescaler turns on when radio is switched on

Prescaler second stage (divide-by-16):

current is only switched on for dividing

Prescaler third stage (divide-by-8):

current is only switched on for dividing

Multiplexer:	switches the clock for the N-counter (proportional tuning)
Gate:	gate time 10.24 ms (one digit = 25 kHz)
N-counter:	13-bit down-counter for tuned frequency (one digit = 25 kHz)
Frequency decoder:	supplies N-counter information to the controller
Tuning current control:	1) integrating AFC ± 800 nA 2) search tuning (50 nA) 3) tuning current (800 nA) 4) down-set current (350 μA)
Adder and offset:	allows the system to store information in 9 bits
RAM:	4 x 9-bit
Last X:	last memory and search tuning counter
Limit:	band limit controller
Display drivers:	outputs to drive a 4 x 4 LCD matrix
Controller:	controls the system

PINNING

pin	description	pin	description
1	LCD matrix: segments 3, 4, 11, 12	15	volume control: AF output right
2	LCD matrix: segments 2, 5, 10, 13	16	volume control: AF output left
3	LCD matrix: segments 1, 6, 9, 14	17	volume control: AF ground
4	LCD matrix: segments 0, 7, 8, 15	18	volume control: AF input right
5	LCD matrix: backplane 4	19	volume control: AF input left
6	LCD matrix: backplane 3	20	test switch
7	LCD matrix: backplane 2	21	negative supply voltage (V_P)
8	LCD matrix: backplane 1	22	oscillator crystal connection
9	key matrix: search/memory	23	RF input from receiver oscillator
10	key matrix: preset 1/preset 2	24	VCO tuning circuit
11	key matrix: preset 3/preset 4	25	current source for power switch transistor
12	key matrix: volume up/volume down	26	input from receiver discriminator
13	key matrix: on/off control	27	stop pulse/field strength
14	frequency band select	28	positive supply voltage (V_P)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 28)	$V_P = V_{28-21}$	−0.5	+ 7.0	V
Supply current (pin 21)	I_{21}	−10	+ 10	mA
AF ground current (pin 17)	I_{17}	−10	+ 10	mA
Input voltage (pins 9 to 16, 18 to 20 and 22 to 27)	V_I	−0.5	7.0	V
Input current (pins 9 to 16, 18 to 20 and 22 to 27)	I_I	–	1.0	mA
Output current (pins 9 to 16, 18 to 20 and 22 to 27)	I_O	–	−1.0	mA
Input voltage LCD matrix (pins 1 to 8)	V_I	−0.5	+ 5.0	V
Input current LCD matrix (pins 1 to 8)	I_I	–	1.0	mA
Output current LCD matrix (pins 1 to 8)	I_O	–	−1.0	mA
Total power dissipation	P_{tot}	–	35	mW
Operating ambient temperature range	T_{amb}	−10	+ 50	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{28-21} = 3$ V; $T_{amb} = 25$ °C; all voltages are referred to pin 21; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range for specified operation (pin 28)		V_P	1.8	3.0	4.0	V
Supply current	$V_P = 3$ V					
standby		I_P	–	25	–	μA
radio on (pin 25)	$I_{PCS} = 0$	I_P	–	3.0	–	mA
tuning		I_P	–	6.8	–	mA
LCD matrix (pins 1 to 8)						
Output voltage		V_{LCD}	see Fig.3			
Output sink current	$V_{LCD} = 2$ V	I_{sink}	20	–	–	μA
Output source current	$V_{LCD} = 0.2$ V	I_{source}	–4	–	–	μA
Key matrix (pins 9 to 13)						
ON/OFF	active = HIGH	V_{ON}	V_P–0.1	–	V_P	V
	testmode = LOW	V_{ON}	0	–	0.5	V
Output current	$V_{ON} = 0$ to 0.5 V	I_O	–	–0.5	–	μA
Input current	$V_{ON} = V_P$–0.1 V to V_P	I_I	–	0.5	–	μA
Radio ON		I_I	–	8	–	μA
Search, preset 1, preset 3, volume up						
Active	KEY = HIGH	V_{9-12}	V_P–0.1	–	–	V
Input current	$V_{KEY} = V_P$–0.1 V to V_P	I_I	–	1	–	μA
Memory, preset 2, preset 4, volume down						
Active	KEY = LOW	V_{9-12}	0	–	0.2	V
Output current	$V_{KEY} = 0$ to 0.2 V	I_O	–	–1	–	μA
Frequency band select (pin 14)	frequency band with respect to TDA7021 IF					
76 to 90 MHz		V_{14}	V_P–0.2	–	V_P	V
input current		I_{14}	–	1.0	–	μA
87.5 to 108 MHz		V_{14}	0	–	0.5	V
output current		I_{14}	–	–0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Volume control AF outputs (pins 15 and 16)						
Attenuation in 16 steps, maximum attenuation step 15	R_L = 20 kΩ	$A_{(max.)}$	–	45	–	dB
Minimum attenuation (step 0)	R_L = 20 kΩ	$A_{(min.)}$	–	0	–	dB
AF output impedance		Z_O	–	20	–	kΩ
Attenuation per step;						
steps 1 to 3		$A_{1\text{-}3}$	–	2	–	dB
steps 4 to 12		$A_{4\text{-}12}$	–	3	–	dB
steps 13 to 15		$A_{13\text{-}15}$	–	4	–	dB
Total harmonic distortion	$V_{in} < 65$ mVeff; 1 kHz	THD	–	1.5	–	%
	$V_{in} < 200$ mVeff; 1 kHz	THD	–	–	4	%
Signal-to-noise ratio	measured unweighted from 400 Hz to 15 kHz					
0 dB attenuation		(S+N)/N	–	60	–	dB
20 dB attenuation		(S+N)/N	–	52	–	dB
Volume control AF inputs (pins 18 and 19)						
AF input voltage (RMS value)	total harmonic distortion < 1%	$V_{i(rms)}$	–	–	80	mV
AF input impedance		Z_i	–	10	–	kΩ
Testmode switch (pin 20)						
Testmode		V_{20}	1.8	–	V_P	V
Operating		V_{20}	0	–	0.3	V
Crystal oscillator (pin 22)						
Crystal frequency		f_{osc}	–	100	–	kHz
Series resonance resistance		$R_{(res)}$	–	–	15	kΩ
Shunt capacitance		C_S	–	–	2.5	pF
DC output current		I_{22}	–	–0.5	–	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (pin 23)						
Input frequency		f	50	–	150	MHz
Minimum voltage for save operation between 76 to 110 MHz		$V_{(min.)}$	–	–	90	mV
Maximum input voltage		$V_{(max.)}$	500	–	–	mV
Input resistance		R_I	–	2.5	–	kΩ
Input capacitance		C_I	–	6	–	pF
VCO tuning current (pin 24)						
AFC off		I_{24}	–	0	–	μA
RF down set	V_{28}-V_{24} > 0.2 V					
V_P = 3 V		I_{24}	–350	–	–	μA
V_P = 1.8 V		I_{24}	–150	–	–	μA
V_P = 5 V		I_{24}	–650	–	–	μA
RF tuning		I_{24}	–	800	–	nA
RF search		I_{24}	–	50	–	nA
AFC transconductance	$V_{26} = V_{28\text{-}26}$	g_m	–	5	–	nA/mV
Maximum source current		I_{source}	–800	–	–	nA
Maximum sink current		I_{sink}	800	–	–	nA
Power switch current source (pin 25)						
Minimum source current	V_{25} < 1 V	I_{25}	–500	–	–	μA
Receiver discriminator (pin 26)						
Input voltage	I_{24} = 0 μA	V_{26}	V_P–315	V_P–300	V_P–285	mV
Voltage when pin 26 acts as a voltage source		V_{26}	–	V_P–300	–	mV
Source current		I_{source}	–100	–	–	μA
Sink current		I_{sink}	50	–	–	μA
Stop pulse/field strength input (pin 27)						
Field strength detected		V_{27}	V_P–450	V_P–400	V_P–350	mV
No field strength detected		V_{27}	V_P–850	V_P–800	V_P–750	mV

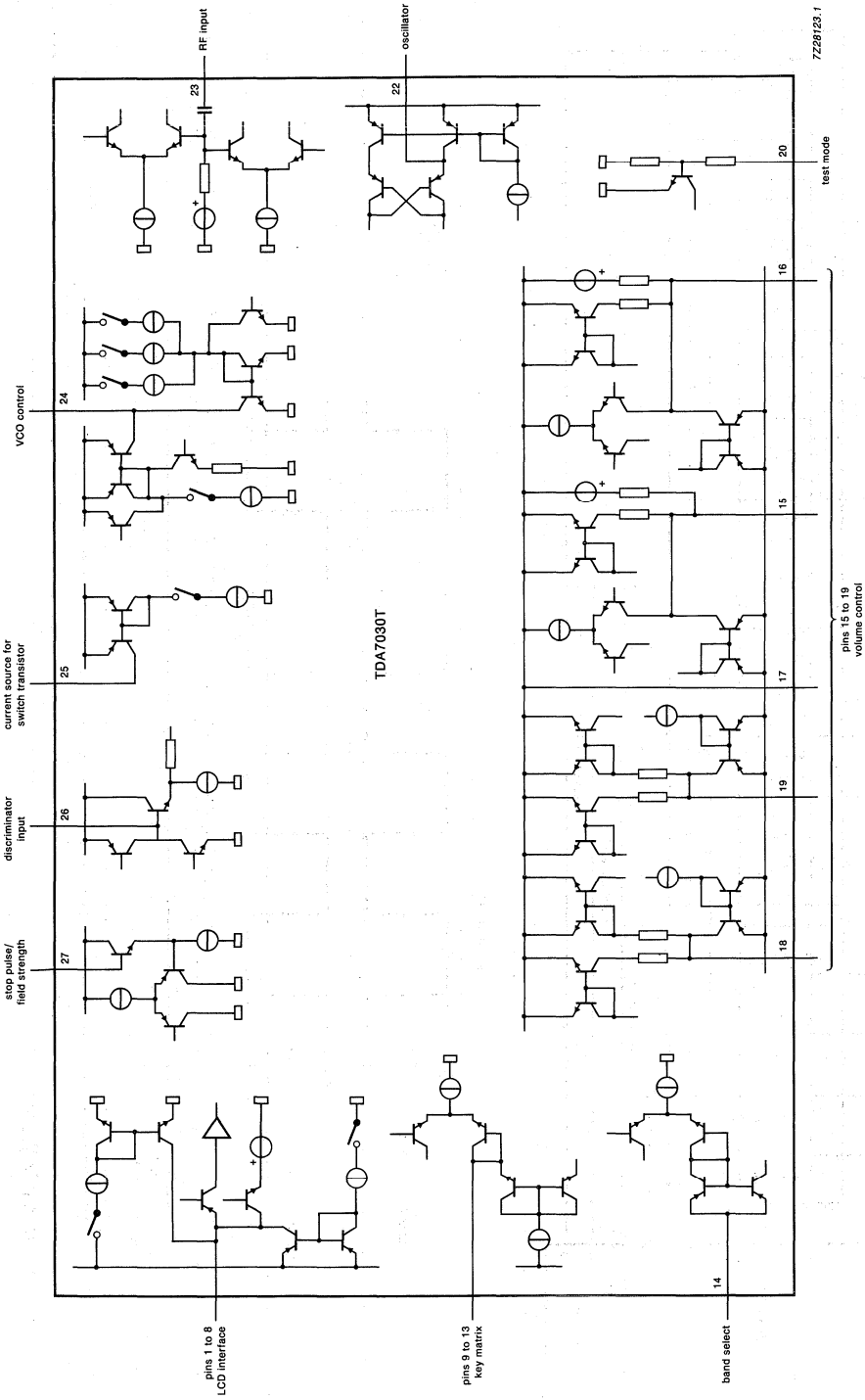
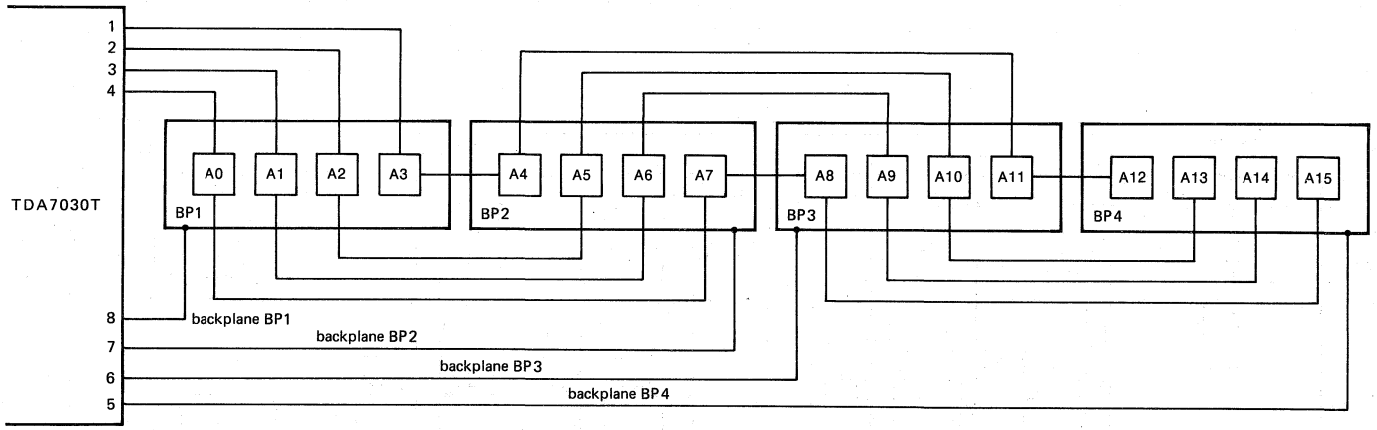
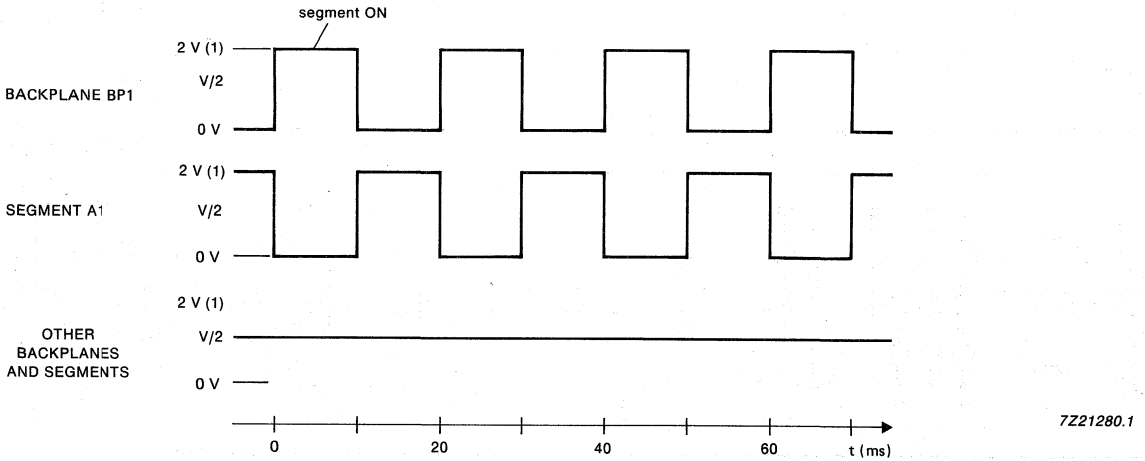


Fig.2 Pin interface diagram.

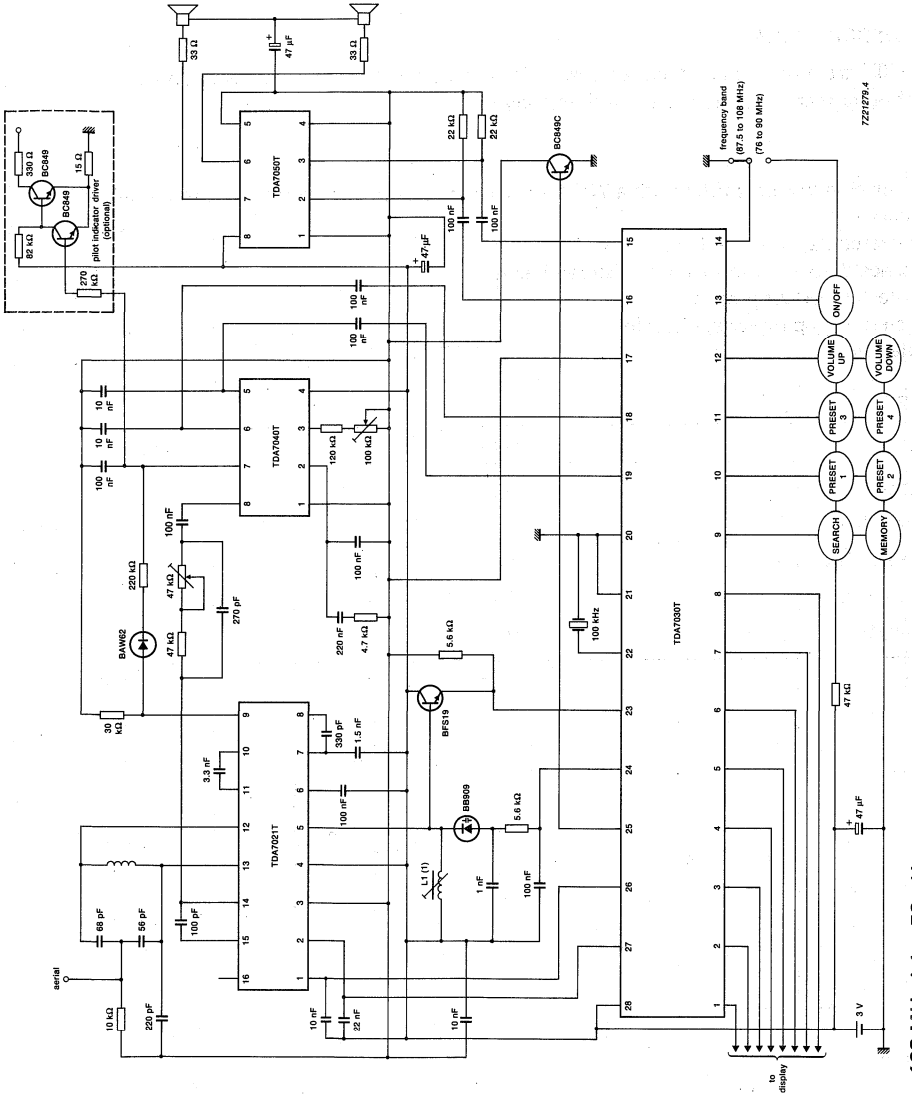
DEVELOPMENT DATA





(1) $V_p \geqslant 2.2$ V

Fig.3 LCD matrix with waveforms showing drive for segment S1.



(1) From 87.5 to 108 MHz L1 = 52 nH
From 76 to 90 MHz L1 = 69 nH

Fig.4 System application using the TDA7030T in conjunction with the single-chip FM radio receiver (TDA7021T), low voltage stereo decoder (TDA7040T) and low voltage stereo power amplifier (TDA7050T).

LOW VOLTAGE PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA7040T is a monolithic integrated circuit for low cost FM stereo radios with an absolute minimum of peripheral components and a simple lay-out.

Features

- Built-in four pole low pass filter with a 70 kHz corner frequency suppressing unwanted out-of-band input signals
- Fully integrated 228 kHz oscillator
- Pilot presence detector and soft mono/stereo blend
- Built-in interference suppression
- External stereo lamp driver applicable
- Adjustable gain

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current V_P = 3 V	I_P	–	3	–	mA
Total harmonic distortion	THD	–	0,3	–	%
Signal to noise ratio	S/(S + N)	–	70	–	dB
Channel separation	α	–	40	–	dB

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

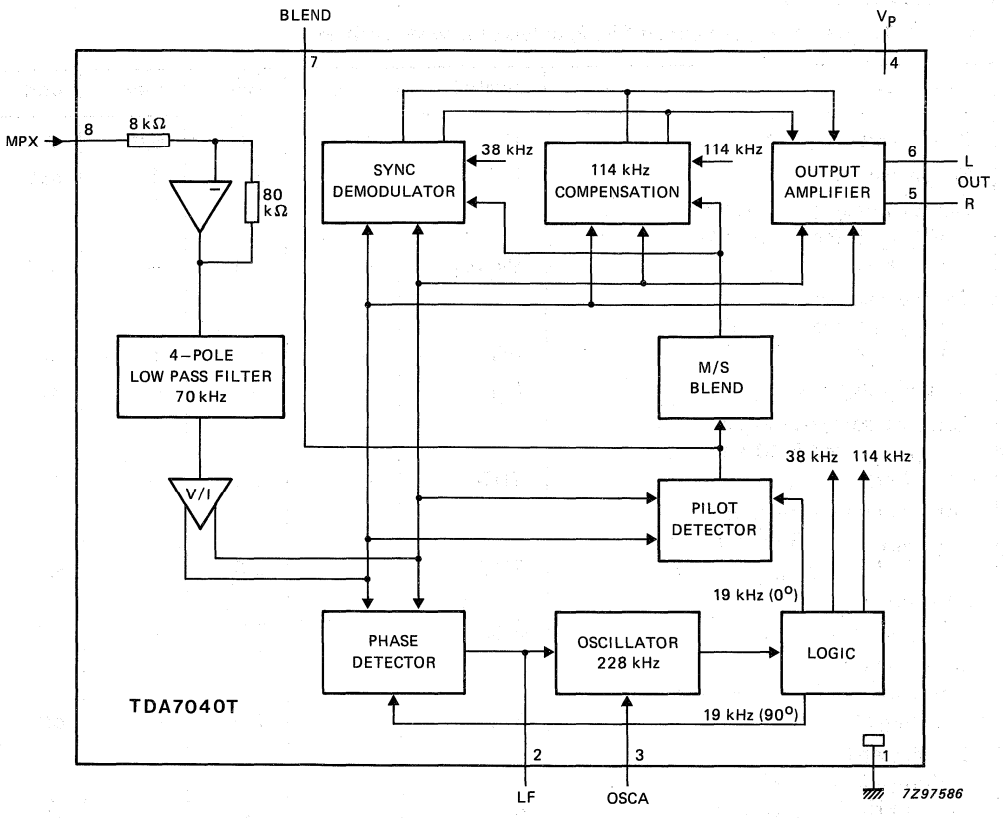


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	–	–	7	V
Operating ambient temperature	T_{amb}	−10	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	3,0	6,0	V
Supply current	I_P	–	3	4	mA
Output voltage (r.m.s. value) $V_{i(rms)}$ L and R 120 mV; f = 1 kHz	$V_{5,\,6\text{-}1}$	–	240	–	mV
Channel balance $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	ΔG_v	–	0	1	dB
Output resistance	R_O	–	5	–	kΩ
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	THD	–	0,1	–	%
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	THD	–	0,3	–	%
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz	S/(S + N)	–	70	–	dB
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz $V_{p(rms)}$ = 12 mV	S/(S + N)	–	70	–	dB
Channel separation $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	α	–	40	–	dB
Capture range $V_{p(rms)}$ = 12 mV; deviation from centre frequency	Δf	–	± 3	–	%
Carrier leak $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz;					
f = 19 kHz		–	30	–	dB
f = 38 kHz		–	50	–	dB
SCA (Subsidiary Communications Authorization) rejection $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{SCA(RMS)}$ = 12 mV; f = 67 kHz	α_{67}	–	70	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
ACI (Adjacent channel interference) $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{ACI(RMS)}$ = 1,3 mV; f = 114 kHz $V_{ACI(RMS)}$ = 1,3 mV; f = 190 kHz	α_{114} α_{119}	– –	90 85	– –	dB dB
Traffic radio (V.W.F.) suppression $\alpha_{57(VWF)} = \frac{V_{o(signal)} \text{ (at 1 kHz)}}{V_{o(spurious)} \text{ (at 1 kHz} \pm \text{23 Hz)}}$ measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%)	$\alpha_{57(VWF)}$	–	75	–	dB

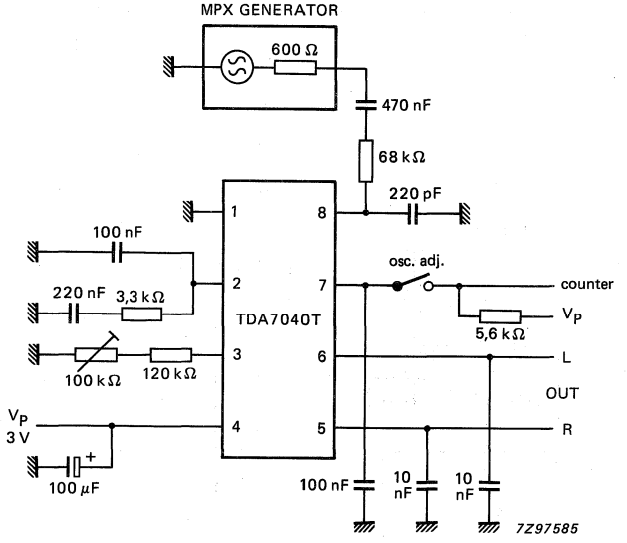


Fig. 2 Test circuit.

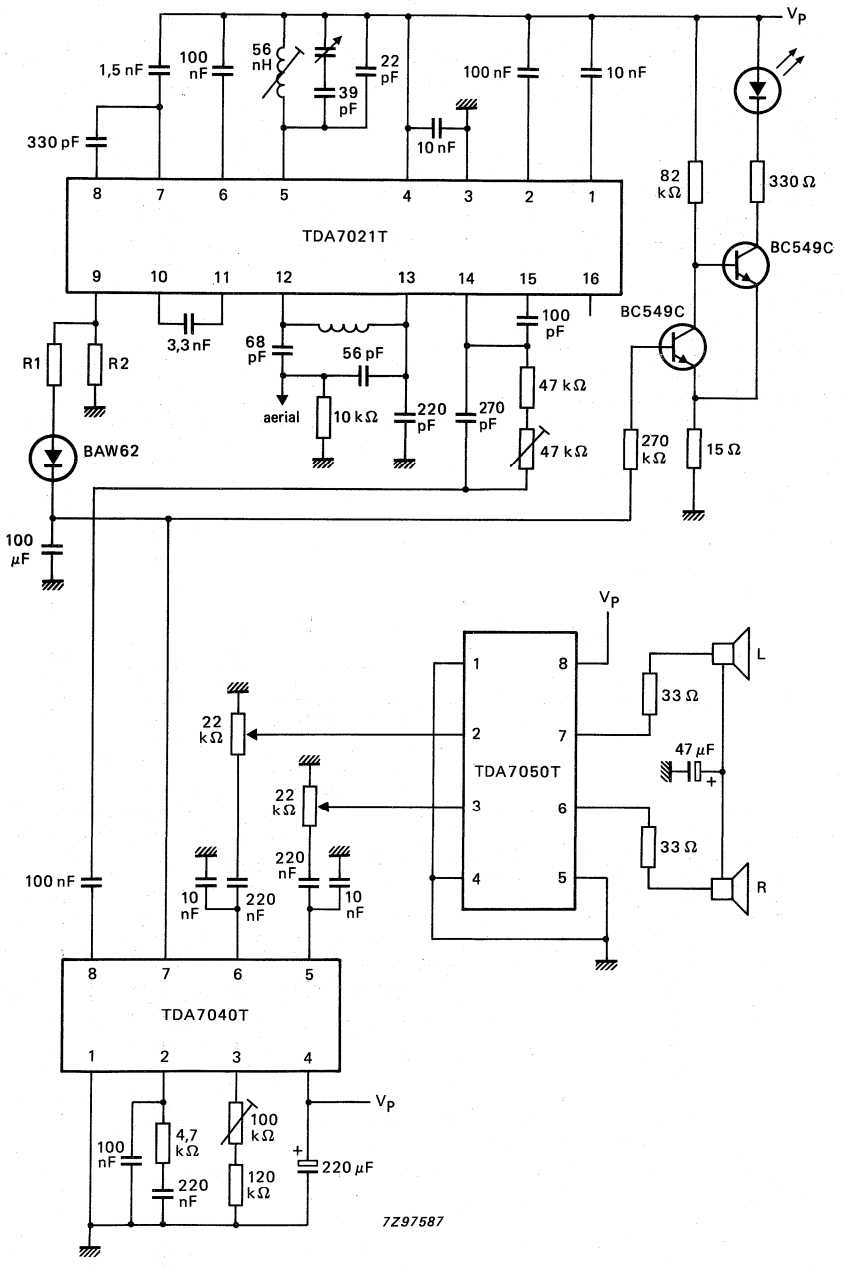


Fig. 3 Application diagram in combination with TDA7021T and TDA7050T.

CHARACTERISTICS

Of the combination TDA7021T, TDA7040T and TDA7050T (Fig. 3).
Conditions unless otherwise specified: $V_{vhf(rms)}$ = 1 mV; f_{hf} = 97 MHz; f_{dev} = 22,5 kHz; $f_{dev\ pilot}$ = 6,75 kHz; noise measured unweighted in a range from 400 Hz to 15 kHz.

parameter	symbol	min.	typ.	max.	unit
Total harmonic distortion (pilot on)					
V_i = (L + R) signal; f_{mod} = 1 kHz	THD	–	0,5	–	%
V_i = L signal; f_{mod} = 1 kHz	THD	–	1,0	–	%
Signal to noise ratio					
V_i = (L + R) signal; f_{mod} = 1 kHz					
pilot off	S/(S + N)	–	56	–	dB
pilot on	S/(S + N)	–	50	–	dB
Channel separation					
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 97 MHz	α	–	26	–	dB
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 87,5 MHz and 108 MHz	α	–	14	–	dB
Output voltage (pilot off)					
V_i = (L + R) signal, f_{mod} = 1 kHz	$V_{o(rms)}$	–	80	–	mV

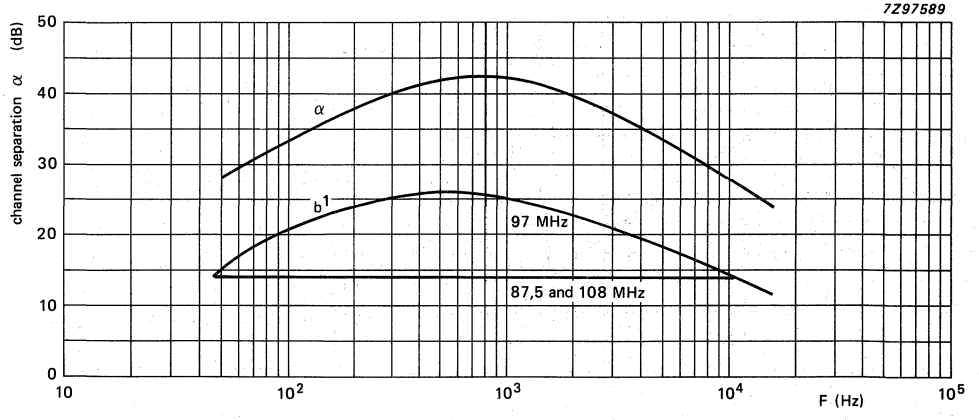


Fig. 4 Channel separation as a function of audio frequency.
a = measured in test circuit (Fig. 2)
b = measured in application diagram (Fig. 3)

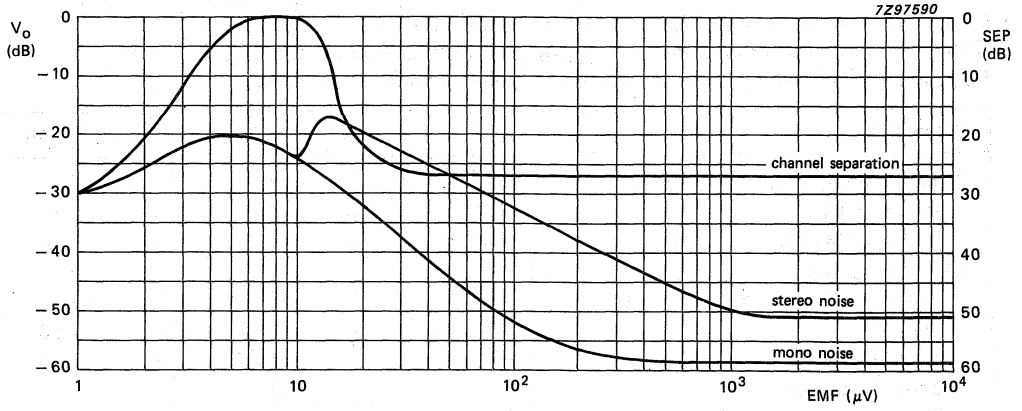


Fig. 5 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 270 kΩ and R2 = 13 kΩ; without diode BAW62.

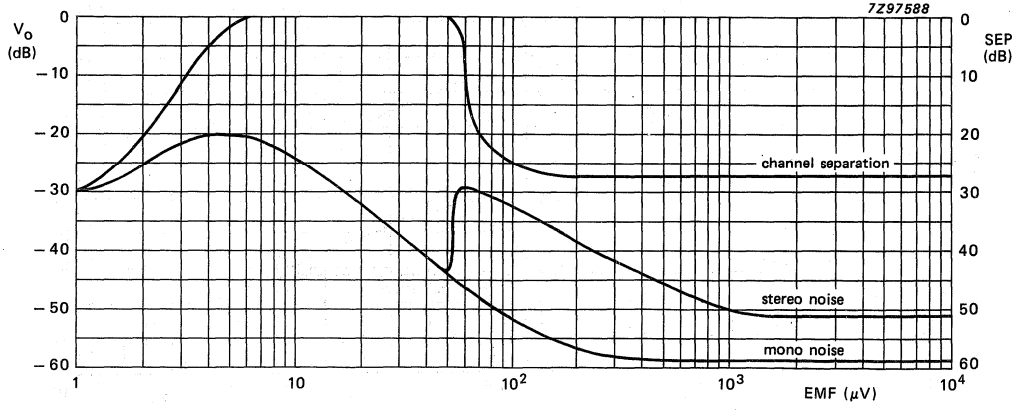


Fig. 6 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 200 kΩ, R2 = 30 kΩ; with diode BAW62.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

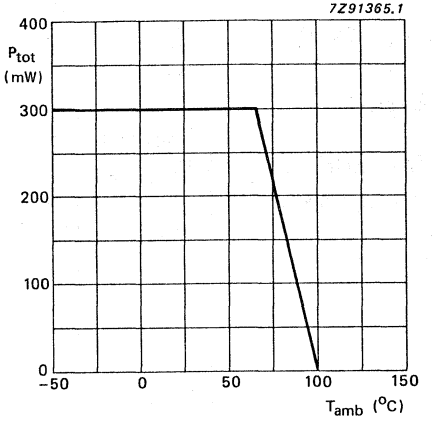


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

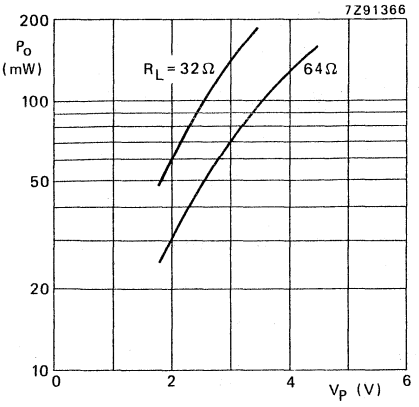


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

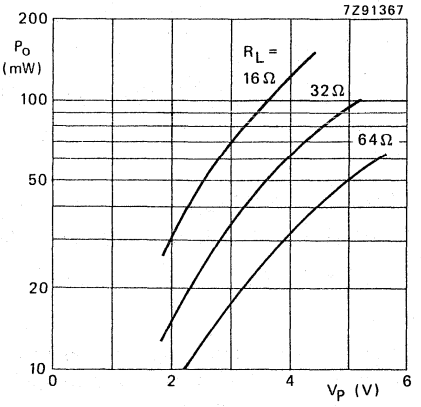


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

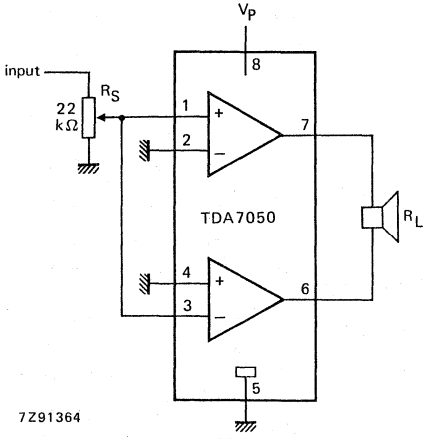


Fig. 4 Application diagram (BTL); also used as test circuit.

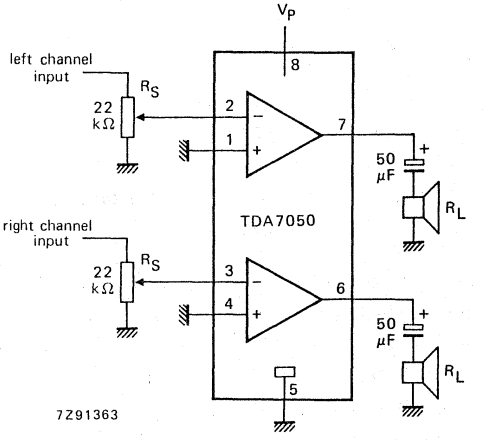


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

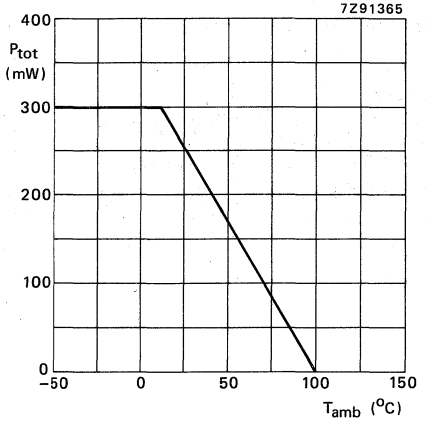


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

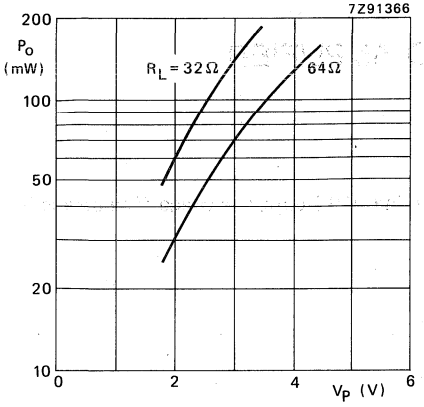


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

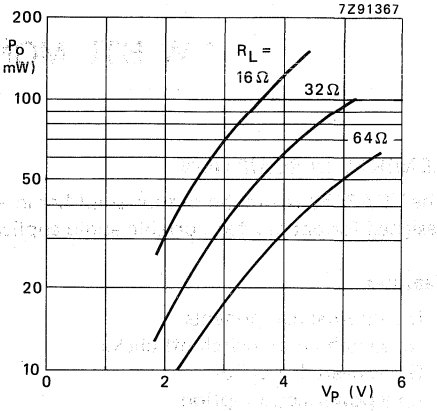


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

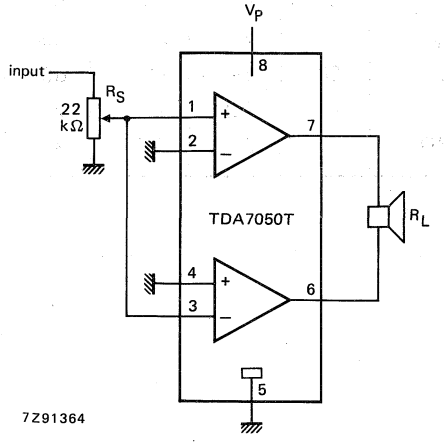


Fig. 4 Application diagram (BTL); also used as test circuit.

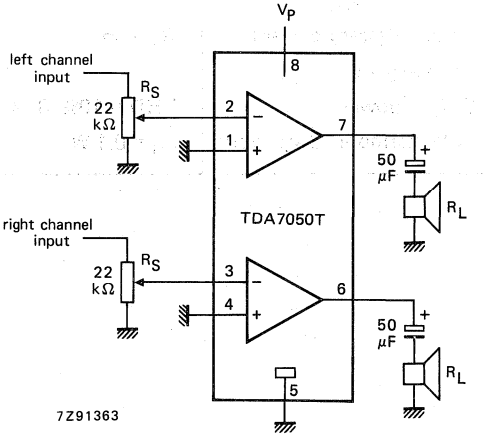


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

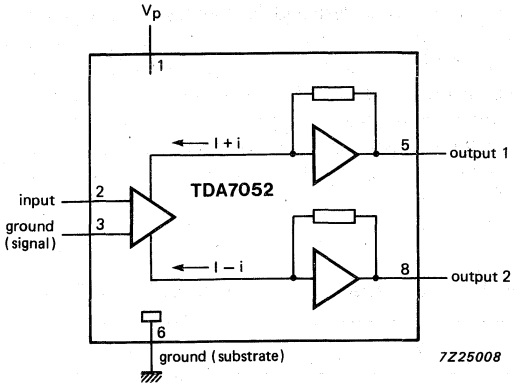


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−55	+150	°C

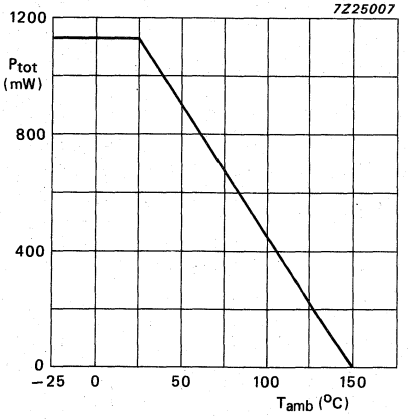


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%	P_o	–	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

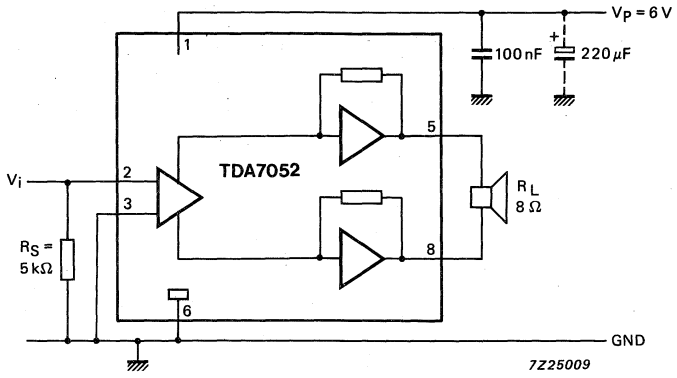


Fig. 3 Application diagram.

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	$R_L = 8\ \Omega$; $V_P = 6$ V	1.0	1.1	–	W
	TDA7052AT	$R_L = 16\ \Omega$; $V_P = 6$ V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	$P_O = 0.5$ W	–	0.3	1	%
	TDA7052AT	$P_O = 0.25$ W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

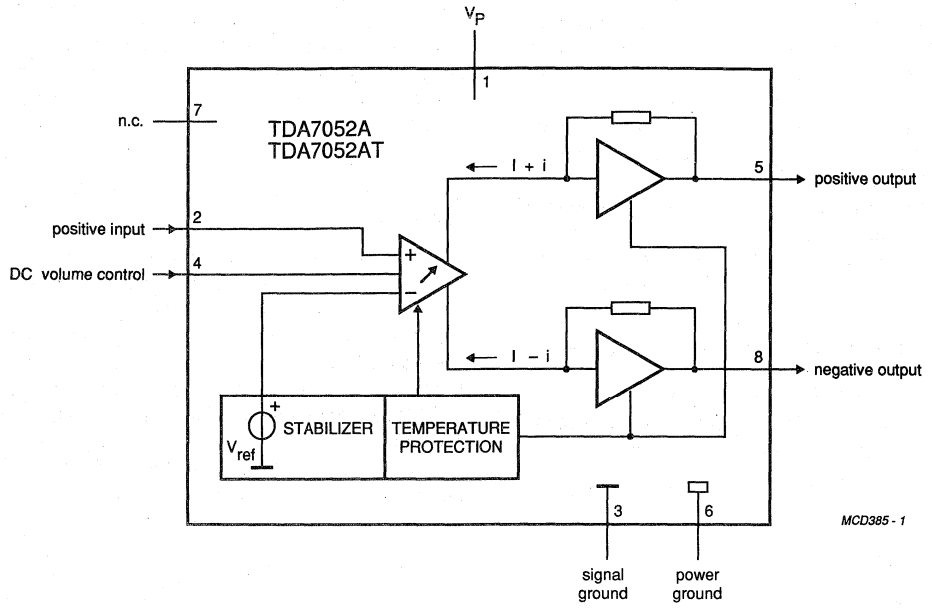


Fig.1 Block diagram.

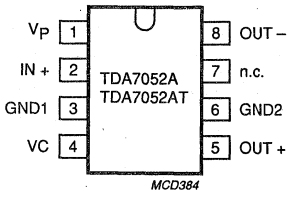


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 35.5 dB to –44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, so the output power is reduced.
Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\%$			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.8	W
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052A	100 K/W
	TDA7052AT	155 K/W

Note to the thermal resistance

TDA7052A: $V_P = 6$ V; $R_L = 8\ \Omega$. The maximum sine-wave dissipation is 0.9 W. Therefore $T_{amb(max)} = 150 - 100 \times 0.9 = 60$ °C.
TDA7052AT: $V_P = 6$ V; $R_L = 16\ \Omega$. The maximum sine-wave dissipation is 0.46 W. Therefore $T_{amb(max)} = 150 - 155 \times 0.46 = 78$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7052A: R_L = 8 Ω; TDA7052AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞ note 1	–	7	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power	THD = 10%				
	TDA7052A		1.0	1.1	–	W
	TDA7052AT		0.5	0.55	–	W
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_4 = 0.8 V; THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	–1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\|V_{off}\|$	DC output offset voltage		–	0	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_4 \leq 0.3$ V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

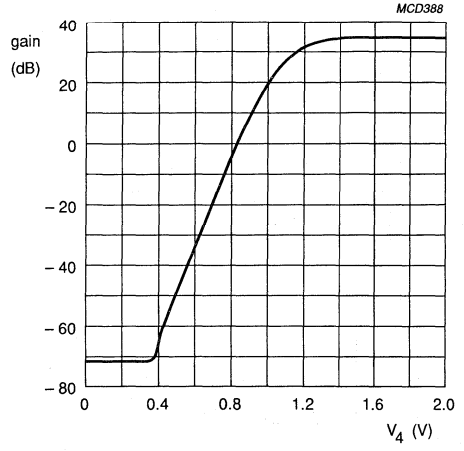


Fig.3 Gain control as a function of DC volume control.

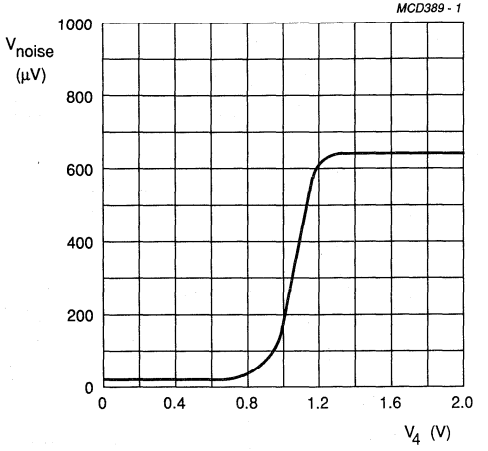


Fig.4 Noise output voltage as a function of DC volume control.

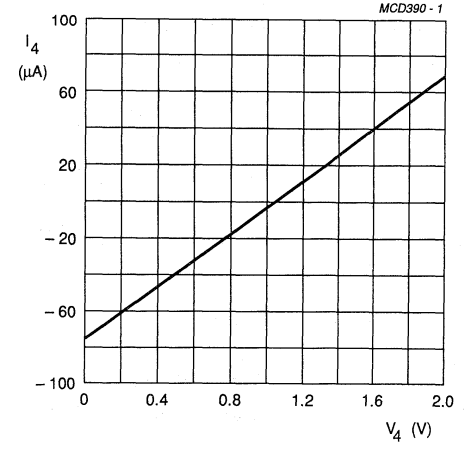
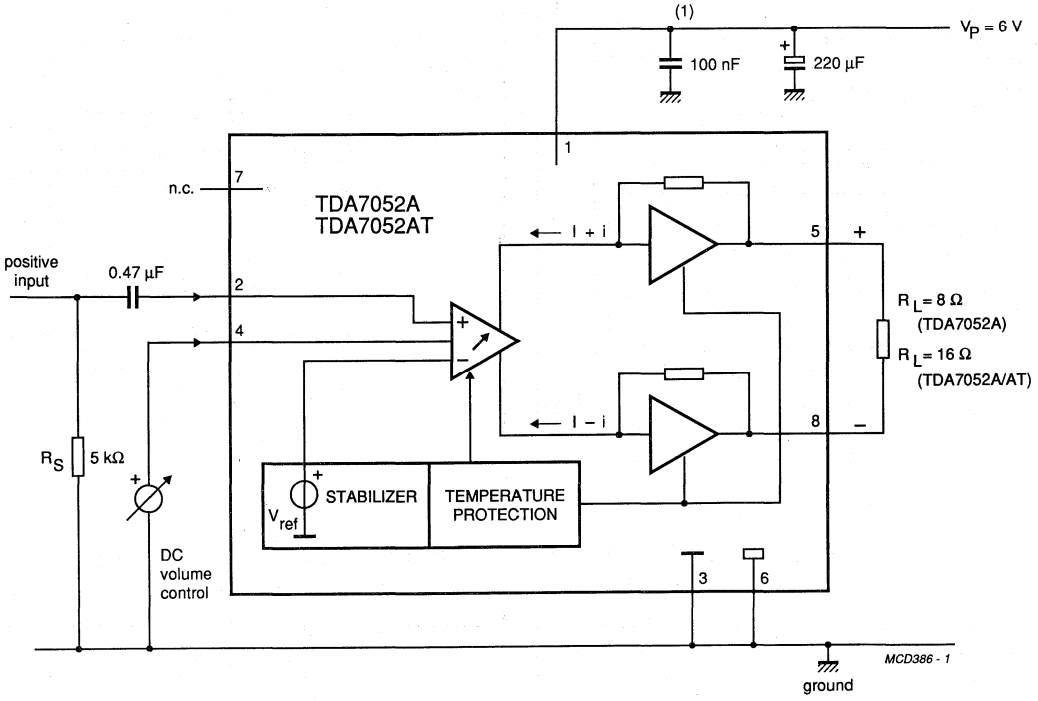


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

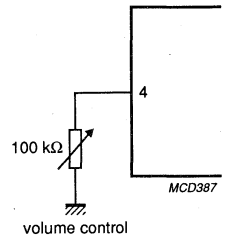


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_v	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

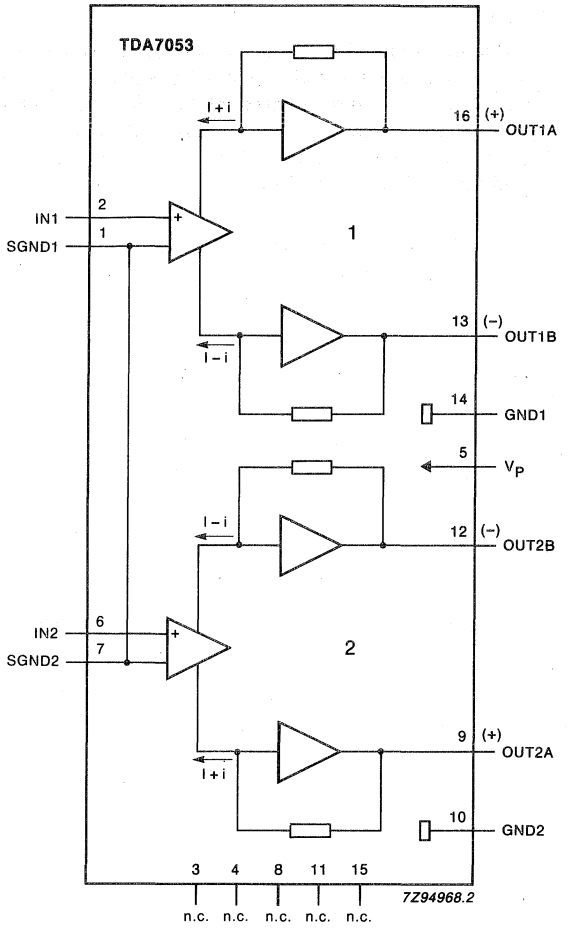


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

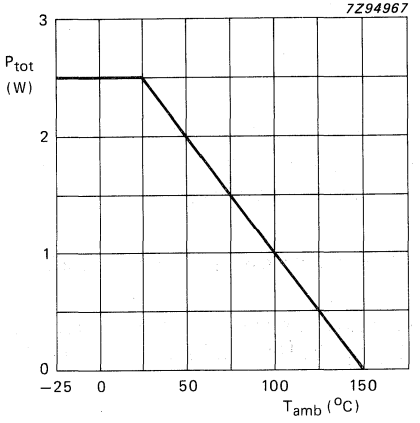


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	R_L = ∞; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_V	38	39	40	dB
Channel balance		ΔG_V	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

APPLICATION INFORMATION

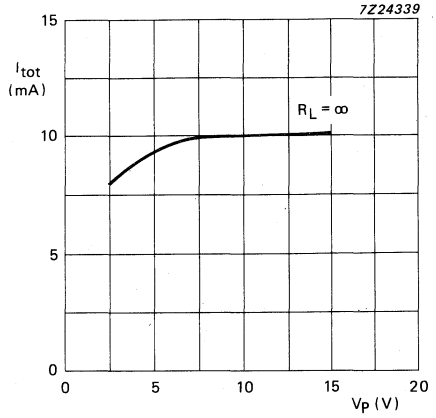


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

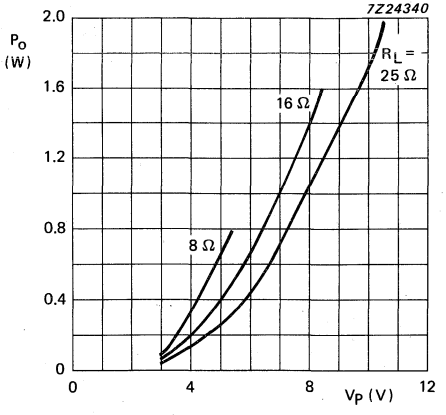
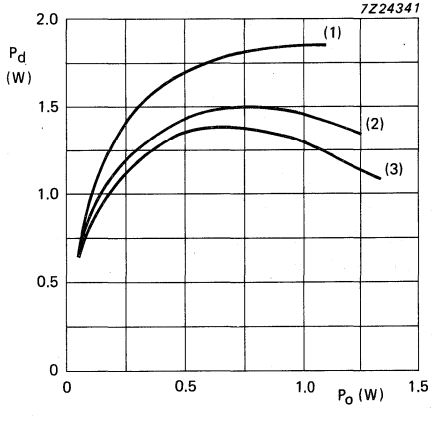
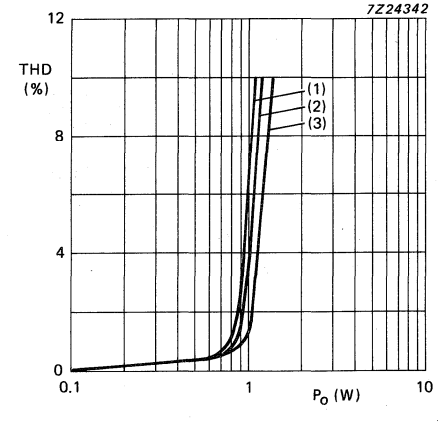


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

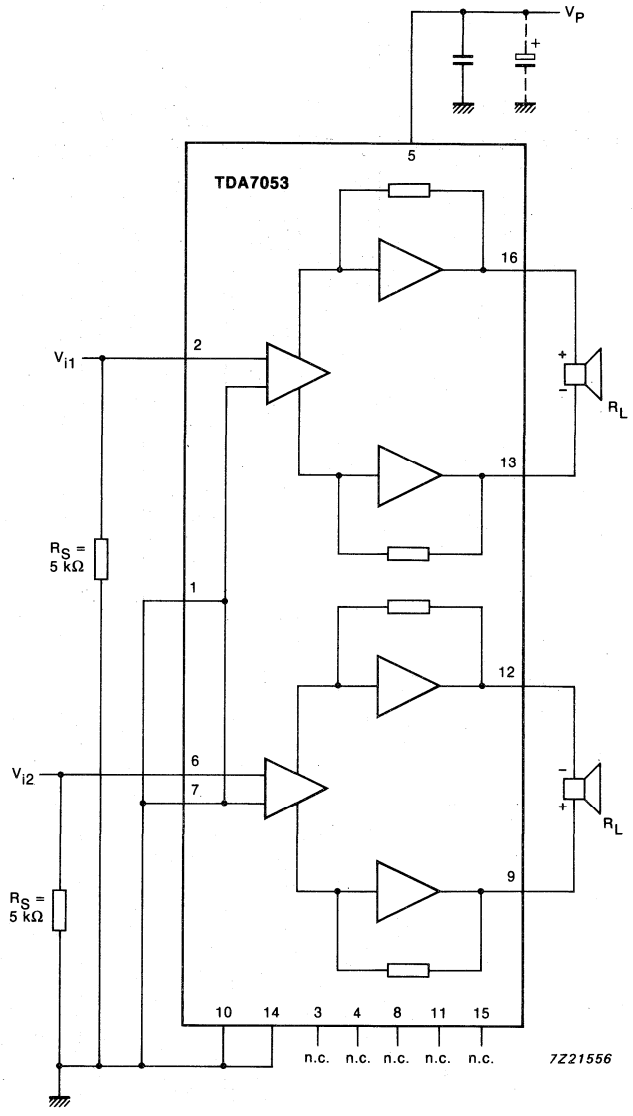


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

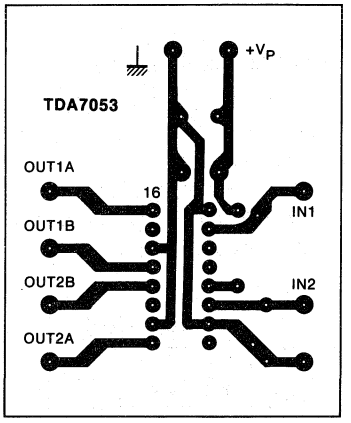


Fig. 8 Printed-circuit board, track side.

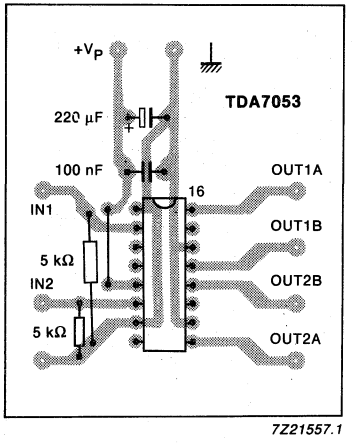


Fig. 9 Printed-circuit board, component side.

Data sheet	
status	Product specification
date of issue	May 1992

TDA7056

3 Watt mono BTL audio output amplifier

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	2.5	3	-	W
G_V	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110

3 Watt mono BTL audio output amplifier TDA7056

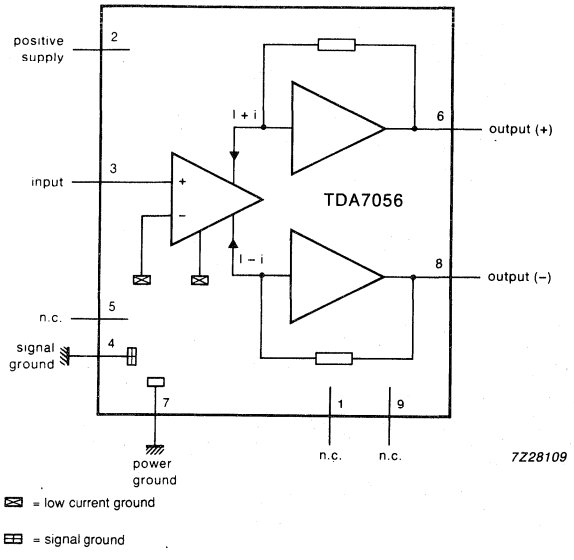


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (-)
9	n.c.

FUNCTIONAL DESCRIPTION

The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television.
For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.
The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		-	18	V
I_{ORM}	Peak output current repetitive		-	1	A
I_{OSM}	Peak output current non-repetitive		-	1.5	A
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C
P_{tot}	total power dissipation	$T_{case} < 60$ °C	-	9	W
T_{sc}	short circuiting time	see note	-	1	hr

Note

The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	NOM.	UNIT
$R_{th\ j\text{-}c}$	from junction to case	10	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	K/W

POWER DISSIPATION

Assume: $V_P = 11$ V; $R_L = 16\ \Omega$.

The maximum sine-wave dissipation is 1.52 W.

The $R_{th\ j\text{-}a}$ of the package is 55 K/W.

T_{amb} max = 150 - 55 x 1.52 = 66.4 °C.

CHARACTERISTICS

At T_{amb} = 25 °C; f = 1 kHz; V_P = 11 V; R_L = 16 Ω (see Fig.2)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		3	11	18	V
I_{ORM}	repetitive peak output current		-	-	0.6	A
I_P	total quiescent current	note 1 $R_L = \infty$	-	5	7	mA
P_O	output power	THD = 10%	2.5	3	-	W
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%
G_v	voltage gain		39	40.5	42	dB
V_{no}	noise output voltage	note 2	-	180	300	μV
V_{no}	noise output voltage	note 3	-	60	-	μV
	frequency response		-	20 to 20.000	-	Hz
RR	ripple rejection	note 4	36	50	-	dB
ΔV	DC-output offset voltage	note 5	-	-	200	mV
$\|Z_i\|$	input impedance		-	100	-	kΩ
I_i	input bias current		-	100	300	nA

Notes to the characteristics

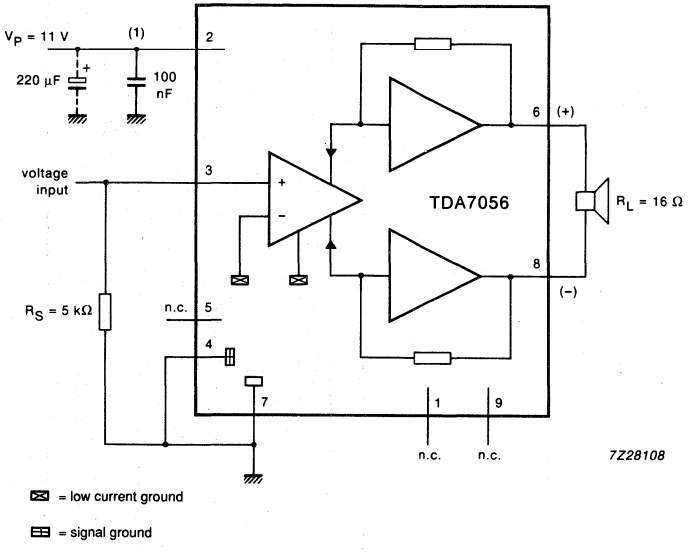
1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.

2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).

3. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz. With a practical load (R_L = 16 Ω, L_L = 200 μH) the noise output current is only 50 nA.

4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.

5. R_S = 5 kΩ



(1) This capacitor can be omitted if the supply electrolytic capacitor is placed closer to pin 2.

Fig.2 Test and application diagram.

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power	R_L = 16 Ω; V_P = 12 V	3	3.5	–	W
G_v	voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	8	16	mA
THD	total harmonic distortion	V_P = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

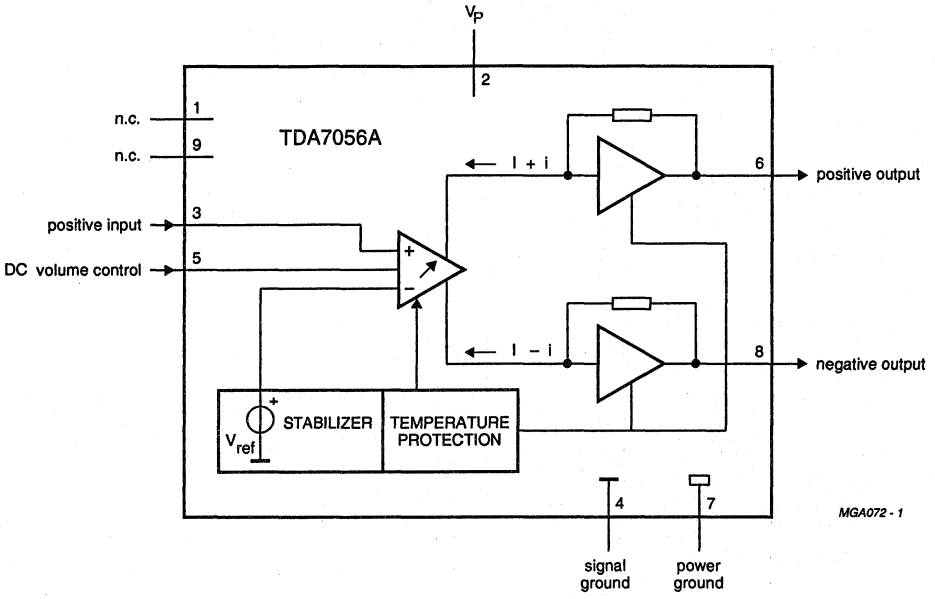


Fig.1 Block diagram.

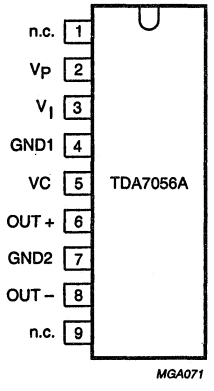


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FUNCTIONAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but also suitable for battery-fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitor to keep the offset voltage low.
In the TDA7056A the DC volume stage is integrated into the input stage so that coupling capacitors are not required and a low offset voltage is maintained.
At the same time the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- lower peak value of the supply current
- the frequency of the ripple on the supply voltage is twice the signal frequency

Thus, a reduced power supply and smaller capacitors can be used which results in cost savings.
For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB.
The DC volume control stage has a logarithmic control characteristic.
The total gain can be controlled from 35.5 dB to –44 dB.
If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	9	W
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_3	input voltage pin 3		–	8	V
V_5	input voltage pin 5		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55 K/W
$R_{th\ j\text{-}c}$	from junction to case	10 K/W

Note to the thermal resistance

V_P = 12 V; R_L = 16 Ω; The maximum sine-wave dissipation is = 1.8 W. The $R_{th\ vj\text{-}a}$ of the package is 55 K/W; $T_{amb\ (max)}$ = 150 – 55 x 1.8 = 51 °C

CHARACTERISTICS

V_P = 12 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified (see Fig.6)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 12 V; R_L = ∞; note 1	–	8	16	mA
Maximum gain (V_5 = 1.4 V)						
P_O	output power					
		THD = 10%; R_L = 16 Ω	3	3.5	–	W
		THD = 10%; R_L = 8 Ω	–	5.2	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_5 = 0.8 V;THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at −1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\|V_{off}\|$	DC output offset voltage		–	0	150	mV
Z_I	input impedance pin 3		15	20	25	kΩ
Minimum gain (V_5 = 0.5 V)						
G_v	voltage gain		–	−44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_5 \leq$ 0.3 V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_5	control current	V_5 = 0 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

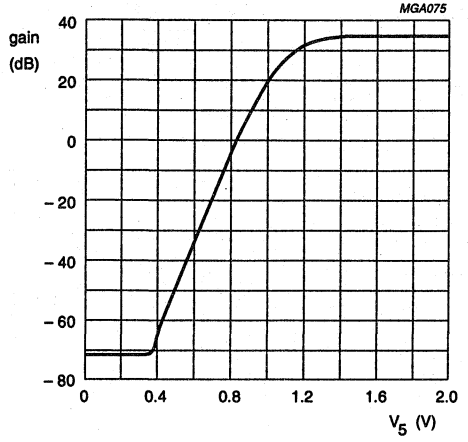


Fig.3 Gain as a function of DC volume control.

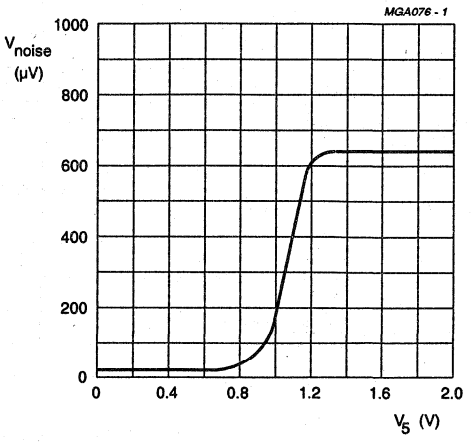


Fig.4 Noise output voltage as a function of DC volume control.

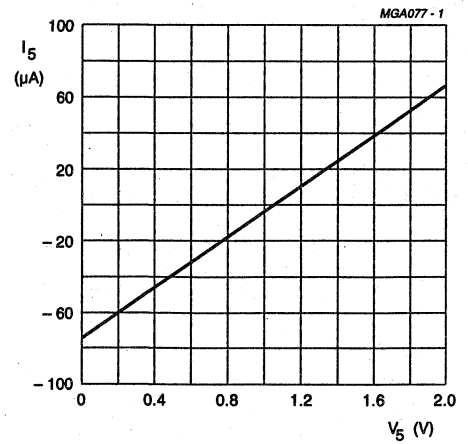
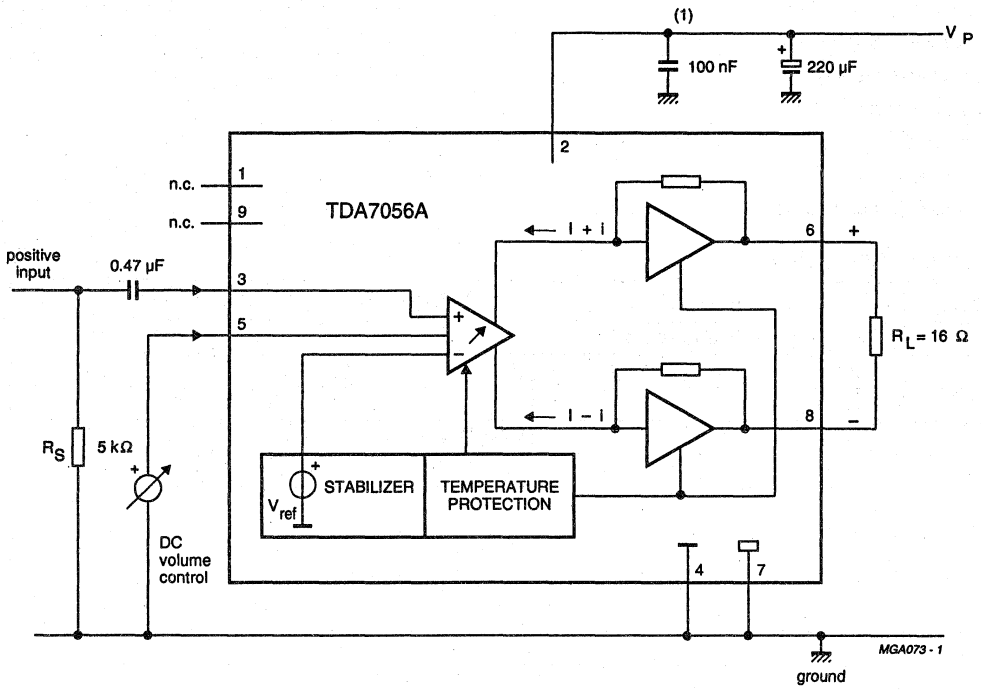


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 2.

Fig.6 Test and application diagram.

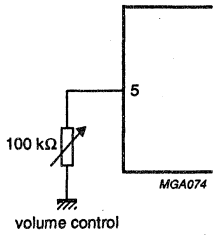


Fig.7 Application using a potentiometer for volume control; G_v = 30 dB.

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

FEATURES

- No external components
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Short-circuit proof
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057Q is a stereo output amplifier in a 13 pin power package. The device is designed for battery-fed portable stereo recorders and radios, but also suitable for mains-fed applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
P_O	output power	V_P = 11 V; R_L = 16 Ω	–	3	–	W
G_v	voltage gain		39	40	41	dB
I_P	total quiescent current	V_P = 11 V; R_L = ∞	–	10	14	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057Q	13	SBD	plastic	SOT141

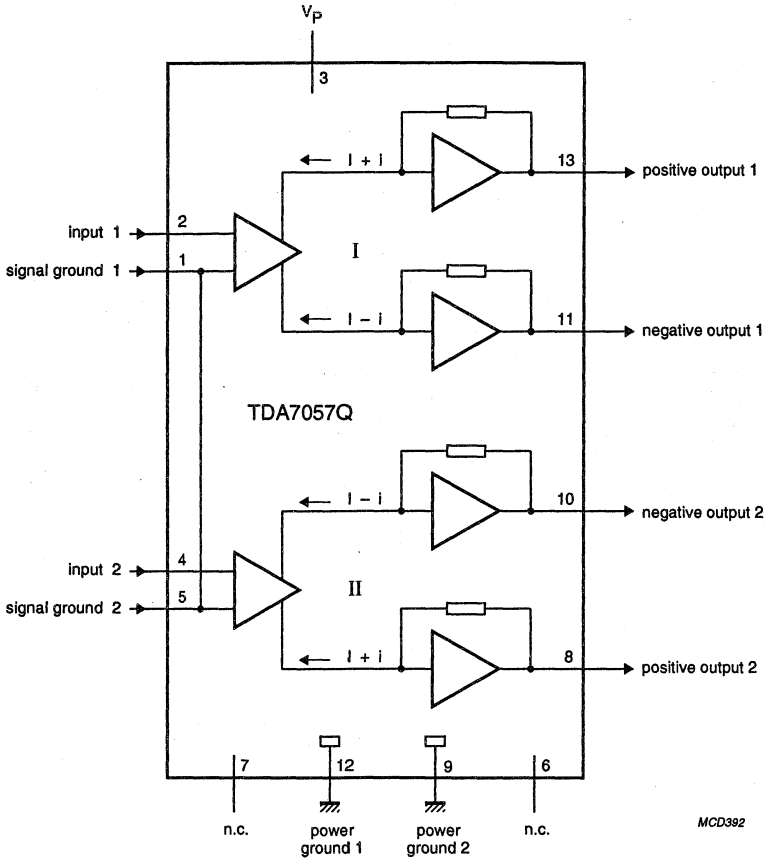


Fig.1 Block diagram.

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

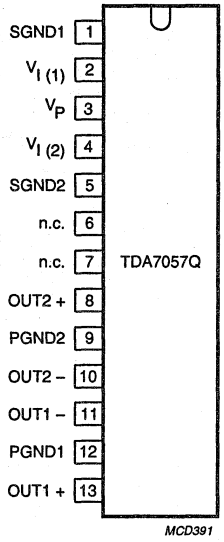


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
SGND1	1	signal ground 1
$V_{I(1)}$	2	voltage input 1
V_P	3	positive supply voltage
$V_{I(2)}$	4	voltage input 2
SGND2	5	signal ground 2
n.c.	6	not connected
n.c.	7	not connected
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2−	10	negative output 2
OUT1−	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

FUNCTIONAL DESCRIPTION

The TDA7057Q is a stereo output amplifier, designed for battery-fed applications e.g. portable radios, but also suitable for mains fed applications. The gain is internally fixed at 40 dB.

For space reason there is a trend to decrease the number of battery cells. This means a decrease in supply voltage, resulting in a reduction of output power at conventional output stages. The latter is not preferred. Using the BTL principle increases the output power.

The TDA7057Q can deliver an output power of 3 W in a speaker load of 16 Ω with 11 V supply.

The circuit is designed such that no external components are required. Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability. The load can be short-circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60$ °C	–	9	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	45 K/W
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

Note to the thermal resistance

$V_P = 11$ V; $R_L = 16\ \Omega$; The maximum sine-wave dissipation is = 3 W; $T_{amb\ (max)} = 60$ °C; $R_{th\ vj\text{-}a} = (150 - 60)/3 = 30$ K/W

$R_{th\ vj\text{-}a} = R_{th\ vj\text{-}c} + R_{th\ c\text{-}HS} + R_{th\ HS}$

$R_{th\ c\text{-}HS} + R_{th\ HS} = 30 - 8 = 22$ K/W

CHARACTERISTICS

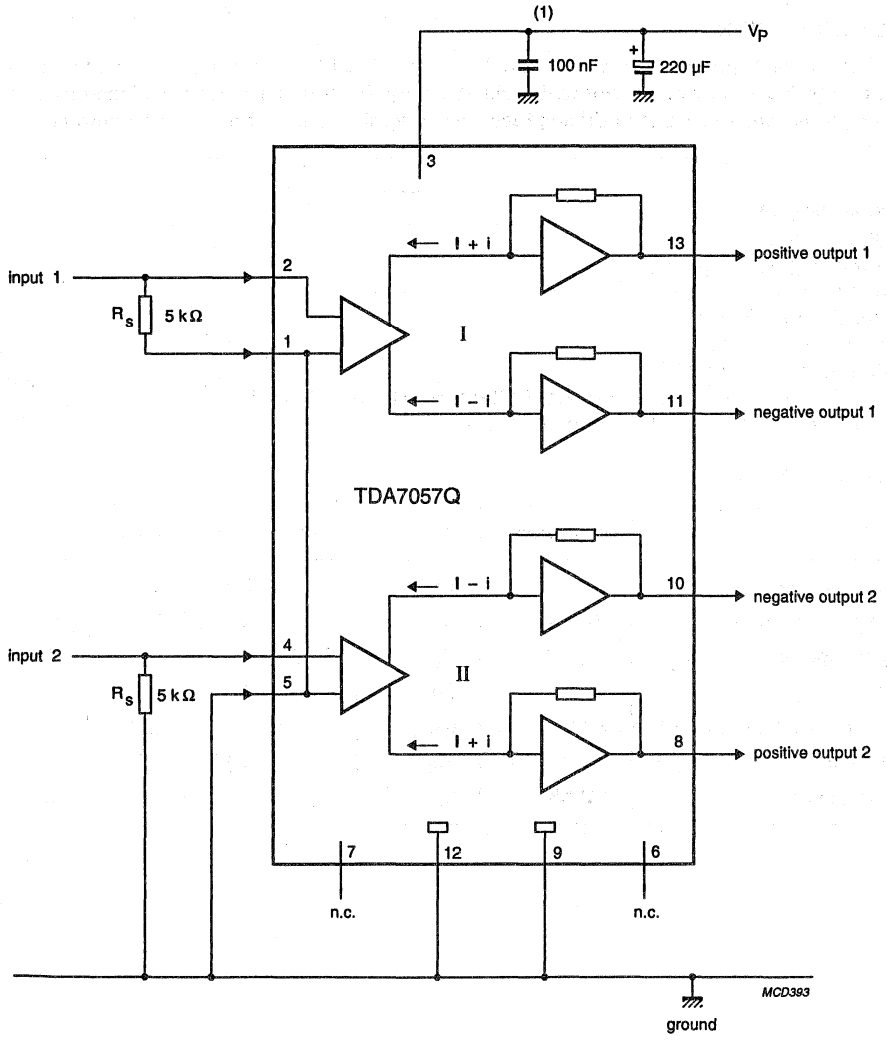
V_P = 11 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
Operating position						
I_P	total quiescent current	R_L = ∞; note 1	–	10	14	mA
P_O	output power	THD = 10%	2.5	3	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%
G_v	voltage gain		39	40	41	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 2	–	180	300	μV
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	60	–	μV
B	bandwidth		–	20 Hz to 20 kHz	–	
SVRR	supply voltage ripple rejection	note 4	36	60	–	dB
$\|V_{off}\|$	DC output offset voltage	R_S = 5 kΩ	–	–	200	mV
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
α	channel separation	R_S = 5 kΩ	40	–	–	dB
$\|G_v\|$	channel balance		–	–	1	dB

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).
3. The noise output voltage RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
   With a practical load (R_L = 16 Ω, L = 200 μH) the noise output current is only 50 nA.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz.
   The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 3.

Fig.3 Test and application diagram.

SINGLE POWER DRIVER

GENERAL DESCRIPTION

The TDA7072 is a single power driver circuit in a Bridge-Tied-Load (BTL) configuration and is intended for use as a power driver in servo systems with a single supply. It has been primarily designed for use in compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Features

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suitable for handling pulse width modulated (PWM) signals up to 176 kHz
- Electrostatic discharge (ESD) protection on all pins

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Internal voltage gain		G_v	37.5	39	40	dB
Slew rate		SR	–	12	–	V/μs
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Input bias current		I_{bias}	–	100	300	nA
Cut-off frequency	–3 dB	f_h	–	1.5	–	MHz

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

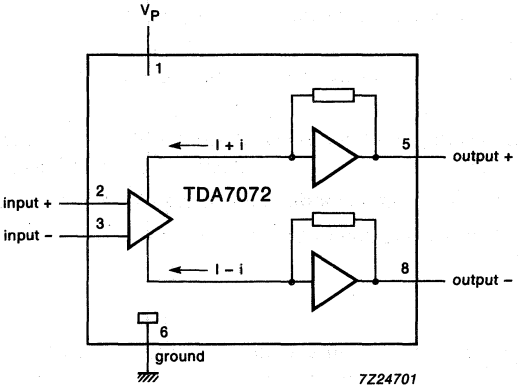


Fig.1 Block diagram.

PINNING

1. Positive supply voltage (V_P)
2. Positive input
3. Negative input
4. Not connected
5. Positive output
6. Ground
7. Not connected
8. Negative output

FUNCTIONAL DESCRIPTION

The TDA7072 is a single power driver circuit in a BTL configuration and is intended for use as a power driver for servo systems with a single supply. It has been primarily designed for compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Utilization of the BTL principle means the device can supply a bidirectional current to the load, with only a single supply voltage.

The voltage gain is fixed by internal feedback at 39 dB and the device operates in a wide supply voltage range (3 to 15 V).

The device can supply a maximum output current of 0.6 A, but the load can be short-circuited under all input conditions.

The differential inputs can handle common mode input voltages from ground (0 V) up to ($V_P - 2.2$) V.

The device has a very high slew rate and due to the very large bandwidth it can handle PWM signals up to 176 kHz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Peak output current					
repetitive		I_{ORM}	–	1	A
non-repetitive		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig.2		
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+ 150	°C
Short-circuiting time	note 1	t_{sc}	–	1	hour

Note to the ratings

1. The load can be short-circuited for all input conditions.

DEVELOPMENT DATA

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 100 K/W

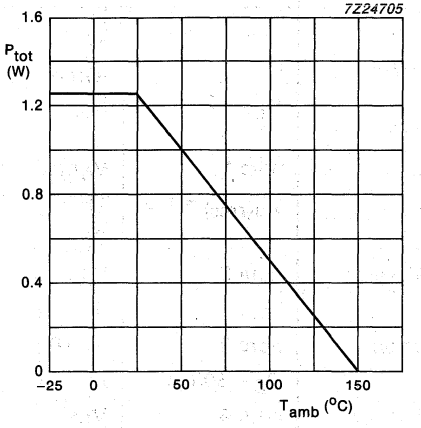


Fig.2 Power derating curve.

Power dissipation example

At T_{amb} = 60 °C the maximum power dissipation is: $\frac{150-60}{100}$ = 0.9 W

CHARACTERISTICS

V_P = 5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Output voltage swing (peak-to-peak value)	note 1	$V_{o(p-p)}$	5.2	5.8	–	V
Total harmonic distortion	$V_{o(rms)}$ = 1 V	THD	–	0.1	1	%
Voltage gain		G_v	37.5	39	40	dB
Noise output voltage (RMS value)	note 2	$V_{no(rms)}$	–	150	300	μV
Bandwidth		B	–	1.5	–	MHz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage	R_S = 500 Ω	$\lvert\Delta V_{5\text{-}8}\rvert$	–	–	100	mV
DC common-mode voltage range	note 4	V_{IC}	–	0–2.8	–	V
DC common-mode rejection ratio		CMRR	–	100	–	dB
Input impedance		$\lvert Z_I\rvert$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA
Slew rate		SR	–	12	–	V/μs

DEVELOPMENT DATA

Notes to the characteristics

1. The output voltage swing is typically limited to 2 x (V_P – 2.1) V (see Fig.4).
2. The noise output voltage (RMS value) is measured with a source impedance (R_S) of 500 Ω, unweighted and a bandwidth of 20 Hz to 20 kHz.
3. The ripple rejection is measured with the source impedance R_S = 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage (200 mV, RMS value) is applied to the positive supply rail.
4. The DC common-mode voltage range is limited to (V_P – 2.2) V.

TEST AND APPLICATION INFORMATION

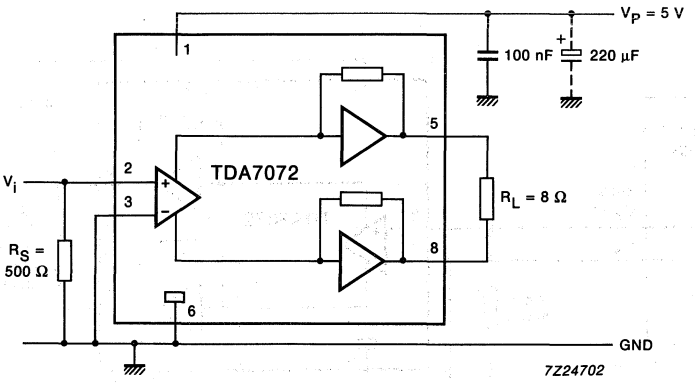


Fig.3 Test circuit diagram.

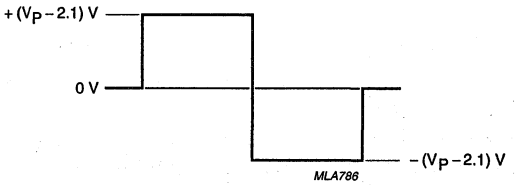


Fig.4 Maximum output voltage swing across R_L.

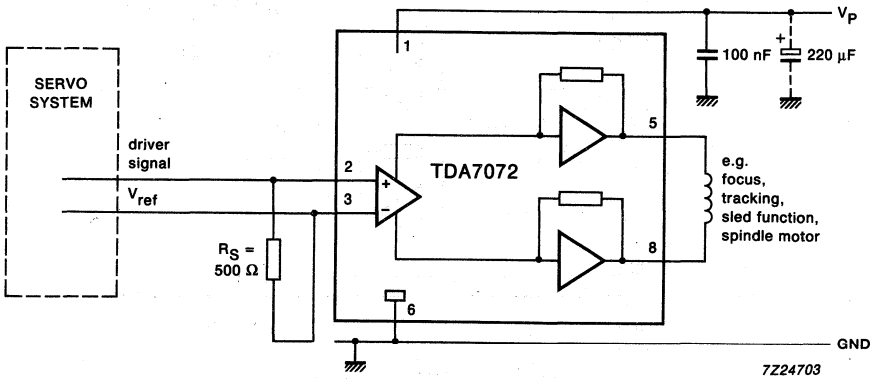


Fig.5 Application circuit diagram.

DEVELOPMENT DATA

Single BTL power driver TDA7072A/AT

FEATURES

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suited for handling PWM signals up to 176 kHz
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7072A/AT are single power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are specially designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
G_v	internal voltage gain		32.5	33.5	34.5	dB
I_P	total quiescent current	V_P = 5 V; R_L = ∞	–	4	8	mA
SR	slew rate		–	12	–	V/µs
I_O	output current		–	–	0.6	A
I_{bias}	input bias current		–	100	300	nA
f_{co}	cut-off frequency	–3 dB	–	1.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7072A	8	DIL	plastic	SOT97
TDA7072AT	8	mini-pack	plastic	SOT96A

Single BTL power driver TDA7072A/AT

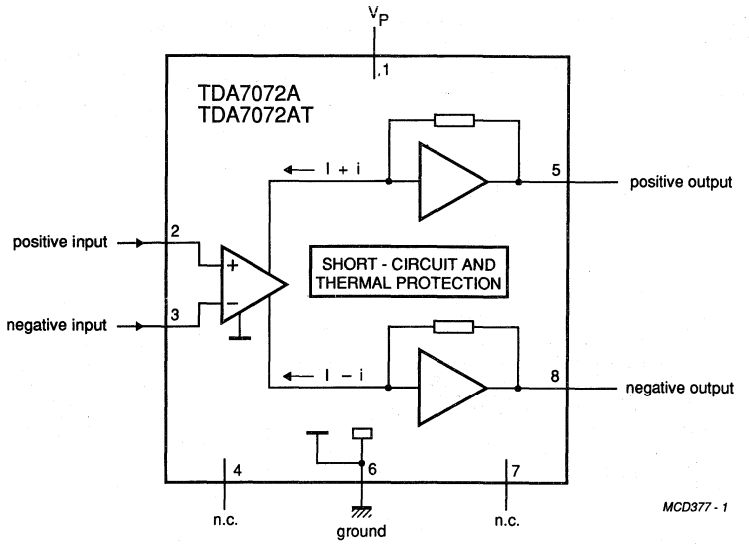


Fig.1 Block diagram.

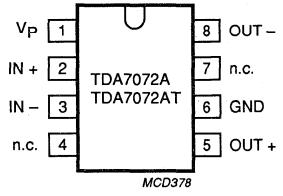


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
IN–	3	negative input
n.c.	4	not connected
OUT+	5	positive output
GND	6	ground
n.c.	7	not connected
OUT–	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7072A/AT are single power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are particular designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Because of the BTL configuration, the devices can supply a bi-directional DC current in the load, with only a single supply voltage. The voltage gain is fixed by internal feedback at 33.5 dB and the devices operate in a wide supply voltage range (3 to 18 V). The devices can supply a maximum output current of 0.6 A. The outputs can be short-circuited over the load, to the supply and to ground at all input conditions. The differential inputs can handle common mode input voltages from ground level up to (V_P –2.2 V). The devices have a very high slew rate. Due to the large bandwidth, they can handle PWM signals up to 176 kHz.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{amb} < 25 °C			
	TDA7072A		–	1.25	W
	TDA7072AT		–	0.54	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The outputs can be short-circuited over the load, to the supply and to ground at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7072A	100 K/W
	TDA7072AT	230 K/W

note to the thermal resistance

TDA7072A: V_P = 5 V; R_L = 8 Ω; The typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.36 A and P_{tot} = 0.76 W; $T_{amb\ (max)}$ = 150 – 0.76 x 100 = 74 °C
TDA7072AT: V_P = 5 V; R_L = 16 typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore I_O = 0.18 A and P_{tot} = 0.38 W; $T_{amb\ (max)}$ = 150 – 0.38 x 230 = 62 °C

CHARACTERISTICS

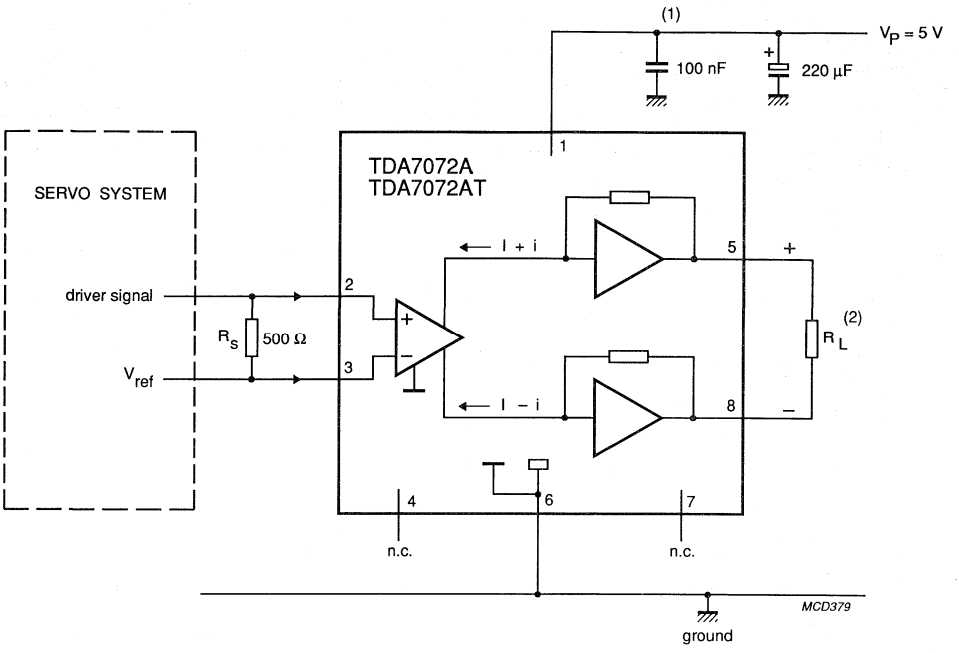
V_P = 5 V; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified (see Fig.3]). TDA7072A: R_L = 8 Ω; TDA7072AT: R_L = 16 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
I_P	total quiescent current	$R_L = \infty$; note 1	–	4	8	mA
ΔV_{OUT}	output voltage swing	note 2	5.2	5.8	–	V
THD	total harmonic distortion	V_{OUT} = 1 V (RMS)				
	TDA7072A		–	0.3	–	%
	TDA7072AT		–	0.1	–	%
G_v	voltage gain		32.5	33.5	34.5	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	75	150	μV
B	bandwidth		–	–	1.5	MHz
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert\Delta V_{5-8}\rvert$	DC output offset voltage	R_S = 500 Ω	–	–	100	mV
$V_{I(CM)}$	DC common mode voltage range	note 5	0	–	2.8	V
CMRR	DC common mode rejection ratio	note 6	–	100	–	dB
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
SR	slew rate		–	12	–	V/μs

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The output voltage swing is typically limited to 2 x (V_P –2.1 V) (see Fig.4).
3. The noise output voltage (RMS value), unweighted (20 Hz to 20 kHz) is measured with R_S = 500 Ω.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The DC common mode voltage range is limited to (V_P –2.2 V).
6. The common mode rejection ratio is measured at V_{ref} = 1.4 V, $V_{I(CM)}$ = 200 mV and f = 1 kHz.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

(2) R_L can be: focus, tracking, sled function or spindle motor.

Fig.3 Test and application diagram.

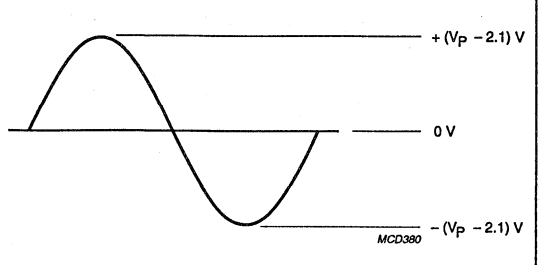


Fig.4 Typical output voltage swing over R_L.

DUAL POWER DRIVER

GENERAL DESCRIPTION

The TDA7073 is a dual power driver circuit in a Bridge-Tied-Load (BTL) configuration and is intended for use as a power driver in servo systems with a single supply. It has been primarily designed for use in compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Features

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suitable for handling pulse width modulated (PWM) signals up to 176 kHz
- Electrostatic discharge (ESD) protection on all pins

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	8	16	mA
Internal voltage gain		G_v	37.5	39	40	dB
Slew rate		SR	–	12	–	V/μs
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Input bias current		I_{bias}	–	100	300	nA
Cut-off frequency	−3 dB	f_h	–	1.5	–	MHz

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

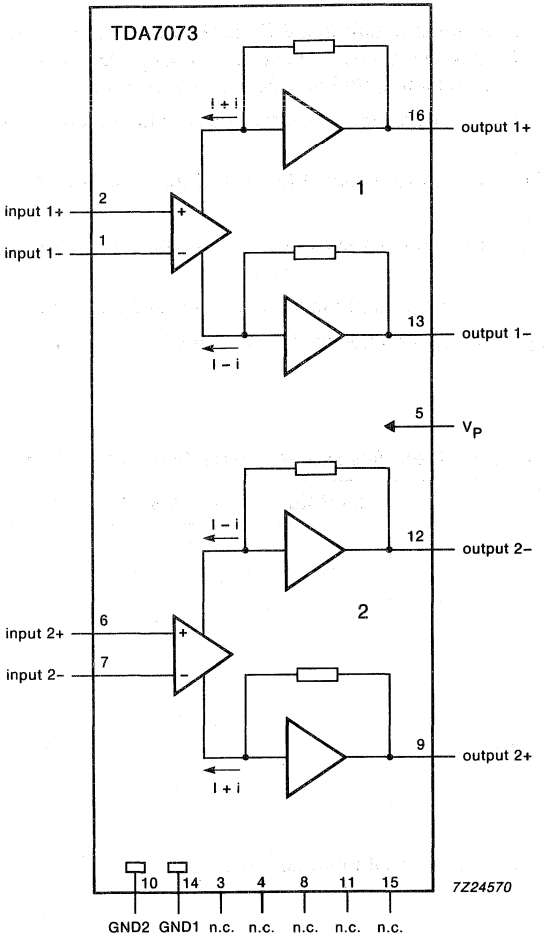


Fig.1 Block diagram.

PINNING

1. Negative input 1
2. Positive input 1
3. Not connected
4. Not connected
5. Supply voltage V_P
6. Positive input 2
7. Negative input 2
8. Not connected
9. Positive output 2
10. Ground 2
11. Not connected
12. Negative output 2
13. Negative output 1
14. Ground 1
15. Not connected
16. Positive output 1

FUNCTIONAL DESCRIPTION

The TDA7073 is a dual power driver circuit in a BTL configuration and is intended for use as a power driver for servo systems with a single supply. It has been primarily designed for compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Utilization of the BTL principle means the device can supply a bidirectional current to the load, with only a single supply voltage.

The voltage gain is fixed by internal feedback at 39 dB and the device operates in a wide supply voltage range (3 to 15 V).

The device can supply a maximum output current of 0.6 A, but the load can be short-circuited under all input conditions.

The differential inputs can handle common mode input voltages from ground (0 V) up to (V_P – 2.2) V.

The device has a very high slew rate and due to the very large bandwidth it can handle PWM signals up to 176 kHz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Peak output current					
repetitive		I_{ORM}	–	1	A
non-repetitive		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig.2		
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+150	°C
Short circuit time	note 1	t_{sc}	–	1	hour

Note to the ratings

1. The load can be short-circuited for all input conditions.

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 55 K/W

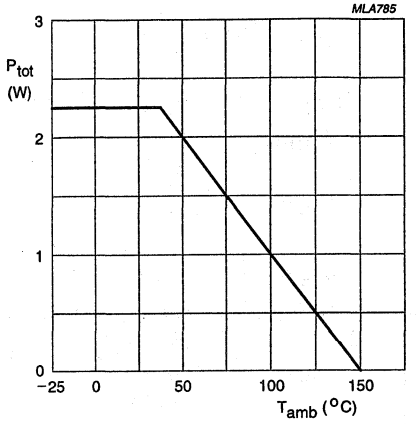


Fig.2 Power derating curve.

Power dissipation example

At T_{amb} = 60 °C the maximum allowable power dissipation is:

$$\frac{150 - 60}{55} = 1.64\ W$$

CHARACTERISTICS

V_P = 5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; see test circuit, Fig.3.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Total quiescent current	$R_L = \infty$	I_{tot}	–	8	16	mA
Output voltage swing (peak-to-peak value)	note 1	$V_{o(p-p)}$	5.2	5.8	–	V
Total harmonic distortion	$V_{o(rms)}$ = 1 V	THD	–	0.1	–	%
Voltage gain		G_v	37.5	39	40	dB
Noise output voltage	note 2	$V_{no(rms)}$	–	150	300	μV
Bandwidth		B	–	1.5	–	MHz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage	R_S = 500 Ω	$\lvert\Delta V_{16\text{-}13}\rvert$	–	–	100	mV
		$\lvert\Delta V_{12\text{-}9}\rvert$	–	–	100	mV
DC common-mode voltage range	note 4	V_I	–	0 - 2.8	–	V
DC common-mode rejection ratio		CMRR	–	100	–	dB
Input impedance		$\lvert Z_I\rvert$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA
Channel separation		α	50	60	–	dB
Channel unbalance		$\lvert\Delta G_v\rvert$	–	–	1	dB
Slew rate		SR	–	12	–	V/μs

Notes to the characteristics

1. The output voltage swing is typically limited to 2 x (V_P – 2.1) V, (see Fig.4).
2. The noise output voltage (RMS value) is measured with a source impedance (R_S) of 500 Ω, unweighted and a bandwidth of 20 Hz to 20 kHz.
3. The ripple rejection is measured with the source impedance R_S = 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage (200 mV, RMS value) is applied to the positive supply rail.
4. The DC common-mode voltage range is limited to (V_P – 2.2) V.

TEST AND APPLICATION INFORMATION

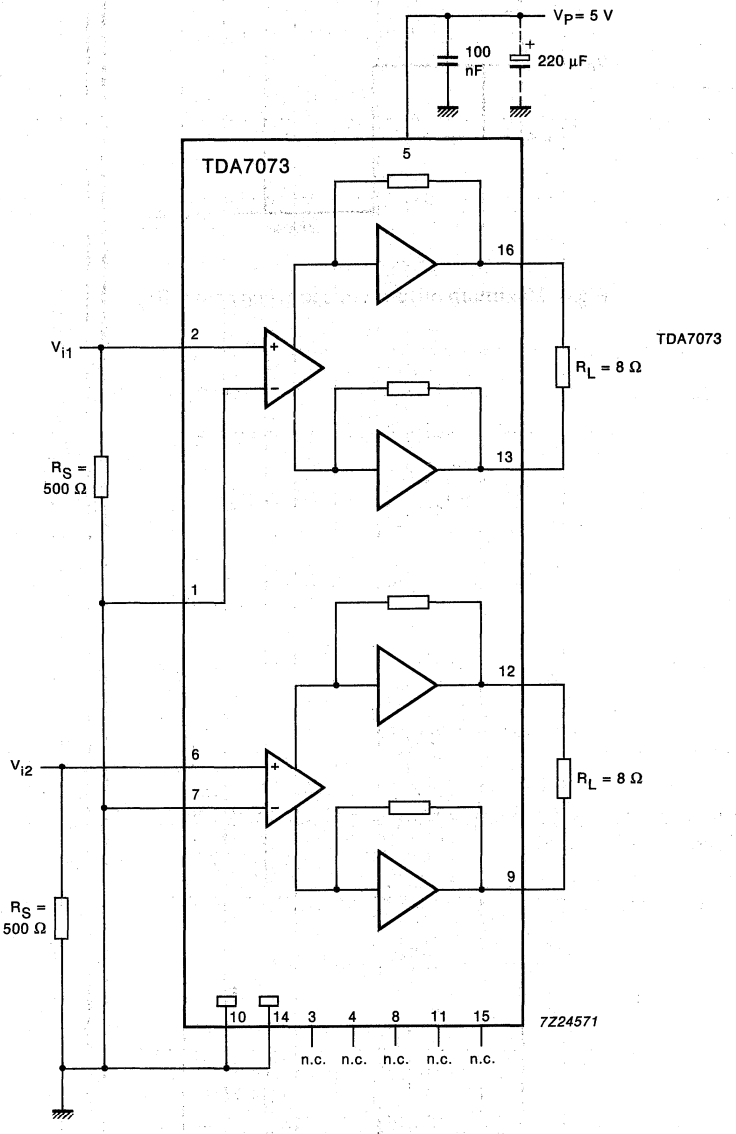


Fig.3 Test circuit diagram.

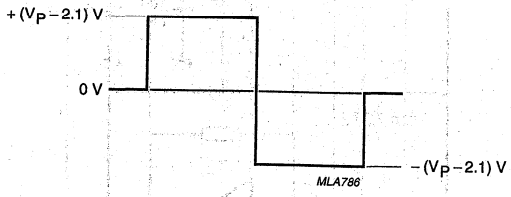


Fig.4 Maximum output voltage swing across R_L.

TEST AND APPLICATION INFORMATION

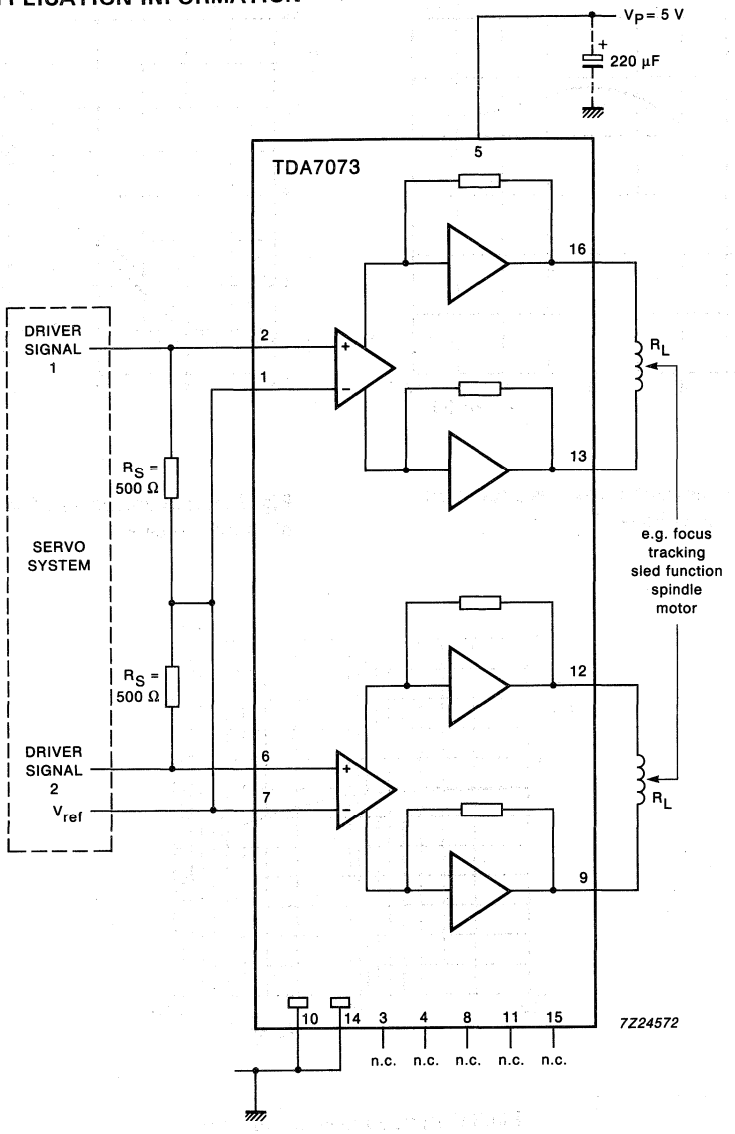


Fig.5 Application circuit diagram.

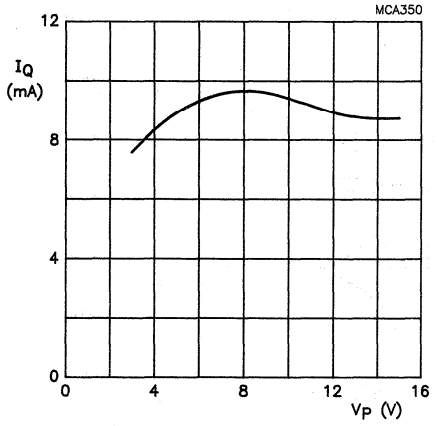


Fig.6 Quiescent current as a function of supply voltage; $R_L = \infty$.

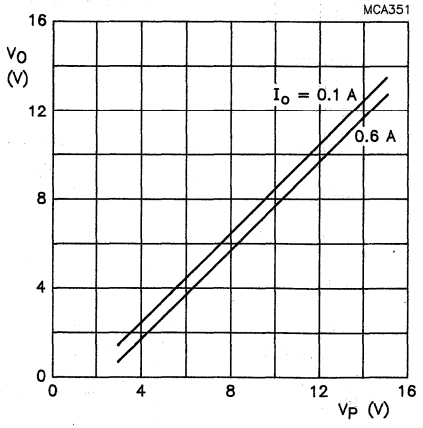


Fig. 7 Output voltage as a function of supply voltage.

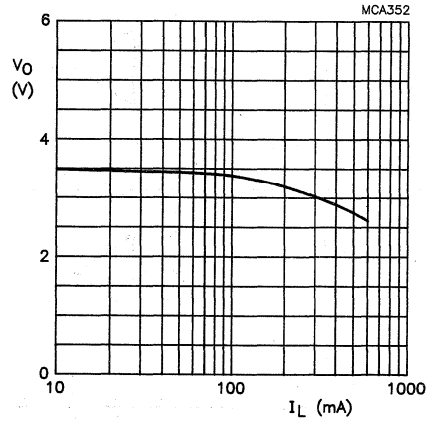


Fig.8 Output voltage as a function of output current; $V_P = 5$ V.

Dual BTL power driver TDA7073A/AT

FEATURES

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suited for handling PWM signals up to 176 kHz
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7073A/AT are dual power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are specially designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
G_v	internal voltage gain		32.5	33.5	34.5	dB
I_P	total quiescent current	$V_P = 5$ V; $R_L = \infty$	–	8	16	mA
SR	slew rate		–	12	–	V/µs
I_O	output current		–	–	0.6	A
I_{bias}	input bias current		–	100	300	nA
f_{co}	cut-off frequency	–3 dB	–	1.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7073A	16	DIL	plastic	SOT38
TDA7073AT	16	mini-pack	plastic	SOT162A

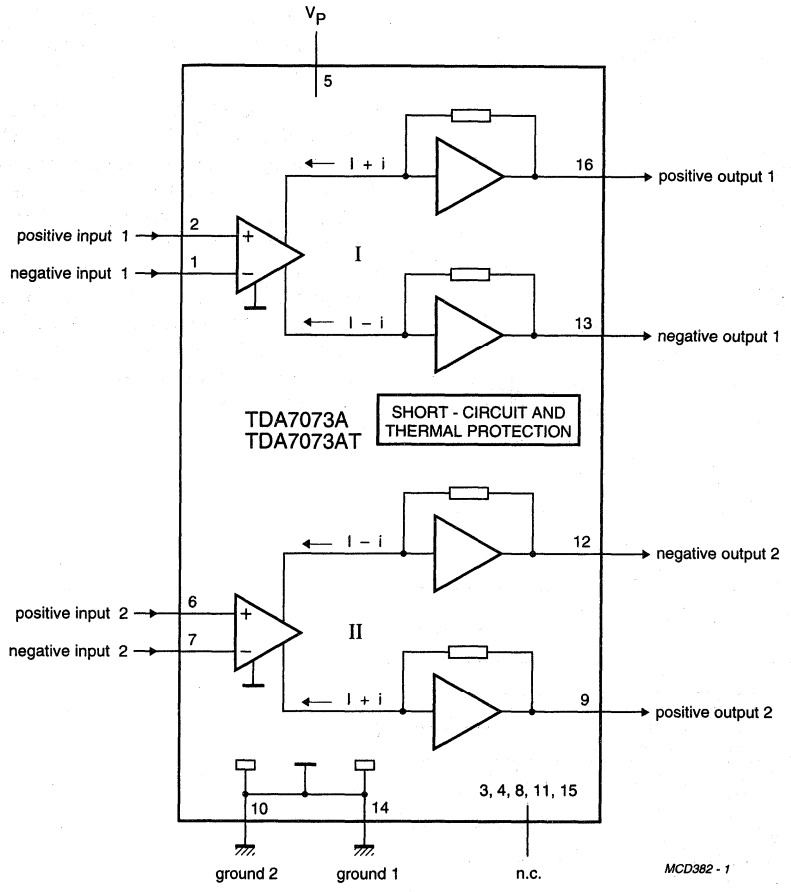


Fig.1 Block diagram.

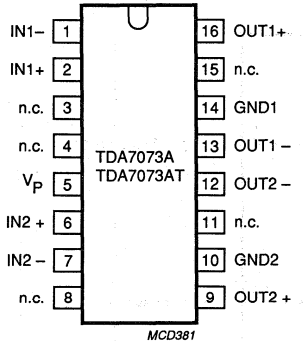


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7073A/AT are dual power driver circuits in a BTL configuration, intended for use as a power driver for servo systems with a single supply. They are particular designed for compact disc players and are capable of driving focus, tracking, sled functions and spindle motors.

Because of the BTL configuration, the devices can supply a bi-directional DC current in the load, with only a single supply voltage. The voltage gain is fixed by internal feedback at 33.5 dB and the devices operate in a wide supply voltage range (3 to 18 V). The devices can supply a maximum output current of 0.6 A. The outputs can be short-circuited over the load, to the supply and to ground at all input conditions. The differential inputs can handle common mode input voltages from ground level up to (V_P –2.2 V). The devices have a very high slew rate. Due to the large bandwidth, they can handle PWM signals up to 176 kHz.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1–	1	negative input 1
IN1+	2	positive input 1
n.c.	3	not connected
n.c.	4	not connected
V_P	5	positive supply voltage
IN2+	6	positive input 2
IN2–	7	negative input 2
n.c.	8	not connected
OUT2+	9	positive output 2
GND2	10	ground 2
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
GND1	14	ground 1
n.c.	15	not connected
OUT1+	16	positive output 1

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} < 25$ °C			
	TDA7073A		–	2.5	W
	TDA7073AT		–	1.32	W
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time	see note	–	1	hr

Note to the limiting values

The outputs can be short-circuited over the load, to the supply and to ground at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7073A	50 K/W
	TDA7073AT	95 K/W

Note to the thermal resistance

TDA7073A: $V_P = 5$ V; $R_L = 8\ \Omega$; The typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore $I_O = 0.36$ A and $P_{tot} = 2 \times 0.76$ W = 1.52 W; $T_{amb\ (max)} = 150 - 1.52 \times 50 = 74$ °C

TDA7073AT: $V_P = 5$ V; $R_L = 16\ \Omega$; typical voltage swing = 5.8 V and V_{loss} is 2.1 V therefore $I_O = 0.18$ A and $P_{tot} = 2 \times 0.38$ W = 0.76 W; $T_{amb\ (max)} = 150 - 0.76 \times 95 = 77$ °C

CHARACTERISTICS

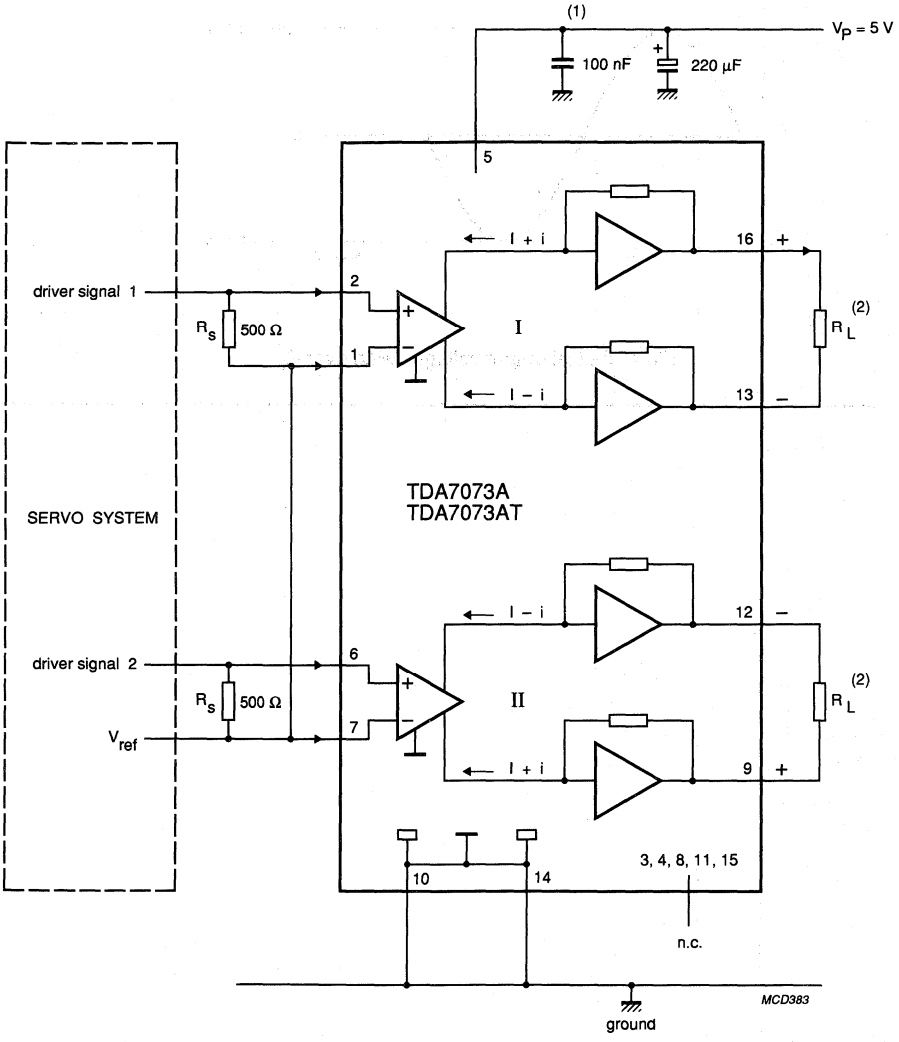
V_P = 5 V; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified (see Fig.3]).
TDA7073A: R_L = 8 Ω; TDA7073AT: R_L = 16 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	5.0	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
I_P	total quiescent current	$R_L = \infty$; note 1	–	8	16	mA
ΔV_{OUT}	output voltage swing	note 2	5.2	5.8	–	V
THD	total harmonic distortion	V_{OUT} = 1 V (RMS)				
	TDA7073A		–	0.3	–	%
	TDA7073AT		–	0.1	–	%
G_v	voltage gain		32.5	33.5	34.5	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 3	–	75	150	μV
B	bandwidth		–	–	1.5	MHz
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert\Delta V_{16\text{-}13,\ 12\text{-}9}\rvert$	DC output offset voltage	R_S = 500 Ω	–	–	100	mV
$V_{I(CM)}$	DC common mode voltage range	note 5	0	–	2.8	V
CMRR	DC common mode rejection ratio	note 6	–	100	–	dB
Z_I	input impedance		–	100	–	kΩ
I_{bias}	input bias current		–	100	300	nA
α	channel separation		40	50	–	dB
$\lvert\Delta G V\rvert$	channel unbalance		–	–	1	dB
SR	slew rate		–	12	–	V/μs

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L
2. The output voltage swing is typically limited to 2 x (V_P –2.1 V) (see Fig.4)
3. The noise output voltage (RMS value), unweighted (20 Hz to 20 kHz) is measured with R_S = 500 Ω
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail
5. The DC common mode voltage range is limited to (V_P –2.2 V)
6. The common mode rejection ratio is measured at V_{ref} = 1.4 V, $V_{I(CM)}$ = 200 mV and f = 1 kHz

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.

(2) R_L can be: focus, tracking, sled function or spindle motor.

Fig.3 Test and application diagram.

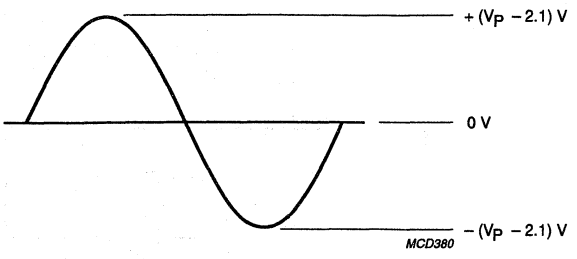


Fig.4 Typical output voltage swing over R_L.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA7088T
FM receiver circuit for battery supply

FEATURES

- Provided with all stages of a mono receiver from antenna to audio output
- Mute circuit
- Search tuning applicable with a single varicap diode
- Mechanical tuning with integrating AFC applicable
- AM application supported
- Power supply polarity protection
- Power supply voltage down to 1.8 V

GENERAL DESCRIPTION

The TDA7088T is a monolithic bipolar integrated circuit for mono portable and pocket radios, wherein a minimum of peripheral components (of small dimensions and low costs) are needed. The circuit is performed with a FLL system (frequency locked loop) and has an FM-IF of about 70 kHz. Selectivity is obtained by active RC-filters. Detuning referred to the IF and too weak input signals is suppressed by muting.

The circuit is applicable for mechanical as well as for electrical tuned radios. Whereas mechanical tuning is possible with or without integrating AFC circuit; electrical tuning is realized by one directional (band-up) search tuning facility, including RESET to the lower band limit.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 4)	1.8	3	5	V
I_P	supply current	4.2	5.2	6.6	mA
f_{iRF}	radio input frequency range	0.5	-	110	MHz
$V_{i\ (rms)}$	input sensitivity for –3 dB limiting (RMS value, mute disable) signal handling	- - 100	 3 200	 6 -	 µV mV
$V_{o\ (rms)}$	AF output signal (R_L = 22 kΩ)	-	85	-	mV
T_{amb}	operating ambient temperature	–10	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7088T	16	mini-pack	plastic	SOT109A

FM receiver circuit for battery supply TDA7088T

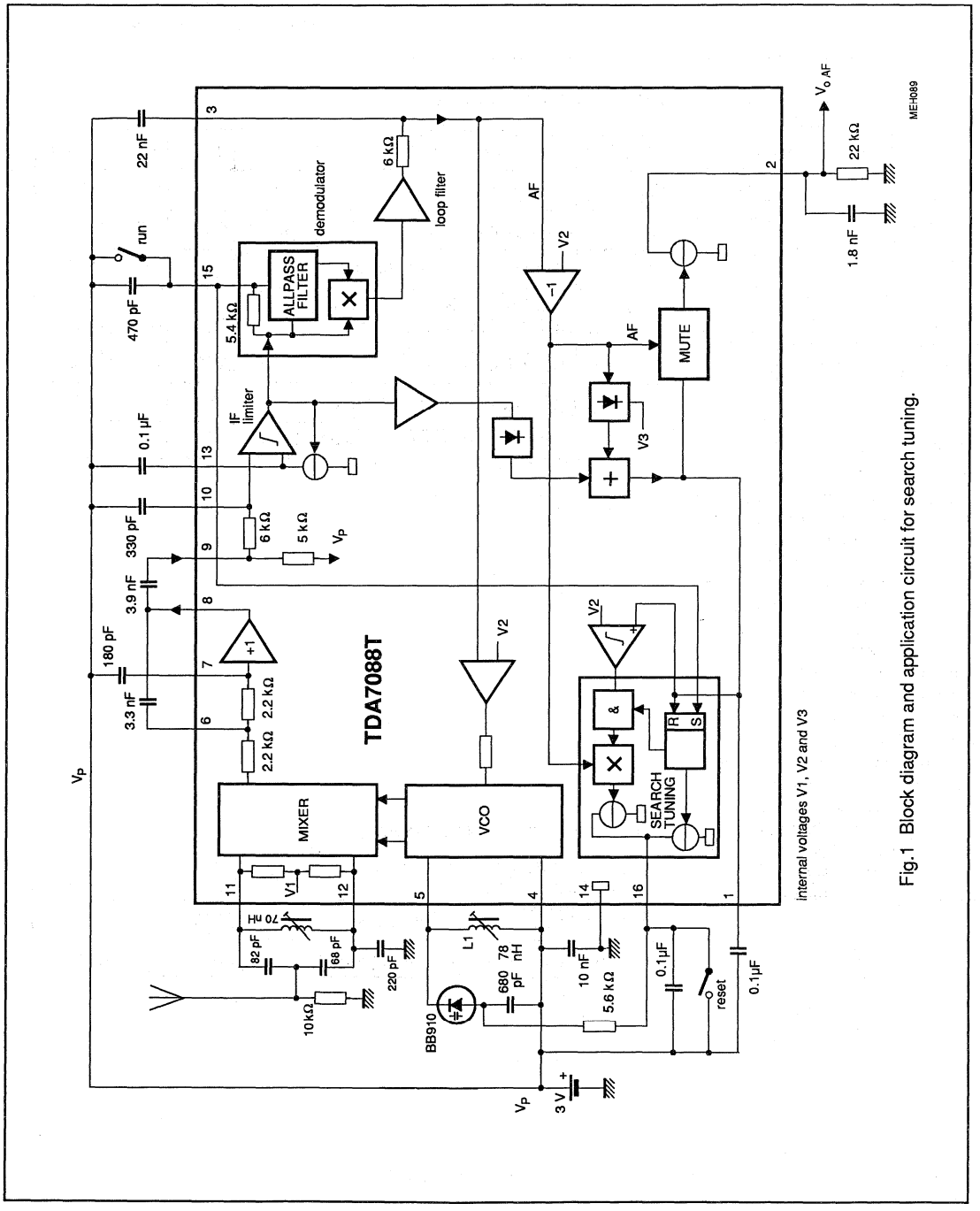


Fig.1 Block diagram and application circuit for search tuning.

FM receiver circuit for battery supply

TDA7088T

PINNING

SYMBOL	PIN	DESCRIPTION
MUTE	1	mute output
V_{oAF}	2	audio frequency output signal
LOOP	3	AF loop filter
V_P	4	+3 V supply voltage
OSC	5	oscillator resonant circuit
IFFB	6	IF feedback
C_{LP1}	7	low-pass capacitor of 1 dB amplifier
V_{oIF}	8	IF output to external coupling capacitor (high-pass)
V_{iIF}	9	IF input to limiter amplifier
C_{LP2}	10	low-pass capacitor of IF limitter amplifier
V_{iRF}	11	radio frequency input
V_{iRF}	12	radio frequency input
C_{LIM}	13	limiter offset voltage capacitor
GND	14	ground (0 V)
C_{AP}	15	all-pass filter capacitor / input for search tuning
TUNE	16	electrical tuning respectively AFC output

PIN CONFIGURATION

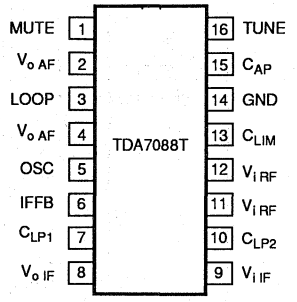


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 4)	0	5	V
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–10	+70	°C
V_{ESD}	electrostatic handling*		-	

* There is no special ESD protection circuit built in; ESD data on request.

DC CHARACTERISTICS

V_P = 3 V and T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 4)		1.8	3	5	V
I_P	supply current		4.2	5.2	6.6	mA
V_1	DC voltage		2.50	2.55	2.60	V
V_3	DC voltage		2.64	2.69	2.74	V
$V_{6, 7}$	DC voltage		2.38	2.44	2.50	V
V_8	DC voltage		1.60	1.67	1.74	V
$V_{9, 10, 13}$	DC voltage		2.42	2.47	2.52	V
$V_{11, 12}$	DC voltage		0.91	0.94	0.98	V
V_{15}	DC voltage		2.06	2.12	2.18	V
V_{16}	DC voltage		t.b.n.	-	-	V
I_2	AF output current		45	60	80	μA
I_5	oscillator current		275	375	500	μA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C ; f_{iRF} = 96 MHz modulated with f_{mod} = 1 kHz and ±22.5 kHz deviation; EMF = 400 μV (R_S = 75 Ω) and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\,RF}$	input sensivity at –3 dB before limiting					
	(RMS value, pins 11–12, Fig.4)	mute-off	-	3	6	μV
	input sensivity	–3 dB muting	3	6	12	μV
		S/N = 26 dB	-	5	10	μV
	signal handling (RMS value, pins 11–12)	Δf = ±75 kHz; THD < 10%	100	200	-	mV
S/N	signal-to-noise ratio	Fig.4	52	56	-	dB
THD	total harmonic distortion	Δf = ±22.5 kHz	-	1	1.4	%
		Δf = ±75 kHz	-	2.4	3.3	%
α_{AM}	AM suppression:	FM: 1 kHz; ±75 kHz				
		AM: 1 kHz; m = 0.8	47	52	-	dB
RR_{1000}	ripple rejection, measurements taken with 100 mV (RMS) ripple on V_P	f = 1 kHz	7	10	-	dB
V_o	audio output signal (RMS value, pin 2)	R_L = 22 kΩ	60	85	120	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Search tuning with BB910 (Fig.1)		C_{16} = 0.1 µF				
V_{16}	minimum output voltage	limiting point	-	V_P–1.85	-	V
$\Delta V/\Delta t$	tuning steepness	voltage pin 16	95	210	420	mV/s
$\Delta f_{osc}/\Delta t$	oscillator steepness		1.25	2.83	5.6	MHz/s
$\Delta I_{AFC}/\Delta V_3$	AFC steepness	voltage pin 3	4.75	9.5	19	µA/V

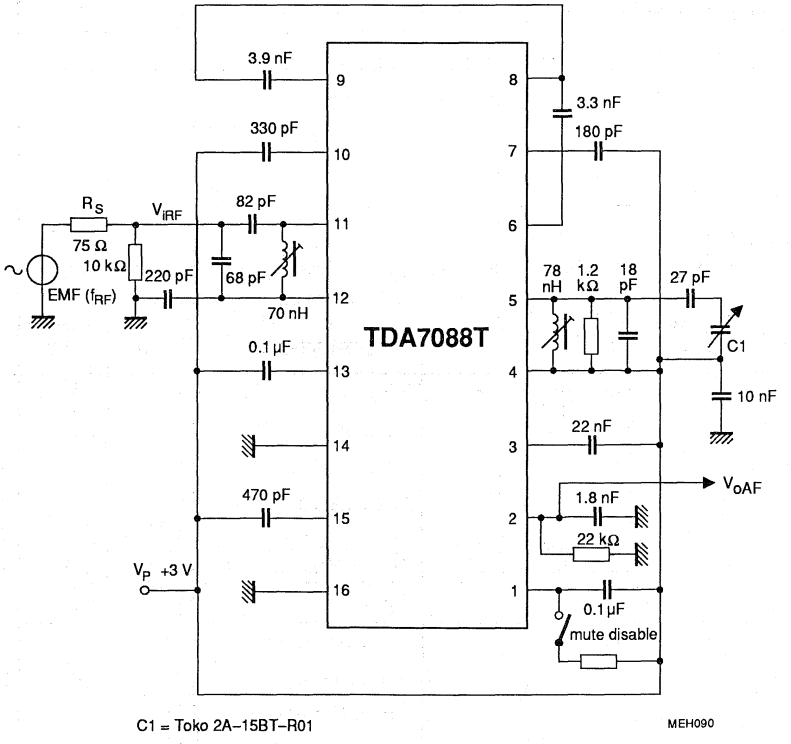


Fig.3 Test circuit and application for mechanical tuning.

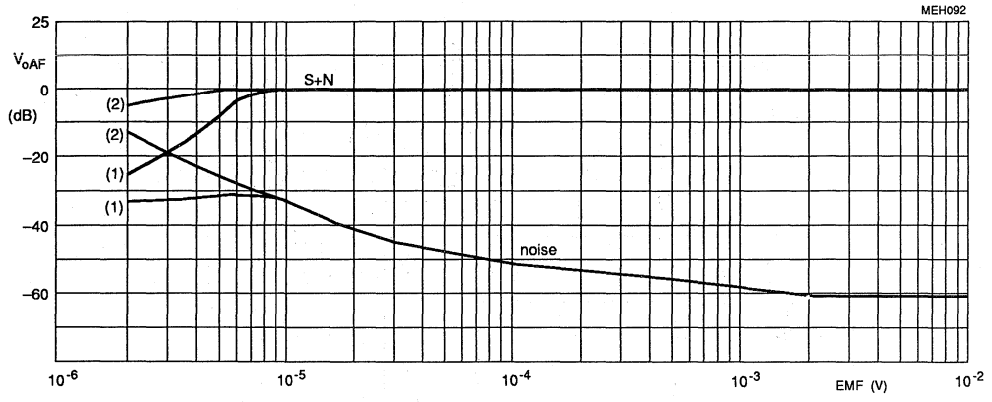


Fig.4 Input sensitivity: (1) mute-on; (2) mute-off.

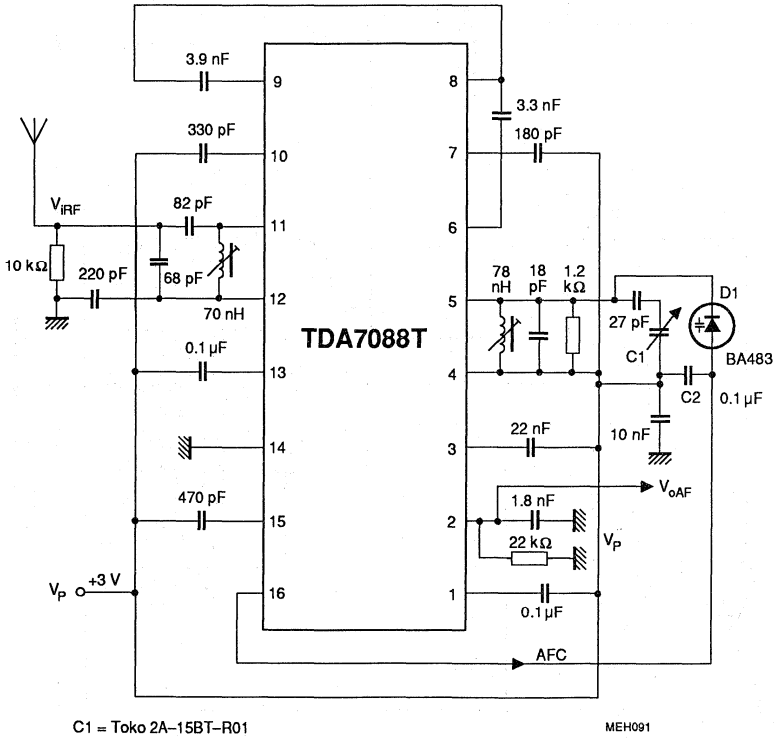


Fig.5 Application circuit with AFC for mechanical tuning.

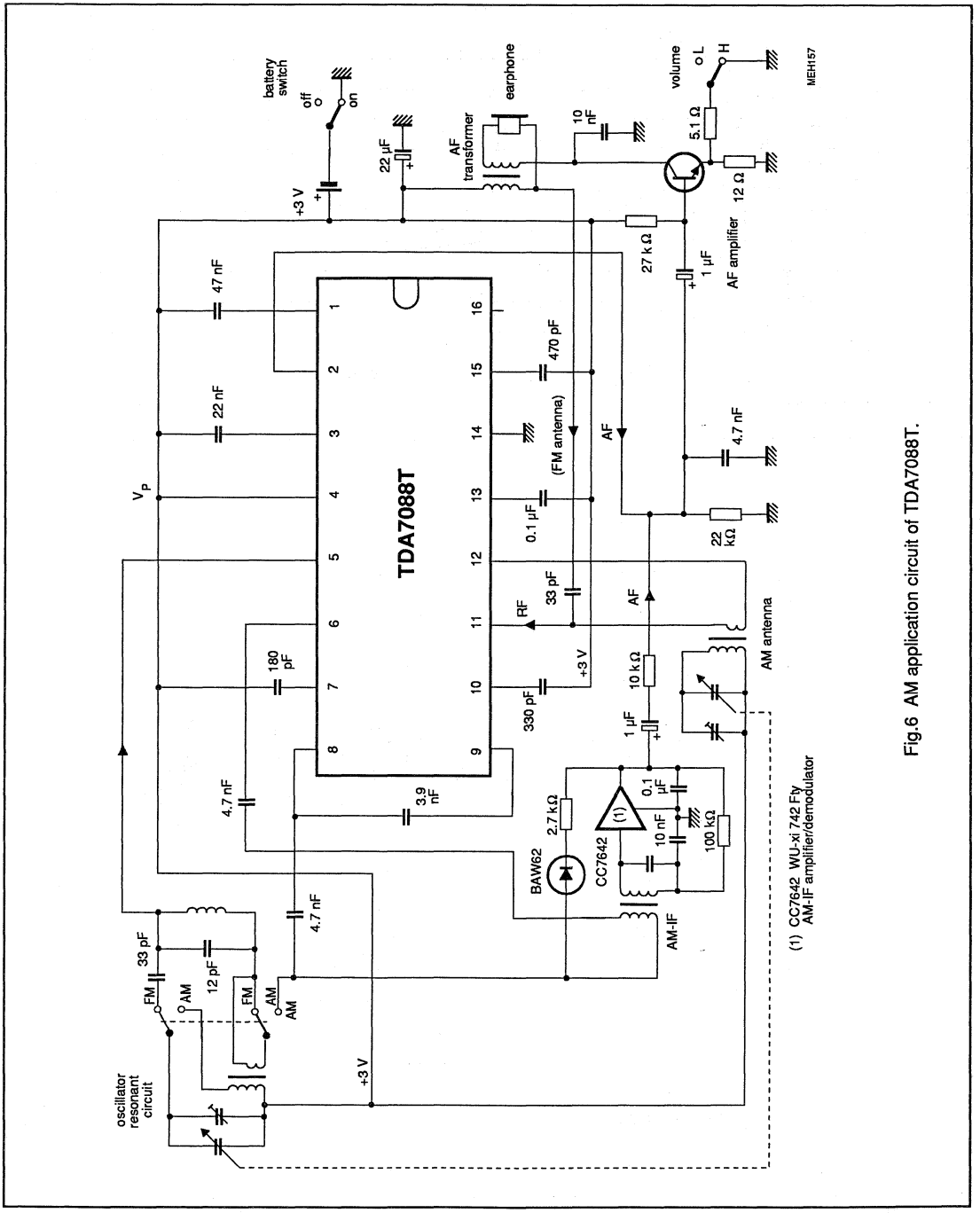


Fig.6 AM application circuit of TDA7088T.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

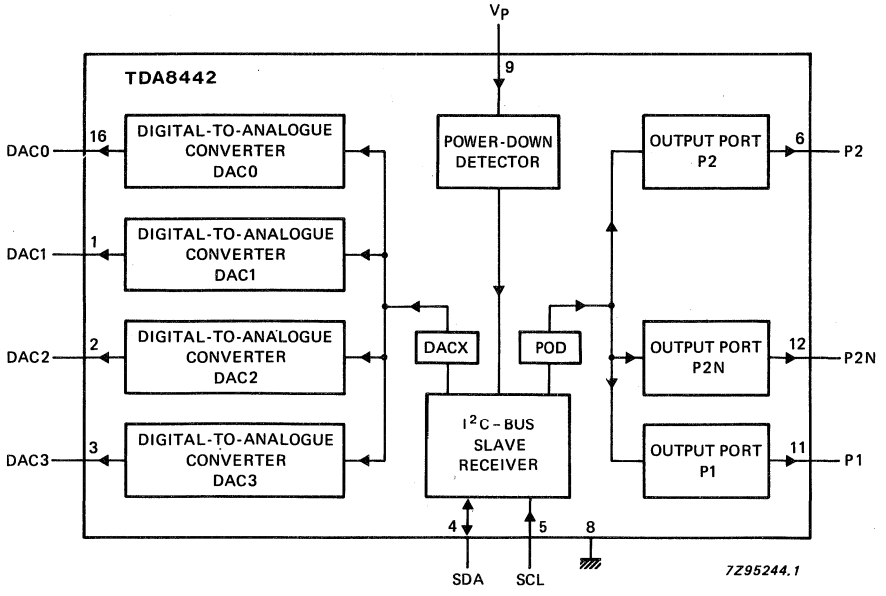


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

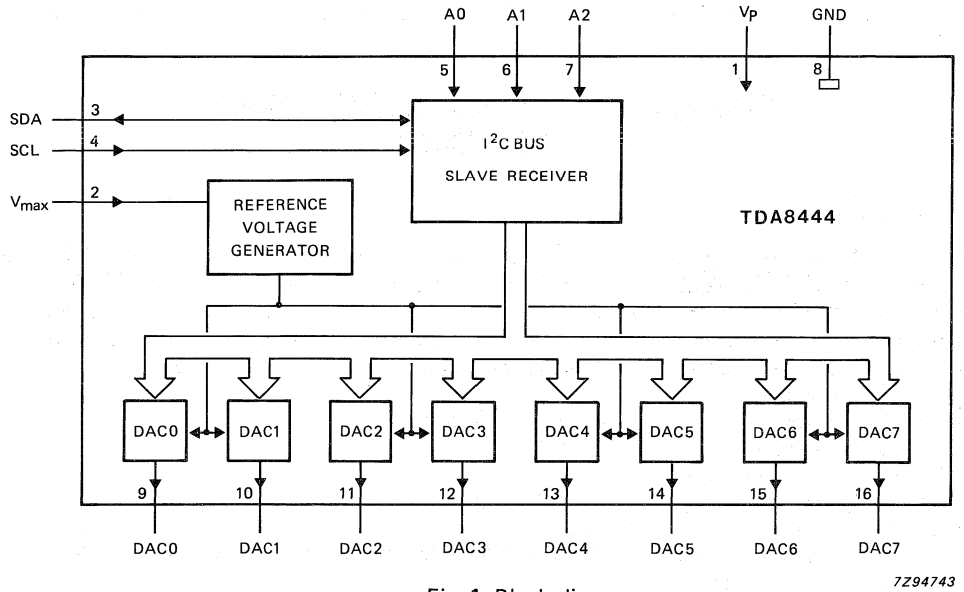


Fig. 1 Block diagram.

PINNING

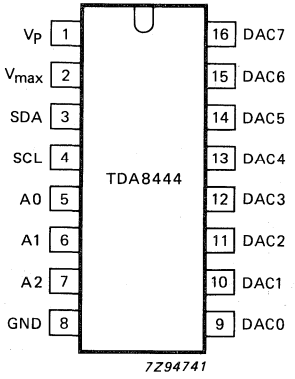


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	Si/$\overline{RD}$ = 0 V	I_Q	7,5	10	12,5	mA
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
LF input current (for each diode input)		I_D	0	–	6	μA
Laser supply output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

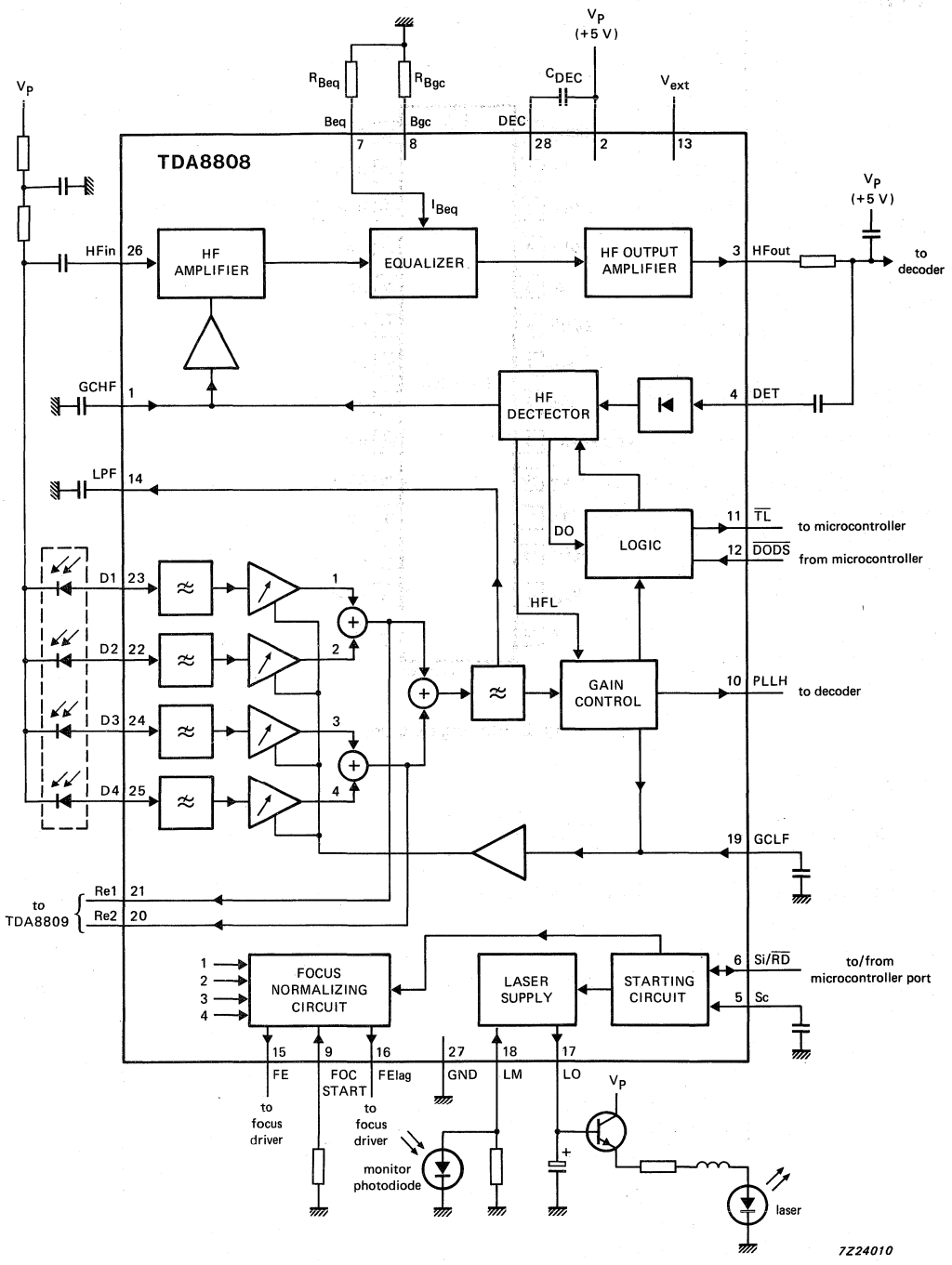


Fig. 1 Block diagram.

PINNING

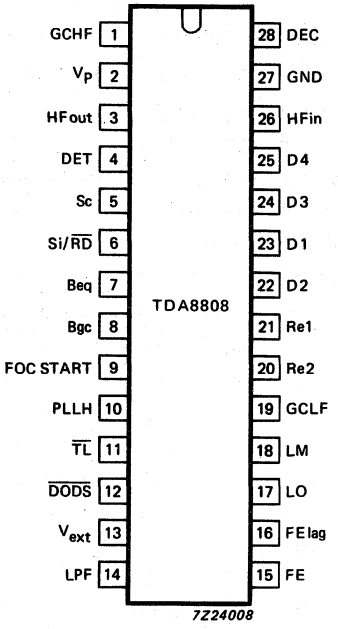


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V_P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T Negative supply connection for FE and FElag output stage; also substrate connection TDA8808AT Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
TDA8808T				
pin 2 to pin 13	$V_P - V_{(ext)}$	−0,3	13	V
pin 27 to pin 13	$V_{GND} - V_{(ext)}$	−0,3	13	V
TDA8808AT				
pin 13 to 27	$V_{ext} - V_{GND}$	−0,3	13	V
pin 2 to pin 27	$V_P - V_{GND}$	−0,3	13	V
Output voltage ranges				
except FE and FE_{lag}	V_O	0	V_P	V
FE and FE_{lag} (TDA8808T)	V_O	V_{ext}	V_P	V
FE and FE_{lag} (TDA8808AT)	V_O	V_{GND}	V_{ext}	V
LM (open loop)	V_O	V_{GND}	V_P	V
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Operating junction temperature	T_j	–	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

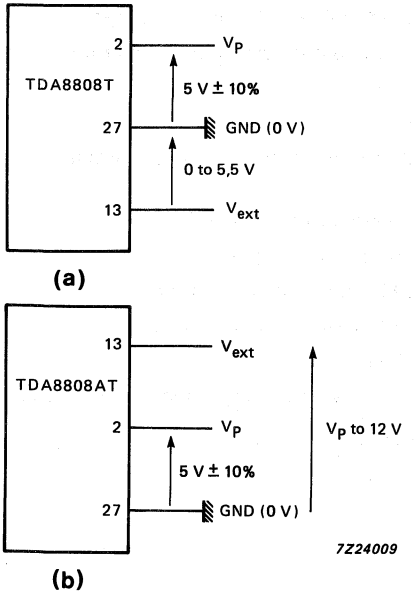


Fig. 3 Supply voltages; (a) TDA8808T, (b) TDA8808AT.

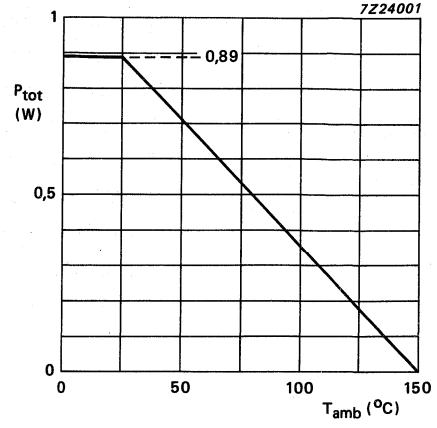


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; V_{ext} = –5 V (TDA8808T); V_{ext} = + 10 V (TDA8808AT); $V_{RE1} = V_{RE2}$ = 3,5 V; $V_{FE} = V_{FElag}$ = 0 V (TDA8808T); $V_{FE} = V_{FElag}$ = 5 V (TDA8808AT); $R_{FOC\ START}$ = 3,3 kΩ; $I_{Beq} = I_{Bgc}$ = 50 μA (current sources); T_{amb} = 25 °C; all voltages measured with respect to V_{GND}, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	–5,5	–5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	$V_{Si/\overline{RD}}$ = 0 V	I_Q	7,5	10	12,5	mA
Reference input (Beq)						
Input voltage level		V_{Beq}	500	560	620	mV
Input current		I_{Beq}	–	–50	–	μA
Reference input (Bgc)						
Input voltage level		V_{Bgc}	1,15	1,25	1,35	V
Input current		I_{Bgc}	–	–50	–	μA
Decoupling input (DEC)						
Input voltage level		V_{DEC}	–	V_P–1,4	–	V
Input impedance		$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
HF input (HFin)						
Input voltage level		V_{HFin}	–	1,4	–	V
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance		$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$	I_{HFin} = ± 1 μA					
Maximum gain	V_{GCHF} = 4 V	G1(max)	390	480	570	mV/μA
Minimum gain	V_{GCHF} = 1,5 V	G1(min)	–5	0	5	mV/μA

parameter	conditions	symbol	min.	typ.	max.	unit
HF part (continued)						
AC characteristics						
Gain (G2) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 1	G2	2	3,5	5	dB
Gain (G3) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 2	G3	4	5,5	7	dB
Phase of input/output signal at 1 MHz	note 3	ϕ	–	$\pi/2$	–	rad.
Group delay at f_{HFin} = 300 kHz + Δf	note 3	τ300	–	290	–	ns
Flatness between 0,1 and 1 MHz	note 3	$\Delta\tau$	*	9	*	ns
HF output (HFout)						
Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	V_{HFout}	1,5	2,4	3,3	V
Output voltage (peak-to-peak value)						
at $I_{HFin(p\text{-}p)}$ = 7 μA	note 4	$V_{O1(p\text{-}p)}$	1	1,20	–	V
at $I_{HFin(p\text{-}p)}$ = 4 to 10 μA	note 5	$V_{O(p\text{-}p)}$	–20%	M_1	+20%	V
Output impedance		$\lvert Z_{HFout}\rvert$	–	60	–	Ω
HF detector input (DET)	see Fig. 5					
DC voltage level	I_{DET} = 0	V_{DET0}	–	2,2	–	V
Positive reference voltage V_{DET} to V_{DET0}		V_{refp}	–10%	540	+10%	mV
Negative reference voltage V_{DET} to V_{DET0}		V_{refn}	–5%	$-V_{refp}$	+5%	mV
Input impedance		$\lvert Z_{DET}\rvert$	–	9	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (GCHF)						
Input voltage for:						
minimum HF gain		V_{GCHF}	–	1,8	–	V
maximum HF gain		V_{GCHF}	–	3,4	–	V
Input impedance						
at V_{GCHF} = 1,5 to 4 V		$\lvert Z_{GCHF}\rvert$	–	25	–	MΩ
Output current (see Fig. 5)						
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	90	100	110	μA
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	86	96	106	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	−0,65	−0,35	−0,2	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	−5,0	−4,4	−3,8	μA
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X*	I_{GCHF}	−0,65	−0,35	−0,2	μA
V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}			10	12,5	15	%
PLLH output (pin 10)						
Output voltage LOW						
I_{PLLH} = 400 μA (sink current)		V_{PLLHL}	–	–	0,4	V
Output voltage HIGH						
I_{PLLH} = −50 μA (source current)		V_{PLLHH}	2,4	–	–	V
Output sink current		I_{PLLH}	0,5	1,5	–	mA
Output source current		I_{PLLH}	–	−100	−50	μA
Threshold total LF current	V_{GCLF} = 3,5 V	I_{DT1}	–	2,0	–	μA
V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25)						
(values given for each input)						
DC voltage level		V_D	–	1,2	–	V
Input current range		I_D	0	–	6	μA
Input impedance at 1 MHz	I_D = 1 μA	$\lvert Z_D\rvert$	–	10	–	kΩ

* X = don't care.

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain						
Maximum DC gain						
for: $A_1 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 3,5 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{11}	S_1–10%	S_1	S_1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{12}	S_1 or 55	S_1	S_1	
for: $A_2 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 3,5 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{21}	S_1–10%	S_1	S_1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{22}	S_1 or 55	S_1	S_1	
S_1 mean value of $A_{11}, A_{12}, A_{21}, A_{22}$			55	64	84	
Minimum DC gain						
for: $A_3 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 0,8 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{31}	S_2–1	S_2	S_2+1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{32}	S_2–1	S_2	S_2+1	
for: $A_4 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 0,8 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{41}	S_2–1	S_2	S_2+1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{42}	S_2–1	S_2	S_2+1	
S_2 mean value of $A_{31}, A_{32}, A_{41}, A_{42}$			–0,1	0,7	3	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain (continued)						
AC gain for:						
$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$						
at $I_{D1} = 0$; $I_{D2(p\text{-}p)} = 1\ \mu A + 2\ \mu ADC$	note 6	G_4	−4,5	−3	−1,5	dB
at $I_{D1(p\text{-}p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D2} = 0$	note 6	G_4	−4,5	−3	−1,5	dB
$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$						
at $I_{D3} = 0$; $I_{D4(p\text{-}p)} = 1\ \mu A + 2\ \mu ADC$	note 7	G_5	−4,5	−3	−1,5	dB
at $I_{D3(p\text{-}p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D4} = 0$	note 7	G_5	−4,5	−3	−1,5	dB
Gain control (GCLF)						
Input voltage for:						
minimum LF gain		V_{GCLF}	–	1	–	V
maximum LF gain		V_{GCLF}	–	2,8	–	V
Input impedance		$\lvert Z_{GCLF} \rvert$	–	25	–	MΩ
Threshold total LF current	I_{DT3}		–	1,6	–	mA
Output current (see Fig. 7)						
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	I_{GCLF}	–	$-0,6\ I_{Bgc}$	± 10	μA
	$I_{DT} > I_{DT3}$; note 8	I_{GCLF}	S_6-10	S_6	S_6+10	μA
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		I_{GCLF}	–	$-0,2\ I_{Bgc}$	± 2	μA
Re1, Re2 outputs (pin 21, pin 20)						
Output current	V_{GCLF} = 3,5 V					
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$		I_{Re1}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re1}	–	0	–	μA
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$		I_{Re2}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re2}	–	0	–	μA
Output voltage						
pin 21		V_{Re1}	1	–	V_P	V
pin 20		V_{Re2}	1	–	V_P	V
Output impedance						
pin 21		$\lvert Z_{Re1} \rvert$	–	1	–	MΩ
pin 20		$\lvert Z_{Re2} \rvert$	–	1	–	MΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Reference current (I_{ret})						
$I_{ret} = I_{Re1} = I_{Re2}$	note	I_{ret}	200	220	240	μA
LPF output (pin 14)						
DC voltage level	note 9	V_{LPF}	V_P–2,1	V_P–1,7	V_P–1,4	V
Input impedance		$\|Z_{LPF}\|$	–	3	–	kΩ
FOC START input (pin 9)						
Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	I_{ST}	75	150	500	μA
	Si/$\overline{RD}$ = LOW	I_{ST}	–	0	–	μA
Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	V_{ST}	430	530	630	mV
	Si/$\overline{RD}$ = LOW	V_{ST}	–20	0	20	mV
FElag output (pin 16)	see Fig. 8					
Output voltage						
TDA8808T		V_{FElag}	V_{ext}+1,5	–	V_P–1,5	V
TDA8808AT		V_{FElag}	+1,5	–	V_{ext}–1,5	V
Output impedance		$\|Z_{FElag}\|$	–	8	–	MΩ
Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V					
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FElag} = I_O$	–10	0	+10	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	–10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	–10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	–5	0	+5	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	–5	0	+5	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
FE output (pin 15)	see Fig. 8					
Output voltage						
TDA8808T		V_{FE}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FE}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\|Z_{FE}\|$	–	8	–	MΩ
Output current	note 10					
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-2S_1-134-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-4S_1-67-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-2S_1-134+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−20%	$-2S_1+67+I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FE} = S_6$	−20%	67	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−15%	$-S_6$	+15%	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−10	0	+10	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	I_{FE}	−5	0	+5	μA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{DODS}}$ logic input (pin 12)						
Switching levels						
input voltage LOW		$V_{\overline{DODS}}$	–	–	+0,8	V
input voltage HIGH		$V_{\overline{DODS}}$	+2	–	–	V
Input source current		$I_{\overline{DODS}}$	–35	–25	–15	μA
Starting input (Sc)	see Fig. 9					
Output voltage	Si/$\overline{\text{RD}}$ = LOW	V_{Sc}	–	0	–	V
Output voltage	S1/$\overline{\text{RD}}$ = HIGH Z	V_{Sc}	–	–	V_P–0,5	V
Output impedance		$\lvert Z_{Sc}\rvert$	–	*	–	MΩ
Output source current	Si/$\overline{\text{RD}}$ = HIGH Z; V_{Sc} = 1,5 V	I_{Sc}	–1,2	–1	–0,8	μA
Output sink current	Si/$\overline{\text{RD}}$ = LOW	I_{Sc}	0,5	1,2	2,0	mA
Si/$\overline{\text{RD}}$ logic input/output (pin 20)	see Fig. 9					
Voltage "forced LOW"	$I_{Si/\overline{RD}}$ = 400 μA; V_{Sc} = 2,5 V; V_{GCLF} < 2,8 V	$V_{Si/\overline{RD}}$	–	0,15	0,4	V
Switching levels						
input voltage LOW		$V_{Si/\overline{RD}}$	–	–	+0,8	V
input voltage HIGH Z	$I_{Si/\overline{RD}}$ = –5 μA	$V_{Si/\overline{RD}}$	2,4	2,8	–	V
Input source current LOW		$I_{Si/\overline{RD}}$	–35	–25	–15	μA
$\overline{\text{TL}}$ logic output (pin 11)	see Fig. 6					
Output voltage level LOW	$I_{\overline{TL}}$ = 400 μA; (sink current)	$V_{\overline{TL}}$	–	0,15	0,4	V
Output voltage level HIGH	$I_{\overline{TL}}$ = –50 μA; (source current)	$V_{\overline{TL}}$	2,4	–	–	V
Threshold total LF current	I_{DT2}		–	3,9	–	μA
Output voltage	DODS = HIGH (≥ 2,4 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{TL}$ logic output (continued)						
Output voltage	$\overline{DODS}$ = LOW ($\leqslant$ 0,8 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V
Output sink current	$V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	1	2,2	–	mA
Output source current	$V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	–100	–50	μA
Delay times (see Fig. 10)	see Fig. 6	τ1	7	8,5	10	μs
		τ2	τ1–15% or 6,5	–	τ1+ 5% or 10	μs
		τ3	7	8,5	10	μs
		τ4	τ3–10% or 7	–	τ3+10% or 10	μs
LO output (pin 17)						
Output voltage		V_{LO}	–	–	V_P – 0,5	V
Output impedance		$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current	Si/$\overline{RD}$ = LOW	I_{LO}	–10	–0,1	0	μA
Maximum output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	–8	–4	–2	mA
LM input (pin 18)						
Input voltage	closed loop	V_{LM}	185	205	225	mV
Input bias current		I_{LM}	–2	–	–	μA
Laser supply						
Transconductance						
For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	G_{LDC}	–	0,5	–	A/V
	Si/$\overline{RD}$ = LOW	G_{LDC}	–	0	–	A/V
For AC (note 12) delay time		τLO	–	*	–	ns

* Value to be fixed.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)}$ = 1 μA; V_{GCHF} = 4 V.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50$ kHz.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.
4. HF part output vpltage for closed loop conditions; f_{HFin} = 500 kHz.
5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.
6. P_1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
7. P_2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

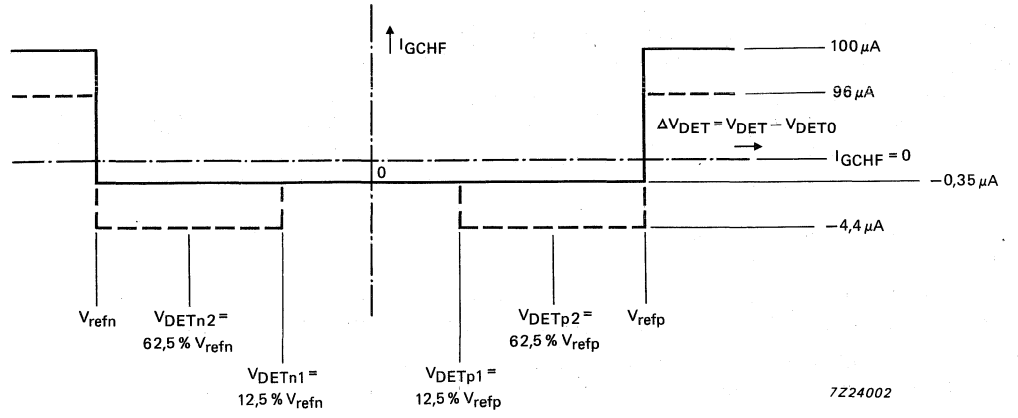
   Measurement taken at V_{GCLF} = 3,5 V.
8. S_6, is the measured value of $S_1 \cdot \frac{I_{DT}}{4} - 1{,}1\ I_{Bgc}$

   Measurement taken at V_{GCLF} = 3,5 V.
9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.
10. FE output current measured at V_{GCLF} = 3,5 V and Si/$\overline{RD}$ = HIGH Z; $I_{ST} = \frac{V_{FOC\ START}}{R_{FOC\ START}}$.
11. Laser supply transconductance for DC

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2$ mA).
12. Laser supply transconductance for AC

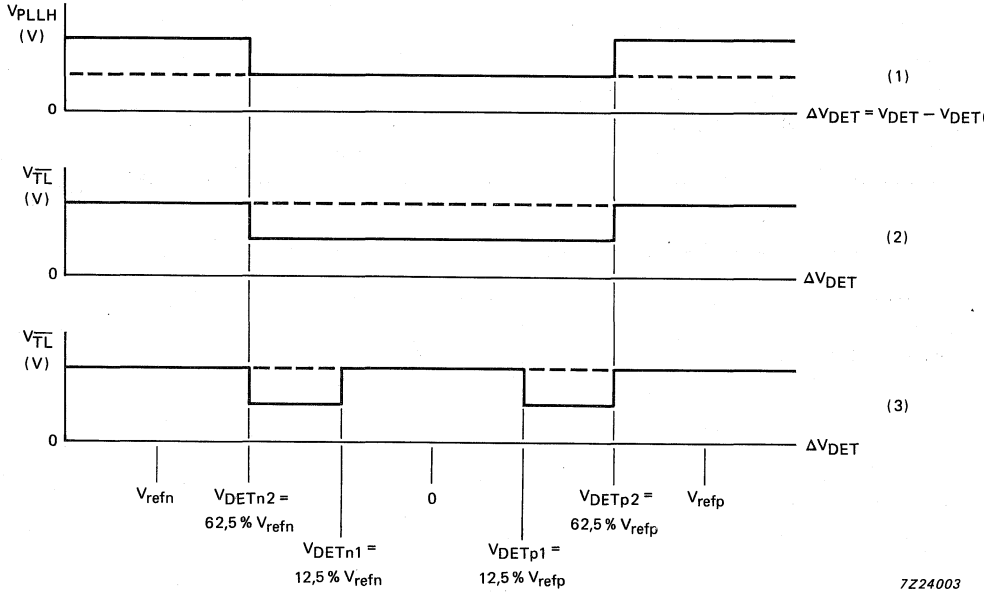
    $G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$

    Where: S is the laplace operator in the frequency domain.



---------- $\overline{DODS}$ = HIGH
——— $\overline{DODS}$ = LOW

Fig. 5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.



(1)

——— $I_{DT} > I_{DT1}$

---------- $I_{DT} < I_{DT1}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$

$I_{DT2} = 5\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(2)

——— $I_{DT} > I_{DT2}$

---------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = LOW

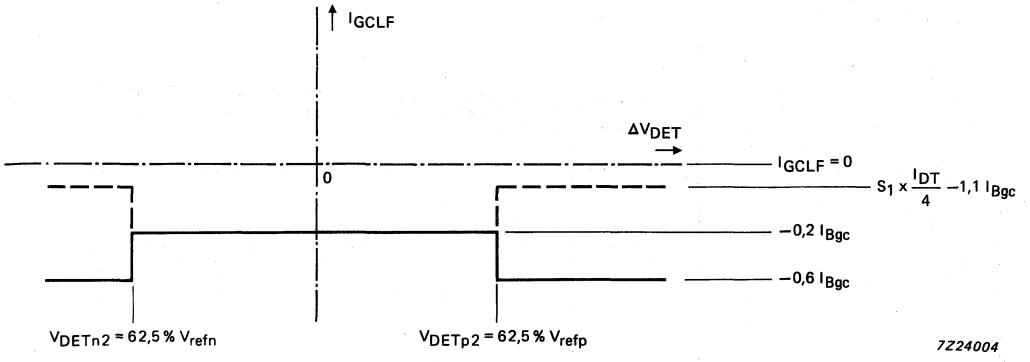
(3)

——— $I_{DT} > I_{DT2}$

---------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = HIGH

Fig. 6 $\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.



---------- $I_{DT} > I_{DT3}$

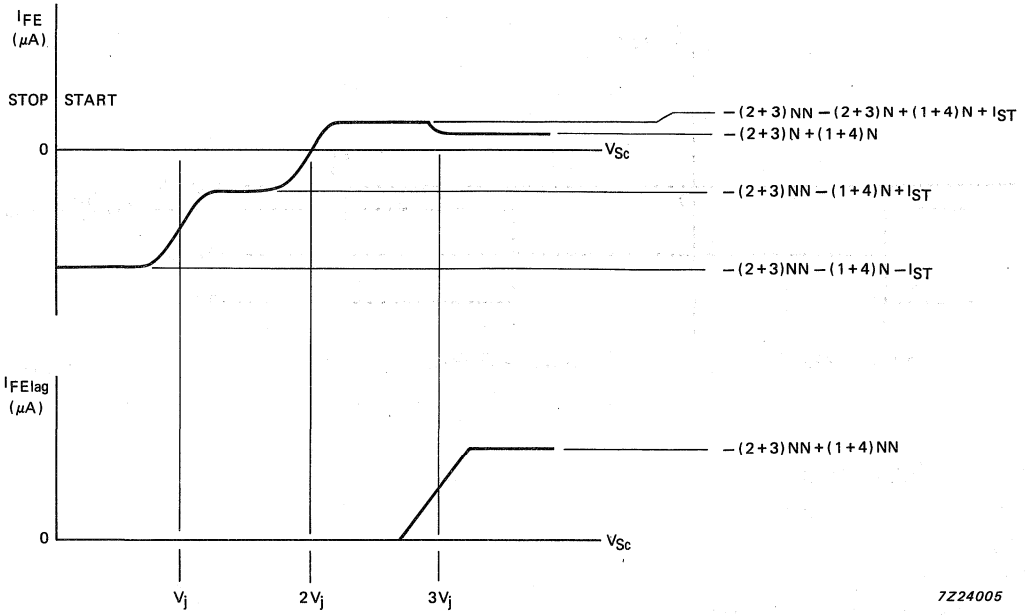
——— $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig. 7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.



I_{ST} = $-I_{FOC\ START}$

I_{cont} = $2\ I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} = $I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} = $I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} = $2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(1 + 4)NN = not normalized currents = $(I_{D1} + I_{D4})\ S_1$

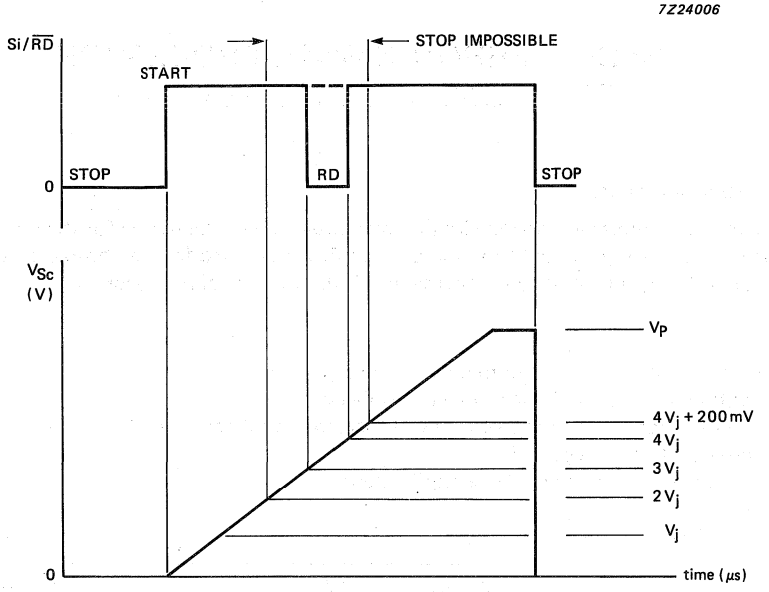
(2 + 3)NN = not normalized currents = $(I_{D2} + I_{D3})\ S_1$

(1 + 4)N = normalized currents = $\left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

(2 + 3)N = normalized currents = $\left(\frac{I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D3}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig. 8 FElag current output as a function of starting voltage input (V_{Sc}).



RD : Si/$\overline{RD}$ forced LOW for ready signal

——— $V_{GCLF} < 2{,}8$ V

---------- $V_{GCLF} > 3{,}5$ V

V_j is the junction voltage (0,7 V typ.)

Fig. 9 Si/$\overline{RD}$ signal as a function of V_{Sc}.

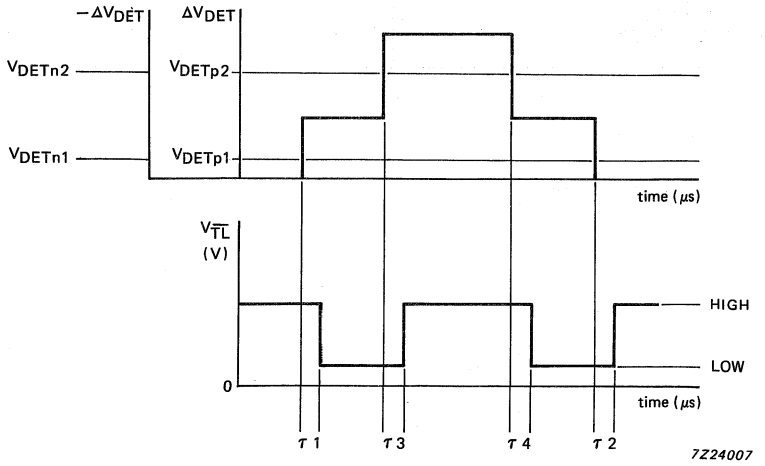


Fig. 10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.

RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8809T is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA8808), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- AGC circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- Radial polarity - 4 - tracks counting
- Possibility for car, home and portable applications

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	–	5,3	–	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

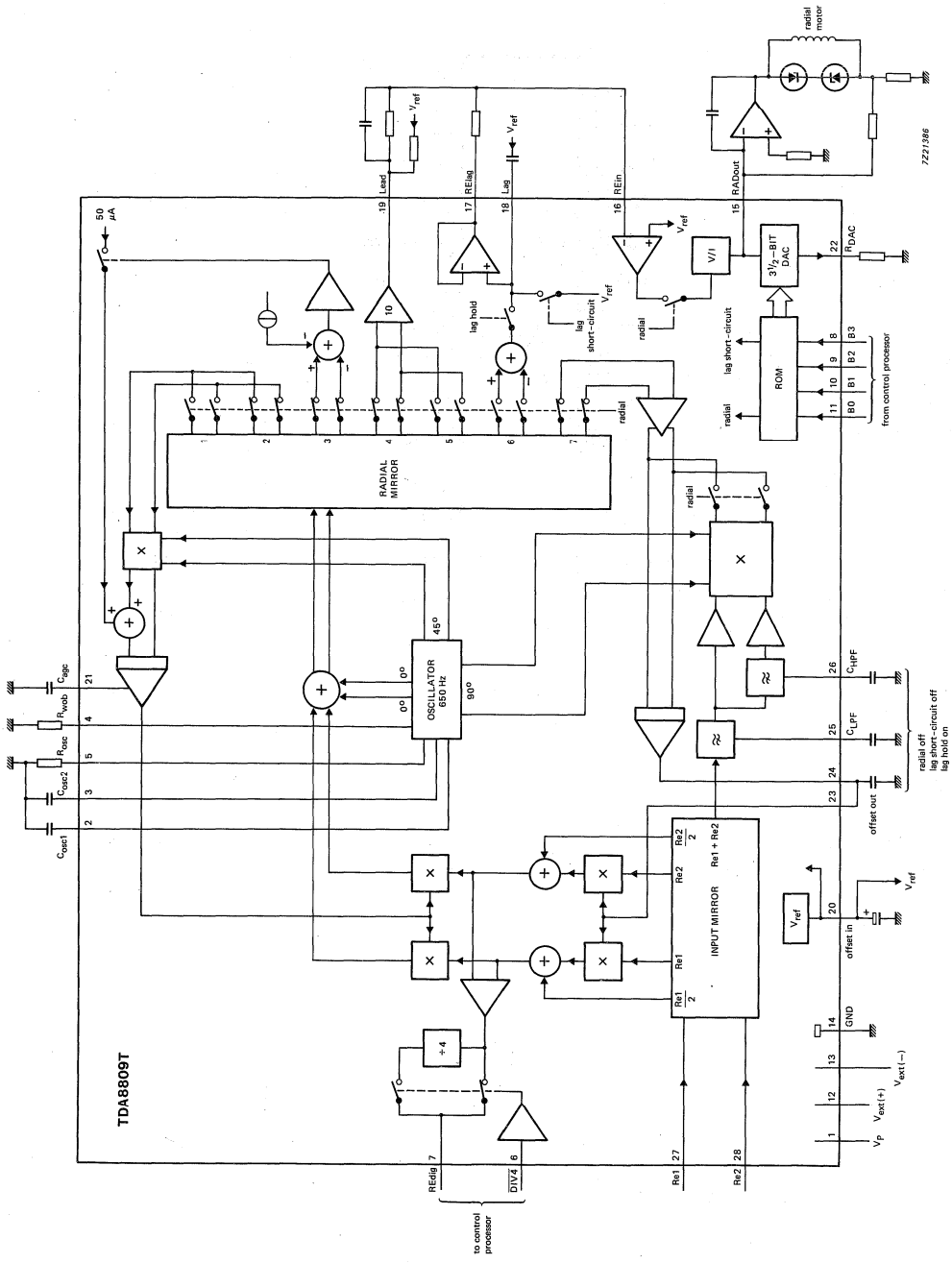


Fig. 1 Block diagram.

PINNING

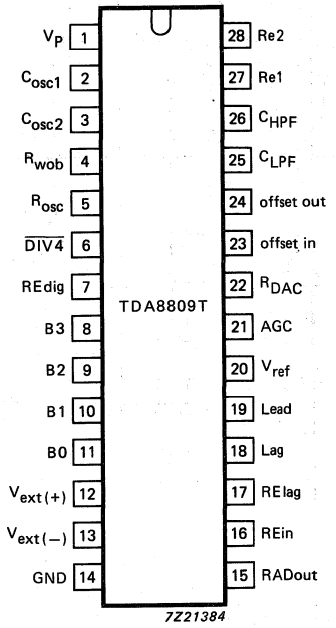


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	V_P	Positive supply voltage
2	C_{osc1}	Frequency setting capacitors for oscillator
3	C_{osc2}	
4	R_{wob}	Wobble generator input
5	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
6	$\overline{DIV4}$	Divide-by-4 input
7	REdig	Digital output of sign (Re2 - Re1)
8	B3	Input control bits for off-, catch-, play-status and DAC output current
9	B2	
10	B1	
11	B0	
12	$V_{ext(+)}$	Positive external voltage input
13	$V_{ext(-)}$	Negative external voltage input (also substrate connection)
14	GND	Negative supply connection
15	RADout	Current output of amplified (Re2 - Re1) input currents
16	REin	Radial error input
17	RElag	Voltage output of integrated (Re2 - Re1) input currents
18	Lag	Connection of integrator capacitor for (Re1 - Re2) input currents
19	Lead	Lead output
20	V_{ref}	Internal reference voltage output
21	AGC	Gain control input for radial error signal
22	R_{DAC}	Biassing resistor for current output for track jumping (3½ bits)
23	offset in	Offset control input for radial offset
24	offset out	Offset control output for radial offset
25	C_{LPF}	Low-pass filter for Re1 and Re2, used for radial offset control
26	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
27	Re1	Input for amplified currents from photo-diodes D1 and D2
28	Re2	Input for amplified currents from photo diodes D3 and D4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
pin 1 to pin 14	V_P	−0,3	13	V
pin 12 to pin 13	V_{ext}	−0,3	13	V
pin 14 to pin 13	$V_{ext(-)}$	−0,3	13	V
Output voltage ranges				
except RADout	V_O	0	V_P	V
RADout	V_O	$V_{ext(-)}$	$V_{ext(+)}$	V
R_{DAC} current range	I_{RDAC}	50	250	μA
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−30	+85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

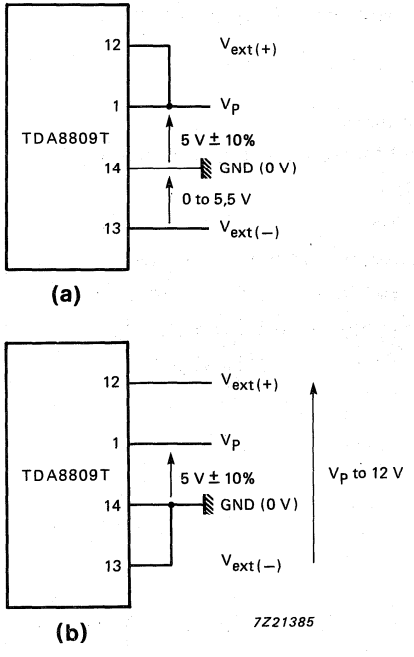


Fig. 3 Supply voltages;
(a) Home application (b) Car application.

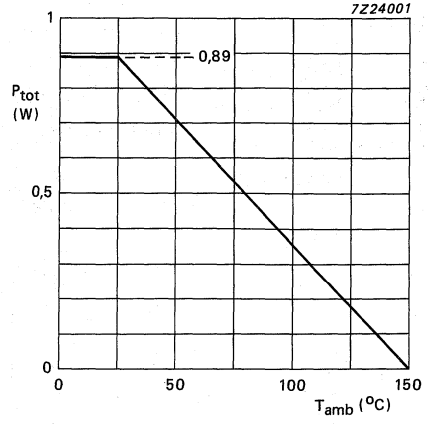


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; $V_{ext(+)}$ = + 5 V; $V_{ext(-)}$ = −5 V; I_{RDAC} (pin 22) = −75 μA; I_{Rwob} (pin 4) = −8 μA; I_{Rosc} (pin 5) = −50 μA; V_{RADout} = 0 V; $V_{offset\ in}$ = V_{lead} = V_{lag} = V_{Cosc1} = V_{Cosc2} = V_{ref}; $V_{offset\ in}$ is connected to $V_{offset\ out}$; T_{amb} = 25 °C; all voltages measured with respect to V_{GND}; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range (see Fig. 3)						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	4,0	5,3	6,6	mA
Reference output (V_{ref})						
Output voltage	$I_{Vref} \leqslant \pm 1$ mA	V_{ref}	2,25	2,45	2,65	V
Output impedance		$\lvert Z_O \rvert$	–	25	–	Ω
Reference input (R_{osc})						
Input voltage level	I_{Rosc} = −50 μA	V_{Rosc}	1,1	1,24	1,3	V
Input current		I_{Rosc}	–	−50	–	μA
Reference input (R_{DAC})						
Input voltage level	I_{RDAC} = −75 μA	V_{RDAC}	1,1	1,23	1,3	V
Input current		I_{RDAC}	–	−75	–	μA
Reference input (R_{wob})						
Input voltage level	I_{Rwob} = −8 μA	V_{Rwob}	150	165	180	mV
Input current		I_{Rwob}	–	−8	–	μA
REdig output (REdig)						
Output source current	note 1 (A)	I_{REdig}	–	−160	−50	μA
Output sink current	note 1 (B)	I_{REdig}	0,4	3,5	–	mA
Output voltage HIGH	I_{REdig} = −50 μA; note 1 (A)	V_{REdig}	2,4	–	–	V
Output voltage LOW	I_{REdig} = 400 μA; note 1 (B)	V_{REdig}	0	0,13	0,4	V

parameter	conditions	symbol	min.	typ.	max.	unit
Digital inputs						
B0, B1, B2 and B3						
Input voltage HIGH	note 2	V_{IH}	2,0	–	V_P	V
Input voltage LOW	note 2	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	0,03	1,0	μA
Input source current LOW		I_{IL}	−3,0	−0,1	0	μA
Divide-by-4 input ($\overline{DIV4}$)						
Input voltage HIGH	divide-by-1	V_{IH}	2,0	–	V_P	V
Input voltage LOW	divide-by-4	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	5,0	*	μA
Input source current LOW		I_{IL}	−10	−3	0	μA
Input frequency at Re1 and Re2		f_i	–	10	50	kHz
Radial error inputs (Re1; Re2)						
Input voltage level	$I_{Re1} = I_{Re2} = -110\,\mu A$	V_{Re1}, V_{Re2}	$V_P-1,81$	$V_P-1,71$	$V_P-1,61$	V
Input current		I_{Re1}, I_{Re2}	–	−110	–	μA
Input impedance		$\lvert Z_{Re1}\rvert, \lvert Z_{Re2}\rvert$	–	2,5	–	kΩ
Gain control input (AGC)	rad on; lag hold off					
Offset current	$V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = 0$	I_{AGC}	−0,2	0	0,2	μA
Lag current for	$I_{Re1} = -85\,\mu A$; $I_{Re2} = -115\,\mu A$					
minimum radial gain	$V_{AGC} = 0,6$ V	I_{lag}	−2,5	−0,45	+ 1,5	μA
maximum radial gain	$V_{AGC} = 3,8$ V	I_{lag}	−42	−30	−18	μA
Input impedance		$\lvert Z_{AGC}\rvert$	–	*	–	MΩ
Gain	$V_{AGC} = 3,8$ V; $V_{Cosc2} = V_{ref} + 1,4$ V; $V_{Cosc1} = V_{ref}$; $I_{Re1} = -100\,\mu A$; $I_{Re2} = -100\,\mu A$	I_{AGC0}	–	−2	–	μA
	$I_{Re1} - I_{Re2} = 4\,\mu A$ − I_{AGC0} then $I_{Re1} - I_{Re2} = -4\,\mu A$ − I_{AGC0}	$\frac{\Delta I_{AGC}}{\Delta(I_{Re1}-I_{Re2})}$	0,7	0,9	1,1	

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (continued)						
Radial error trackcrossing	rad off; V_{AGC} = 3,8 V; $I_{Re2}-I_{Re1}$ = −12 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	−3	0	3	μA
	$I_{Re2}-I_{Re1}$ = −48 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	39	49	59	μA
Offset control (offset out)						
Offset current	rad on; I_{CHPF} = 0; $I_{Re1}=I_{Re2}$ = −110 μA	$I_{offset\ out}$	−0,1	0	0,1	μA
Offset lag current for	rad on; lag hold off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA					
minimum amplification Re1 maximum amplification Re2	$V_{offset\ in}$ = V_{ref} − 1,2 V	I_{lag}	−115	−100	−85	μA
minimum amplification Re2 maximum amplification Re1	$V_{offset\ in}$ = V_{ref} + 1,2 V	I_{lag}	+ 85	+100	+115	μA
Offset lag current	note 3	I_{lag}	−7	0	+ 7	μA
Transconductance factor						
	rad off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}$ $V_{range\ offset\ in}$	0,17	0,21	0,25	
	rad off; $V_{AGC}=V_{GND}$ $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}$ $V_{range\ offset\ in}$	−0,1	0	0,1	
Input impedance		$\lvert Z_{offset\ in}\rvert$	−	*	−	MΩ
High-pass filter (C_{HPF})						
Voltage level at I_{CHPF} = 0	$I_{Re1}=I_{Re2}$ = 0; I_{CLPF} = 0	V_{CHPF}	V_P −0,82	V_P −0,72	V_P −0,62	V
Transresistance from Re1, Re2 to C_{HPF}	$I_{Re1}+I_{Re2}$ = −200 μA	$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}-I_{Re2})}$	−200	*	200	Ω
		$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}+I_{Re2})}$	6,2	8,8	11,5	kΩ
Input impedance		$\lvert Z_{CHPF}\rvert$	−	8	−	kΩ

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Low-pass filter (C_{LPF})						
Voltage level at $I_{CLPF} = 0$	$I_{Re1} = I_{Re2} = 0$	V_{CLPF}	4,7	–	V_P	V
Input impedance		$\|Z_{CLPF}\|$	–	8	–	kΩ
RElag output						
Output voltage range	$I_{RElag} = -200\ \mu A$; $V_{lag} = 4{,}25$ V	V_{RElag}	$V_P-1{,}1$	–	–	V
	$I_{RElag} = 200\ \mu A$; $V_{lag} = 0{,}9$ V	V_{RElag}	–	–	1,1	V
Maximum source current output	$V_{lag} = 4{,}1$ V	I_{RElag}	−6,0	−3,5	−1,0	mA
Maximum sink current output	$V_{lag} = 0{,}9$ V	I_{RElag}	2,5	4,1	5,5	mA
Output impedance	f = < 10 kHz	$\|Z_{RElag}\|$	–	–	50	Ω
Offset ($V_{RElag}-V_{ref}$)	lag short-circuit on; lag hold on	$V_{RElag\ offset}$	−10	–	10	mV
Transfer lag ⟶ RElag	f = < 10 kHz; lag short-circuit off; lag hold on	$\frac{V_{RElag}}{V_{lag}}$	−5%	1	5%	
Slew rate						
RElag output amplifier	lag short-circuit off; lag hold on	SR	–	0,4	–	V/μs
Lag push-pull current output, voltage input (pin 18)	note 4					
Output voltage	$I_{lag} = -20\ \mu A$; $V_{offset\ in} = V_{ref}-1{,}2$ V	V_{lag}	$V_P-1{,}5$	–	–	V
	$I_{lag} = 20\ \mu A$; $V_{offset} = V_{ref} + 1{,}2$ V	V_{lag}	–	–	1,5	V
Output impedance		$\|Z_{lag}\|$	–	*	–	MΩ
Switch lag short-circuit						
Impedance $\frac{\Delta V_{lag}}{\Delta I_{lag}}$	lag short-circuit on; lag hold on; $I_{lag} = \pm 100\ \mu A$	$\|Z_{lag\ sc}\|$	–	0,4	1	kΩ
Radial error input (REin)						
Input impedance	rad on	$\|Z_{REin}\|$	–	0	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RADout push-pull current output						
Output voltage	rad on I_{REin} = 180 μA; I_{RADout} = −50 μA	V_{RADout}	$V_{ext(+)}$−1,5	−	−	V
	I_{REin} = −180 μA; I_{RADout} = 50 μA	V_{RADout}	−	−	$V_{ext(-)}$+1,5	V
Current gain	rad on; I_{REin} = ± 100 μA	$\frac{I_{RADout}}{I_{REin}}$	−10%	1	10%	
Slew rate		SR	−	0,4	−	V/μs
Output impedance		$\lvert Z_{RADout} \rvert$	−	*	−	MΩ
Ratio of output current to reference current	I_{REin} = 0; I_{RDAC} = −75 μA; see also Table 1	$\frac{I_{RADout}}{I_{RDAC}}$	−5%	−0,5	+ 15%	
			−8%	−2	+ 12%	
			−0,02	0	0,02	
			−0,02	0	0,02	
			−14%	0,5	+ 6%	
			−12%	2	+ 8%	
			−0,1	0	0,1	
			−0,1	0	0,1	
			−5%	−0,5	+ 15%	
			−5%	−0,375	+ 15%	
			−5%	−0,25	+ 15%	
			−4%	−0,125	+ 16%	
			−14%	+ 0,5	+ 6%	
			−13%	+ 0,375	+ 7%	
			−13%	+ 0,25	+ 7%	
			−13%	+ 0,125	+ 7%	
Lead output	V_{AGC} = 3,8 V					
Output voltage	I_{Re1} = −90 μA; I_{Re2} = −100 μA; I_{lead} = −20 μA	V_{lead}	V_P−1,5	−	−	V
	I_{Re1} = −100 μA; I_{Re2} = −90 μA; I_{lead} = 20 μA	V_{lead}	−	−	1,5	V
Offset current	$I_{Re1} = I_{Re2}$ = −100 μA	$I_{lead\ offset}$	−100	0	100	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Lead output (continued)						
Current gain	$I_{Re1} = -120\ \mu A$; $I_{Re2} = -100\ \mu A$	$\frac{\Delta I_{lead}}{\Delta(I_{Re1}-I_{Re2})}$	−11,2	−9,9	−8,8	
Output impedance		$\lvert Z_{lead}\rvert$	–	*	–	MΩ
Oscillator						
(C_{osc1} and C_{osc2} connected to 12 nF capacitors)						
Amplitude oscillation (peak-to-peak value)						
C_{osc1}		$V_{osc1(p-p)}$	1,05	1,25	1,45	V
C_{osc2}		$V_{osc2(p-p)}$	1,05	1,25	1,45	V
Operating frequency	$I_{Re1} = I_{Re2} = -110\ \mu A$	f_{osc}	690	740	790	Hz
Output voltages (peak-to-peak value)						
0° injection						
lead (pin 19)	$R_{lead} = 10\ k\Omega$	$V_{lead(p-p)}$	0,85	1,05	1,25	V
C_{lag} (pin 18)	$R_{lag} = 10\ k\Omega$; rad on; lag hold off	$V_{lag(p-p)}$	85	105	125	mV
	rad on; lag hold on	$V_{lag(p-p)}$	–	0	20	mV
90° injection						
offset out	$I_{CHPF} = -100\ \mu A$; $R_{offset\ out} = 10\ k\Omega$; rad on	$V_{offset\ out}$ (p-p)	90	110	130	mV
45° injection						
AGC	$R_{agc} = 10\ k\Omega$; $V_{offset\ in} = V_{ref} + 1\ V$; rad on	$V_{AGC(p-p)}$	200	250	300	mV

Notes to the characteristics

1. REdig output conditions:
   (A) $I_{Re1} > I_{Re2} + 5\ \mu A$; (B) $I_{Re2} > I_{Re1} + 5\ \mu A$.
2. Input voltage HIGH indicates logic 1; Input voltage LOW indicates logic 0; see also Table 1.
3. $\overline{DIV4}$ = HIGH; $V_{offset\ in}$ adjusted for $V_{REdig} = 1,4$ V; rad on; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$.
4. Output voltage conditions are:
   rad on; lag short-circuit off; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$; $V_{offset} = V_{ref} - 1,2$ V.

Table 1 Truth table for DAC output current

functions	DAC output	logical inputs				internal switches		
	I_{REout}/I_{DAC}	B3	B2	B1	B0	lag s/c	rad	lag hold
PUSH	−1/2	0	0	0	0	off	off	on
(kick)	−2	0	0	0	1	off	off	off
OFF	0	0	0	1	0	off	off	on
OFF	0	0	0	1	1	on	off	off
PULL	1/2	0	1	0	0	off	off	on
(kick)	2	0	1	0	1	off	off	off
CATCH	0	0	1	1	0	off	on	on
PLAY	0	0	1	1	1	off	on	off
PUSH	−1/2	1	0	0	0	on	off	on
PUSH	−3/8	1	0	0	1	on	off	off
PUSH	−1/4	1	0	1	0	on	off	on
PUSH	−1/8	1	0	1	1	on	off	off
PULL	1/2	1	1	0	0	on	off	on
PULL	3/8	1	1	0	1	on	off	off
PULL	1/4	1	1	1	0	on	off	on
PULL	1/8	1	1	1	1	on	off	off

Where:

0 = input voltage LOW; 1 = input voltage HIGH.

Photo diode signal processor for compact disc players

TDA8900

APPLICATIONS

- Compatible for single and dual supply
- Suitable for home, car and portable applications

FEATURES

- Data amplifier with equalizer and AGC
- Offset-free preamplifier with AGC for the servo signals
- Track-loss detection
- Start-up procedure for focus
- Crosstalk reduction circuit to minimize radial error interference
- Laser supply amplifier and reference source
- Focus in-lock signal; Ready signal output (READY)
- AGC circuit with automatic start-up and wobble generator
- Tracking control for fast forward, reverse scan, repeat and pause functions.

GENERAL DESCRIPTION

The TDA8900 is a bipolar integrated circuit which has been designed for use in compact disc players that have a single spot read-out system. The IC processes the input data signals and the error signals for the focus and radial control network. Interfacing, with the control processor, is achieved via a serial specific bus. Feedback is achieved via an extra line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage range		4.5	–	13.0	V
V_{SS}	negative supply voltage range		−1.8	–	−1.3	V
I_Q	quiescent supply current	$V_{DD}-V_{SS}$ = 5 V	15	–	40	mA
I_D	LF input current for each diode input		0	50	–	µA
I_{LO}	laser supply output current		−6.5	–	−3.8	mA
T_{amb}	operating ambient temperature range		0	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8900	40	DIL	plastic	SOT129FG5

Photo diode signal processor for compact disc players

TDA8900

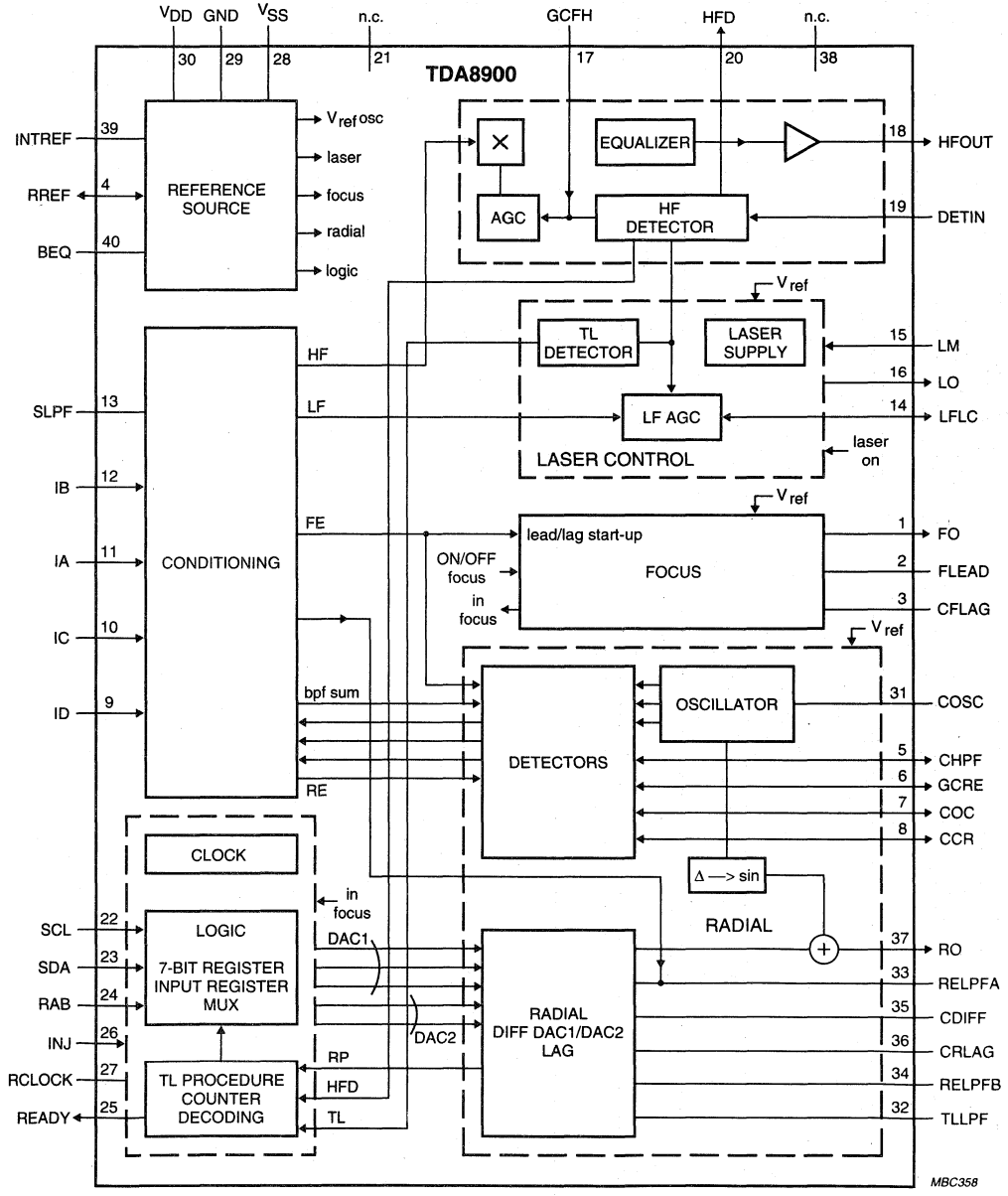


Fig.1 Block diagram.

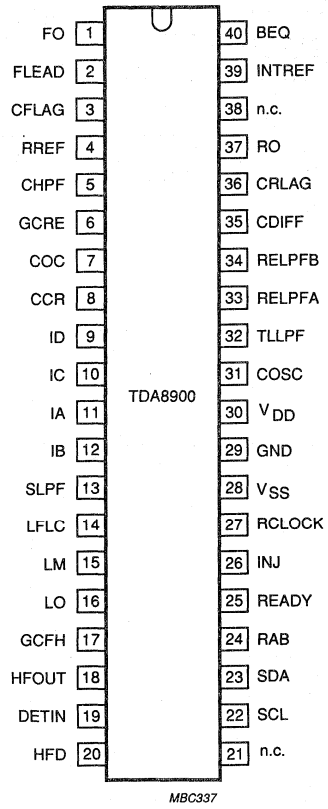


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
FO	1	focus output
FLEAD	2	focus loop lead filter
CFLAG	3	focus loop lag function
RREF	4	reference voltage output and current input
CHPF	5	high-pass filter for sum signal
GCRE	6	gain control voltage input of radial loop and current output of gain detector
COC	7	offset control voltage input of radial loop and current output of offset detector
CCR	8	crosstalk control voltage input and current output of crosstalk detector
ID	9	current input
IC	10	current input
IA	11	current input
IB	12	current input
SLPF	13	low-pass filter for sum signal and high-pass filter for HF signal
LFLC	14	laser power control voltage input/output
LM	15	laser monitor voltage input of diode current level detector
LO	16	laser power control current output
GCFH	17	gain control voltage input of HF part and current output of amplitude detector
HFOUT	18	HF amplifier output
DETIN	19	HF amplitude detector voltage input
HFD	20	HF amplitude detector output
n.c.	21	not connected
SCL	22	serial clock input
SDA	23	serial data input/output
RAB	24	data synchronization input
READY	25	message to microprocessor
INJ	26	injector input for I^2L logic
RCLOCK	27	logic oscillator frequency adjustment
V_{SS}	28	negative supply

SYMBOL	PIN	DESCRIPTION
GND	29	ground
V_{DD}	30	positive supply
COSC	31	wobble oscillator capacitor
TLLPF	32	radial error condition for track loss detection
RELPFA	33	pre-filter for radial signal
RELPFB	34	post-filter for radial signal
CDIFF	35	differential radial error signal
CRLAG	36	lag capacitor in radial part
RO	37	radial output
n.c.	38	not connected
INTREF	39	internal reference voltage
BEQ	40	equalizer current control

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

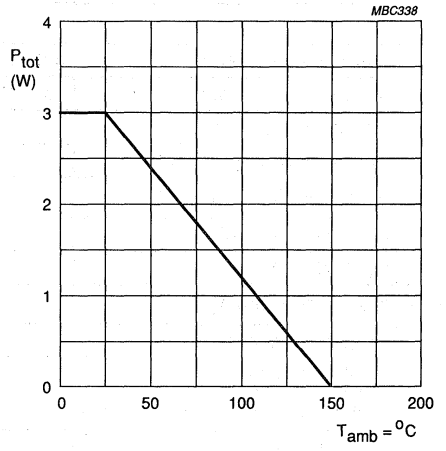


Fig.3 Power derating curve.

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}-V_{SS}	supply voltage		–0.3	13.0	V
V_{GND}-V_{SS}	voltage between pins 29 and 28	no current limiting	–0.3	1.5	V
V_O	output voltage range		V_{SS}	V_{DD}	V
P_{tot}	total power dissipation	see Fig.3			
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		0	+85	°C
T_j	operating junction temperature		–	150	°C

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply range	note 1	4.5	5.0	5.5	V
V_{SS}	negative supply range	note 1	−1.8	–	−1.3	V
I_{DD}	quiescent supply current		15	–	40	mA
I_{SS}	maximum supply current		−20	–	−5	mA
Reference input BEQ (pin 40)						
V_{40}	input voltage level		540	600	660	mV
I_{40}	input current range		−150	–	−10	µA
Reference input RREF (pin 4)						
V_4	input voltage level		1.1	1.2	1.4	V
I_4	input current level		–	−50	–	µA
Internal reference voltage INTREF (pin 39)						
V_{39}	output voltage range		1.8	1.95	2.1	V
R_{39}	output resistance	I_{39} = 1 mA	–	70	–	Ω
I_{39}	output current range		−1	–	+1	mA
Current inputs IA to ID (pins 9 to 12)						
$V_{9\text{-}12}$	input voltage level	IA to ID = 50 µA	–	0.6	–	V
$R_{9\text{-}12}$	input resistance		–	500	–	Ω
$I_{9\text{-}12}$	input current		0	–	150	µA
HF amplifier and equalizer						
AC CHARACTERISTICS						
TR_{18}	transresistance (pin 18)	$V_{17} \geq V_{39} + 1$	10	–	–	Ω
	V_{18} divided by ΣI_I	note 2; $V_{17} \leq V_{39} - 1$	–	–	0	kΩ
SR_{18}	slew rate (pin 18)	AC coupled; Z_O = 3 kΩ	6	–	–	V/µs
Δf	frequency range where the group delay is flat		0.2	–	1	MHz
		I_{40} = −80 µA	0.2	–	2	MHz
G	amplitude characteristic	note 3; I_{40} = −80 µA; 400 kHz to 2 MHz	4.5	–	7.5	dB
$V_{18(p\text{-}p)}$	AC output voltage (peak-to-peak value)	AGC loop closed	–	1.0	–	V
Z_{18}	output impedance		–	200	–	Ω
Δτ	flatness group delay		−10	–	+10	ns
		I_{40} = 80 µA	−5	–	+5	ns
DC CHARACTERISTICS						
V_{18}	output voltage		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain control HF part GCHF (pin 17)						
$V_{17\ max}$	input voltage for maximum gain		–	V_{39}+0.75	–	V
$V_{17\ min}$	input voltage for minimum gain		–	V_{39}–0.75	–	V
R_{17}	input resistance	–0.75 V < V_{17}–V_{39} < +0.75 V	25	–	–	MΩ
HF amplitude detector						
DETECTOR INPUT DETIN (PIN 19)						
V_{19}	output voltage level		–	2.1	–	V
$V_{ref(pos)}$	positive voltage reference level (input to output)		–10%	0.57	+10%	V
$V_{ref(neg)}$	negative voltage reference level (output to input)		–5%	$V_{ref(pos)}$	+5%	V
R_{19}	input resistance		–	9	–	kΩ
Detector output GCHF (pin 17) (see Fig.5)						
I_{17}	detector output current	note 4	–	+100	–	μA
		note 5	–	–5	–	μA
HFD output (digital) (pin 20) (see Figs 4 and 5)						
SWL_{20}	relative switching levels for $V_{19(pos)}/V_{ref(pos)}$ and $V_{19(neg)}/V_{ref(neg)}$		57.5	62.5	67.5	%
t_d	delay		–	8	–	μs
V_{OH}	HIGH level output voltage	note 6; I_{20} = –50 μA	2.4	–	V_{DD}–0.5	V
V_{OL}	LOW level output voltage	note 7; I_{20} = 400 μA	–	0.15	0.4	V
I_{OH}	HIGH level output current	note 8; V_{20} = 2.4 V	–	–80	–50	μA
I_{OL}	LOW level output current	note 9; V_{20} = 0.4 V	0.4	1.6	–	μA
Laser output LO (pin 16)						
V_{16}	output voltage range	I_O = 1 mA	V_{SS}–0.3	–	V_{DD}–0.5	V
R_{16}	output resistance	laser off	–	30	–	kΩ
I_{leak}	output leakage current	V_{16} = GND	–10	–	–	μA
$I_{16\ max}$	maximum output current		–6.5	–	–3.8	mA
Laser monitor (pin 15)						
V_{15}	input voltage	laser on; loop closed	–10%	1.8	+10%	V
I_{bias}	input bias	$V_{14} > V_{39}$ + 1	–2	–	0	μA
G	transconductance (LM to LO)	$V_{14} > V_{39}$ + 1	–	0.5	–	S
G	gain (V_{14} to V_{15})		–	0.24	–	
Low-pass filter SLPF (pin 13)						
H	transfer from ΣI_I to SLPF ($\Delta I_{13}/\Delta\Sigma I_I$)	note 2; $V_{13} = V_{39}$	–5%	0.25	+5%	
R_{13}	output resistance		13	14.5	16	kΩ

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Laser power control LFLC (pin 14)						
H	transfer from ΣI_I to I_{14}	$V_{19\ in}-V_{19\ out} > 0.65$ V $V_{19\ in} = V_{19\ out}$	−6% 0	0.25 0	+6% 0	
I_{14}	current level		−5.5	–	+25	μA
R_{14}	output resistance		–	25	–	MΩ
V_{14}	active voltage range		$V_{39}-0.75$	–	$V_{39}+0.75$	V
Offset detector COC (pin 7)						
H	transfer from V_{33} to I_7		–	10	–	μS
V_7	active voltage range		$V_{39}-0.75$	–	$V_{39}+0.75$	V
I_7	output current	RAD ON	−10	–	+10	μA
R_7	output resistance	RAD ON	– –	50 –	– 1	MΩ kΩ
High-pass filter CHPF (pin 5)						
H	transfer from ΣI_I to V_5	$\Sigma I_I < 350$ μA	–	4.1	–	kΩ
R_5	output resistance		–	8.2	–	kΩ
Crosstalk detector CCR (pin 8)						
V_8	active voltage range	laser ON; RAD ON	$V_{39}-0.75$	–	$V_{39}+0.75$	V
I_8	output current	RAD ON $V_8 > V_{39}$ +0.2 V $V_8 < V_{39}$ −0.2 V	−10 −20% +20%	– 0.8 −0.8	+10 +20% −20%	μA μA μA
R_8	output resistance	RAD ON	– –	50 120	– –	MΩ kΩ
Gain control GCRE (pin 6)						
V_6	active voltage range		$V_{39}-0.75$	–	$V_{39}+0.75$	V
I_6	output current	RAD ON	−10	–	+10	μA
R_6	output resistance	RAD ON	– –	50 –	– 1	MΩ kΩ
I_6	output current	$V_{33}-V_{39} > 0.75$ V $V_{33}-V_{39} < 0.75$ V	– –	110 −2	– –	μA μA
Focus (pins 1, 2 and 3) (note 10)						
TRANSFERS FROM INPUT CURRENTS TO CFLAG AND FLEAD (ΣI_I = 100 μA; FOCUS START 1 AND 2)						
I_{3ref}	I_{CFLAG}/FE		–	5	–	μA
V_{2ref}	V_{FLEAD}/FE		–	0.5	–	V
H	transfer from V_3 to I_1		–	100	–	μS
H	transfer from I_2 to I_1	focus start 1 and 2	–	−1	–	

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSFER FROM V_3 TO I_3 (ΔOSC)						
$\|I_3\|$	during focus start	focus start 1 focus start 2	–20% –20%	5.5 1.4	+20% +20%	µA µA
$\|V_{det}\|$	detection voltage during focus start		–	0.75	–	V
H	transfer from input to FO (I_{FO}/FE)	R_{FLAG} = 100 kΩ; R_{FLEAD} = ∞; focus start 1 and 2	–5%	47	+5%	µA
H	transfer from input to FO (I_{FO}/FE)	R_{FLAG} = 0; R_{FLEAD} = 10 kΩ; focus start 1 and 2	–5%	50	+5%	µA
Active voltage ranges						
V_3	linear range pin 3		V_{39}–0.75	–	V_{39}+0.75	V
V_2	linear range pin 2		V_{39}–0.75	–	V_{39}+0.75	V
V_1	linear range pin 1	$\|I_1\|$ < 250 µA	V_{SS}+1	–	V_{DD}–1	V
Impedance						
R_3	output resistance pin 3	focus start 2 focus start 1	50 –	– –	– 1	MΩ kΩ
R_2	output resistance pin 2		–	–	10	Ω
Current levels						
I_2	current range pin 2		–250	–	+250	µA
I_1	current range pin 1		–250	–	+250	µA
I_{3OS}	offset current pin 3	IA = IB = IC = ID = 50 µA	–300	0	+300	nA
V_{2OS}	voltage offset pin 2		–20	0	+20	mV
RADIAL PART						
VOLTAGE RANGES						
V_{33}	pre-filter for radial signal		V_{39}–0.75	–	V_{39}+0.75	V
V_{34}	post-filter for radial signal		V_{39}–0.75	–	V_{39}+0.75	V
V_{35}	differential radial error signal		V_{39}–0.75	–	V_{39}+0.75	V
V_{36}	lag capacitor		V_{39}–0.75	–	V_{39}+0.75	V
V_{37}	radial output		V_{SS}+1	–	V_{DD}–1	V
TRANSFERS						
K1	transfer ΣI_i to I_{33}	I_{33} = K1 (IA+IB–IC–ID) + K2 x ΣI_i V_6–V_{39} = 0.7 V V_6–V_{39} = –0.7 V	 – –	 0.67 0	 – –	
K2		V_7–V_{39} = 0.7 V V_7–V_{39} = –0.7 V	– –	0.5 –0.5	– –	
H	transfer from V_{33} to V_{35}		–5%	1	+5%	
V_{35OS}	voltage offset pin 35	V_{33} = V_{39}	–150	0	+150	mV

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSFERS						
H	transfer from I_{35} to I_{34}	$\|I_{35}\| < 200\ \mu A$	−10%	1	+10%	
H	transfer from V_{33} to I_{34}	pin 35 not connected	−10%	23.5	+10%	µS
I_{34OS}	offset current	pin 35 not connected	−1	0	+1	µA
H	transfer from V_{34} to I_{36}	$V_{34}-V_{39} \leq 0.1$ V	−20%	100	+20%	µS
I_{36}	input current	$V_{34}-V_{39} \geq 0.15$ V	−	10	−	µA
I_{36OS}	offset current pin 36	$V_{34} = V_{39}$	−1.5	0	+1.5	µA
H	transfer from					
	V_{34} to I_{37}	$V_{36} = V_{39}$	−10%	235	+10%	µS
	V_{36} to I_{37}	$V_{34} = V_{39}$	−10%	235	+10%	µS
I_{37OS}	offset current pin 37		−10	0	+10	µA
	input resistance for					
R_{33}	RELPFA pin 33		10	−	−	MΩ
R_{34}	RELPFB pin 34		10	−	−	MΩ
C_{35}	CDIFF pin 35		−	120	−	Ω
C_{36}	CRLAG pin 36		50	−	−	MΩ
Wobble oscillator						
I_{37}	output current pin 37	RAD ON	−	3.5	−	µA
f_{37}	input frequency pin 37	$C_{31} = 3.6$ nF	−10%	350	+10%	Hz
THD	total harmonic distortion		−	−	3	%
Radial polarity signal (RP)						
HY	hysteresis	see Fig.6	−	−	0.4	V
I_{37}	DAC2 currents	commands				
	DAC2+	DAC2+	−	50	−	µA
	DAC2++	DAC2++	−	170	−	µA
	DAC2−	DAC2−	−	−50	−	µA
	DAC2− −	DAC2− −	−	−170	−	µA
I_{34}	DAC1 currents	pin 35 not connected; commands				
	DAC1+	jump 4 (D = 1)	−	−60	−	µA
	DAC1++	jump 16 (D = 1)	−	−120	−	µA
	DAC1−	jump 4 (D = 0)	−	60	−	µA
	DAC1− −	jump 16 (D = 0)	−	120	−	µA
OSCILLATOR FREQUENCY ADJUSTMENT RCLOCK (NOT CONNECTED)						
Injector input INJ (pin 26)						
V_{26}	input voltage level	$I_{26} = 2.4$ mA	−	1.4	−	V
I_{26}	current in logic part		−	2.4	−	mA

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOGIC INPUTS (CL, DA and RAB) (pins 22, 23 and 24)						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.3	V
I_I	input current		−1	–	+1	µA
t_d	write data delay time		2	–	–	µs
t_{SU}	RAB set-up time (pin 24)		2	–	–	µs
t_{HD}	RAB hold time (pin 24)		2	–	–	µs
f_{CLK}	clock frequency		–	–	100	kHz
LOGIC OUTPUTS (READY and HFD) (pins 25 and 20)						
V_{OL}	LOW level output voltage	I_{OL} = 400 µA	–	0.15	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −50 µA	2.4	–	V_{DD}−0.6	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	0.4	1.6	–	mA
I_{OH}	HIGH level output current	V_{OH} = V_{DD}−0.5 V	–	−80	−50	mA
CONDITIONS ON THE PINS						
V_H	voltage POR HIGH		–	–	1.5	V
V_L	voltage POR LOW		2.3	–	–	V
V_H	voltage LASERIN HIGH		0.15	–	–	V
V_L	voltage LASERIN LOW		–	–	0.1	V
I_H	current INFOCUS HIGH	IA = ID = 0	12	–	–	µA
I_L	current INFOCUS LOW	IA = ID = 0	–	–	7	µA
V_L	voltage TLREN LOW	RAD ON; V_{19} = V_{39}; IA to ID = 75 µA	320	–	–	mV
		V_{32}−V_{39} = 350 mV; IA to ID = 75 µA	–	–	280	mV
I_L	current TLREN LOW	V_{19} = V_{39}; V_{32}−V_{39} = 350 mV; IA = IB = IC = ID	60	–	–	µA
V_H	voltage TLREN HIGH	RAD ON; V_{19} = V_{39}; IA to ID = 75 µA	–	–	220	mV
		V_{32}−V_{39} = 350 mV; IA to ID = 75 µA	340	–	–	mV
I_H	current TLREN HIGH	V_{19} = V_{39}; V_{32}−V_{39} = 350 mV; IA = IB = IC = ID	–	–	50	µA

Notes to the characteristics

1. V_{SS} can be connected to ground
2. $\Sigma I_I = IA + IB + IC + ID$
3. $gain = 20 \log \frac{V_{01}}{V_{02}}$
4. $V_{19\ out} - V_{19\ in} > V_{ref(neg)}$ or $V_{19\ in} - V_{19\ out} > V_{ref(pos)}$
5. $-V_{ref(neg)} < V_{19\ in} - V_{19\ out} < V_{ref(pos)}$
6. $V_{19\ neg} < V_{19\ out} - V_{19\ in}$ or $V_{19\ pos} < V_{19\ in} - V_{19\ out}$
7. $-V_{19\ neg} < V_{19\ in} - V_{19\ out} < V_{19\ pos}$
8. $V_{19\ neg} < V_{19\ out} - V_{19\ in}$ or $V_{19\ pos} < V_{19\ in} - V_{19\ out}$
9. $-V_{19\ neg} < V_{19\ in} - V_{19\ out} < V_{19\ pos}$
10. $FE = \frac{I_I - IB}{IA + IB} - \frac{IC - ID}{IC + ID}$

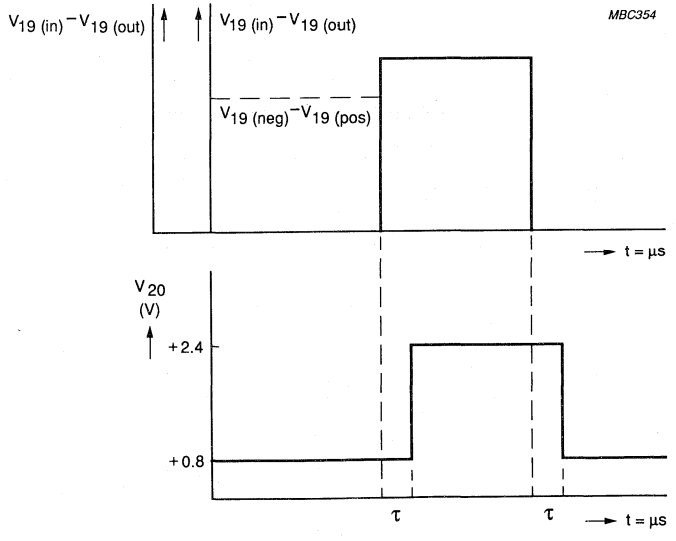


Fig.4 Definition of delay time.

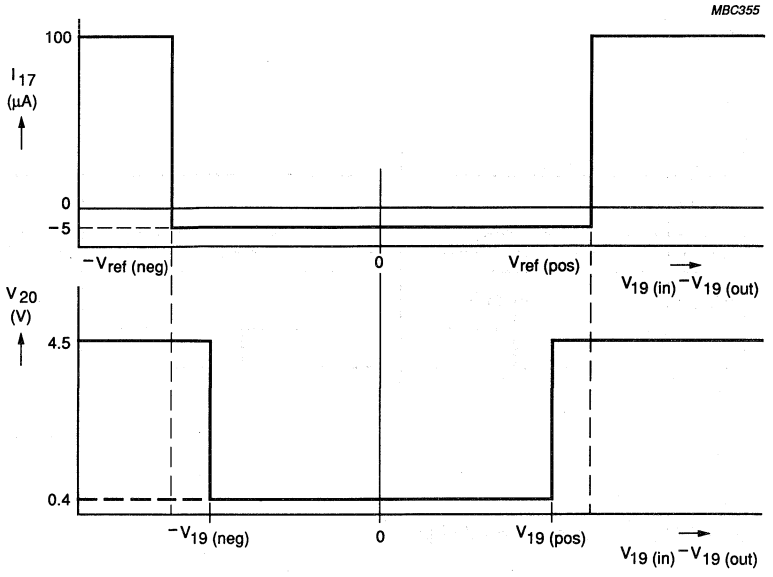


Fig.5 Definition of HF detector.

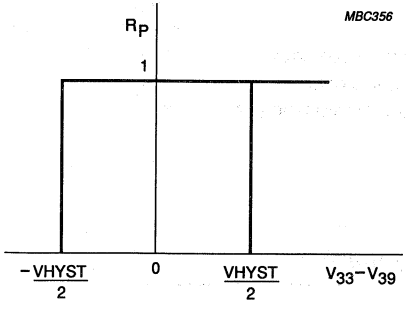
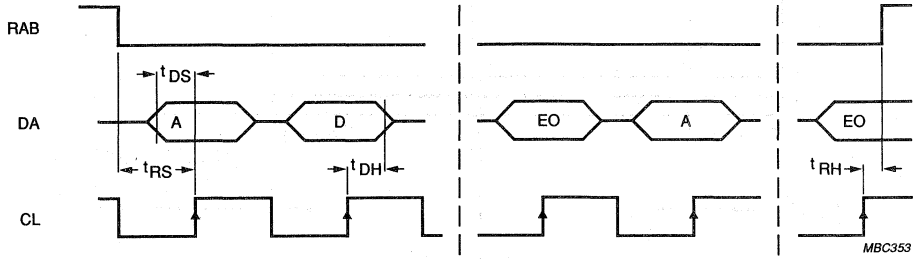


Fig.6 RP signal.



DA = data; CL = clock; RAB = request acknowledge.

Fig.7 Timing diagram.

Logic part

Timing of microprocessor interface

The timing diagram for writing data into the TDA8900 is illustrated in figure 7.

TDA8900 CONTROL

The status of the TDA8900 is controlled by the data signal DA. A list of commands and codes is given in Table 1. These commands set and reset flip-flops in the status register; jump commands are indicated by numbers only. These numbers are loaded into a 15-bit counter. A READY signal is generated from a number of commands thus indicating that a command has been executed.

The status of the output pin READY is controlled by the internal logic signals POR,LASERIN, INFOCUS and TLREN. Table 2 lists the logic signals and their control pins.

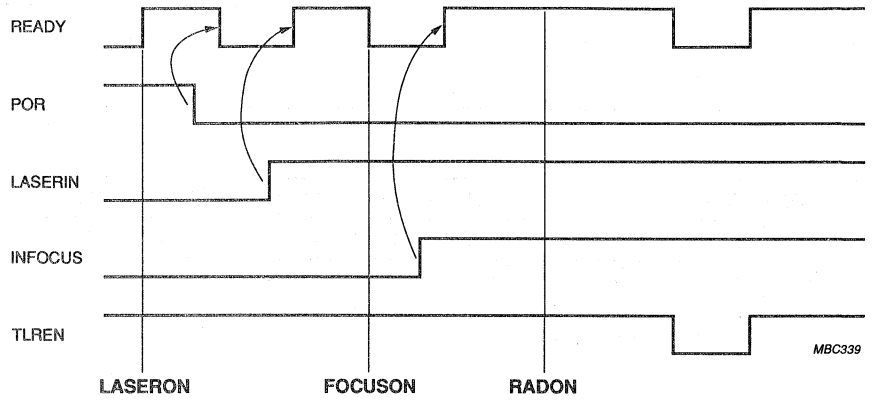


Fig.8 Sequence of the READY signal during system start-up.

Table 1 List of codes

COMMAND								ACTION
E0	E1	E2	E3	M0	M1	D	A	
X	X	X	X	X	X	X	0	wrong address (no action)
0	0	0	0	0	0	D	1	jump 1
0	0	0	0	0	1	0	1	radial reset
0	0	0	0	0	1	1	1	DAC2+
0	0	0	0	1	0	0	1	DAC2++
0	0	0	0	1	0	1	1	DAC2–
0	0	0	0	1	1	0	1	DAC2– –
0	0	0	0	1	1	1	1	radial ON
1	1	1	1	0	0	0	1	focus start 1
1	1	1	1	0	0	1	1	focus start 2
1	1	1	1	0	1	0	1	sfj
1	1	1	1	0	1	1	1	TLREN ON ready
1	1	1	1	1	0	0	1	laser ON
1	1	1	1	1	0	1	1	laser ON
1	1	1	1	1	1	0	1	no action
1	1	1	1	1	1	1	1	no action

Table 2 Logic signals

LOGIC SIGNAL	CONTROL PINS
POR	16
LASERIN	15
INFOCUS	9 to 12
TLREN	9 to 12, 19 and 32

Table 3 Jump instructions

COMMAND								M0	M1	M0	M1	M0	M1	M0	M1
E0	E1	E2	E3	M0	M1	D	A	0	0	1	0	0	1	1	1
1	0	0	0	M0	M1	D	1	-	2	-	2	-	3	-	3
0	1	0	0	M0	M1	D	1	-	4	-	5	-	6	-	7
1	1	0	0	M0	M1	D	1	-	8	-	10	-	12	-	14
0	0	1	0	M0	M1	D	1	-	16	-	20	-	24	-	28
1	0	1	0	M0	M1	D	1	-	32	-	40	-	48	-	56
0	1	1	0	M0	M1	D	1	-	64	-	80	-	96	-	112
1	1	1	0	M0	M1	D	1	-	128	-	160	-	192	-	224
0	0	0	1	M0	M1	D	1	-	256	-	320	-	384	-	448
1	0	0	1	M0	M1	D	1	-	512	-	640	-	768	-	896
0	1	0	1	M0	M1	D	1	-	1024	-	1280	-	1536	-	1792
1	1	0	1	M0	M1	D	1	-	2048	-	2560	-	3072	-	3584
0	0	0	1	M0	M1	D	1	-	4096	-	5120	-	6144	-	7168
1	0	1	1	M0	M1	D	1	-	8192	-	10240	-	12288	-	14336
0	1	1	1	M0	M1	D	1	-	16384	-	20480	-	24576	-	28672

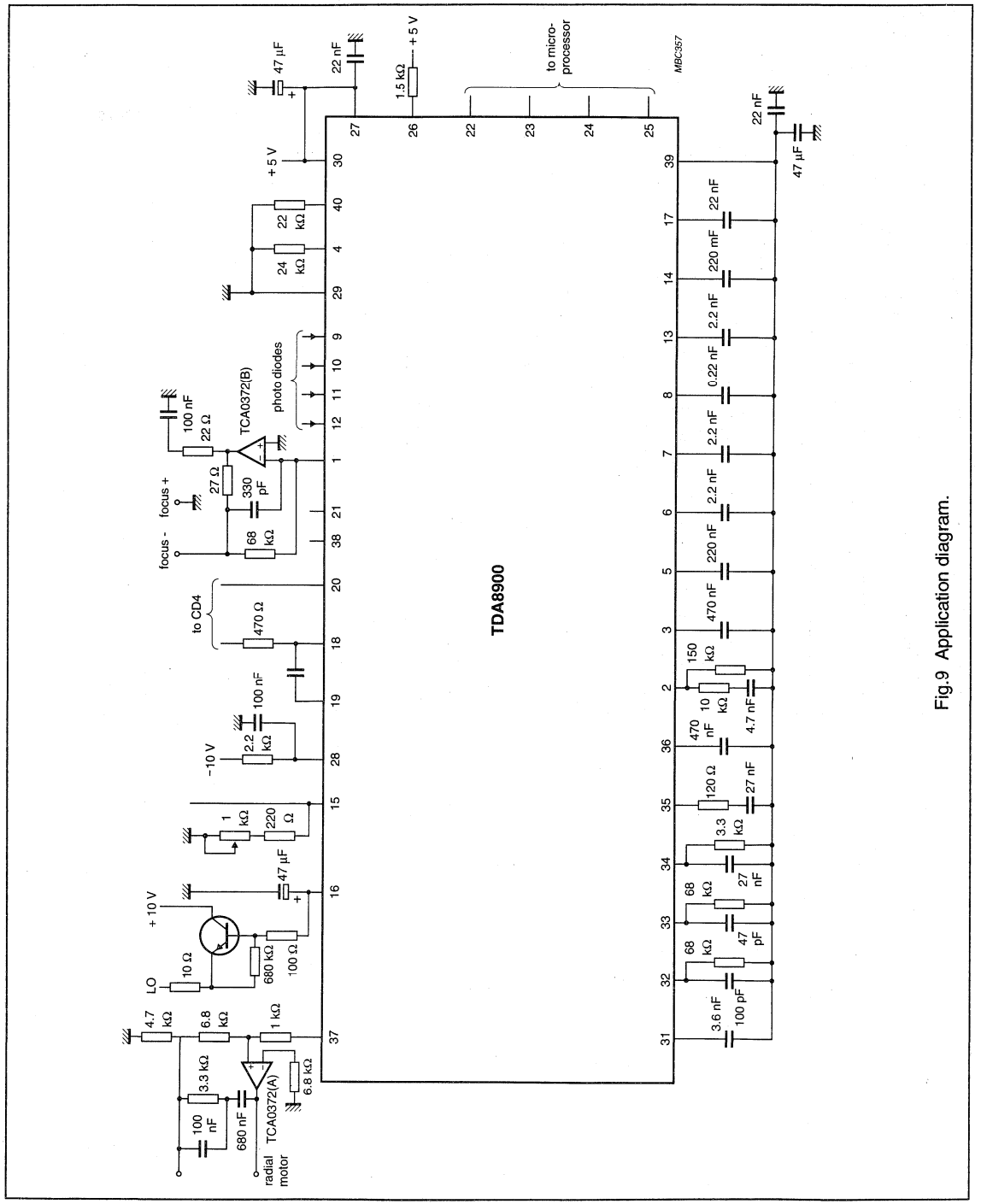


Fig.9 Application diagram.

Data sheet	
status	Product specification
date of issue	September 1990

TEA0655

Dual Dolby* B-type noise reduction circuit for playback applications

FEATURES

- Dual noise reduction channels
- Head preamplifiers
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV

GENERAL DESCRIPTION

The TEA0655 is an integrated circuit that provides two Dolby B-type noise reduction channels for playback applications in car radios. The TEA0655 includes head and equalization amplifiers with electronically switched time constants. The device will operate with power supplies in the range 9 to 15 volts, the output overload level increasing with an increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF, therefore it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range	8	–	15	V
I_{CC}	supply current	–	20	25	mA
(S+N)/N	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0655	20	DIL	plastic	SOT146

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

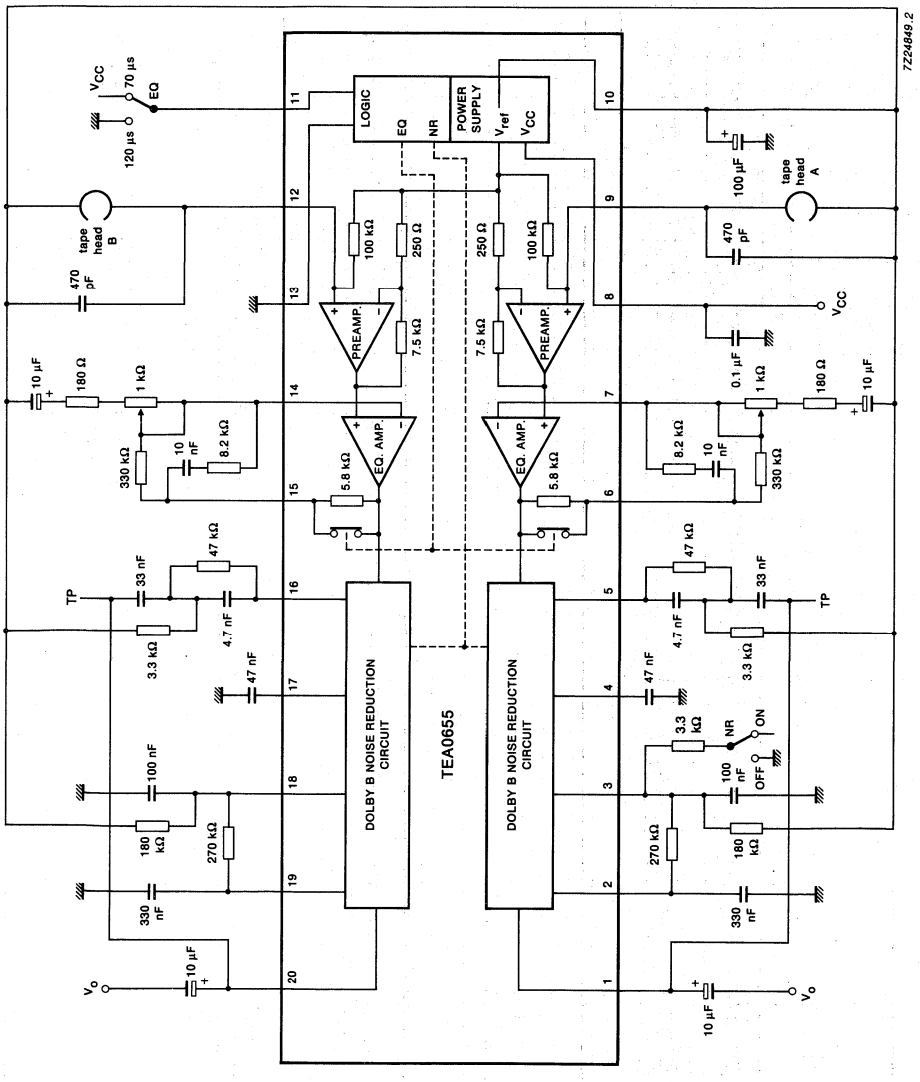


Fig.1 Block and application diagram.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 3 is open-circuit and disabled when pin 3 is connected to GRD (pin 13) via a 3.3 kΩ resistor (see Fig.1).

Pin 3 performs the functions of a logic input for noise reduction switching for both channels. It also provides smoothing for the control signal in one channel. It is important that no voltage is applied to pin 3 when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel. Time constant switching is achieved by applying a DC voltage to pin 11.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
EQA	6	equalizing output channel A
EQFA	7	equalizing input channel A
V_{CC}	8	voltage supply
INA	9	input channel A
V_{ref}	10	reference voltage
SWEQ	11	equalizing switch
INB	12	input channel B
GRD	13	ground
EQFB	14	equalizing input channel B
EQB	15	equalizing output channel B
SCB	16	side chain channel B
HPB	17	high-pass filter channel B
CONTRB	18	control voltage channel B
INTB	19	integrating filter channel B
OUTB	20	output channel B

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	16	V
V_I	input voltage (pins 1 to 20)	−0.3	V_{CC}	V
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C
V_{es}	electrostatic handling *	–	–	–

* Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V = ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

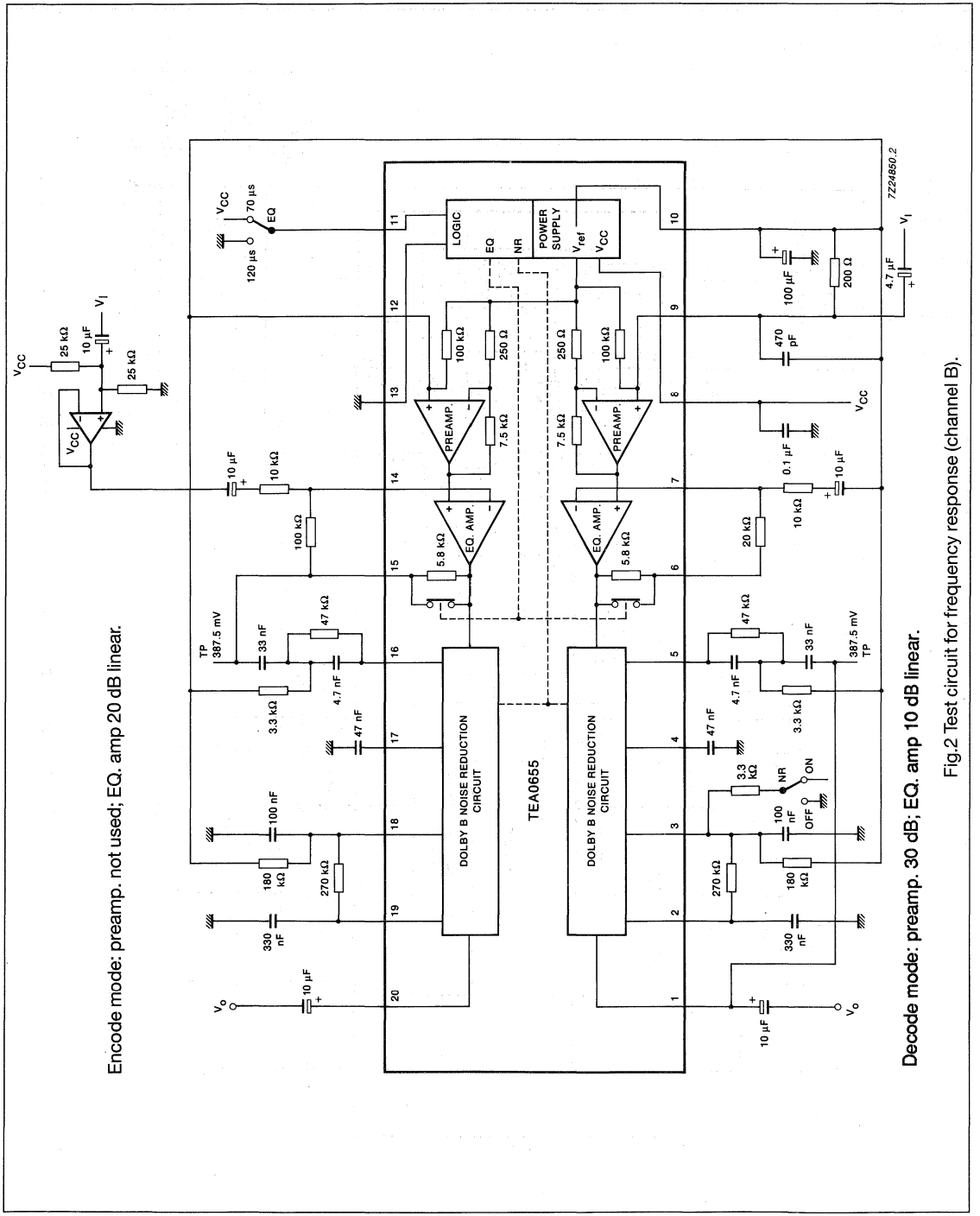
V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels referenced to 387.5 mV RMS (0 dB) at test point (TP) (pin 1 or 20); test circuit Fig.1; NR ON; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8	10	15	V
I_{CC}	supply current		–	20	25	mA
	channel matching	NR OFF	–0.5	–	+0.5	dB
THD	distortion 2nd and 3rd harmonic	f = 1 kHz; 0 dB	–	0.08	0.15	%
		f = 10 kHz; +10 dB	–	0.15	0.3	%
	signal handling	V_{CC} = 8 V; 1% distortion at 1 kHz	12	15	–	dB
(S+N)/N	signal-plus-noise to noise ratio (see Fig.2; decode mode)	internal gain 40 dB linear; CCIR/ARM weighted	78	84	–	dB
PSRR	power supply ripple rejection	f = 1 kHz; 250 mV; see Fig.3	52	57	–	dB
	frequency response measured in encode mode see Fig.2 referenced to test point	note 1				
		f = 1 kHz; 0 dB	–1.5	0	+1.5	dB
		f = 1 kHz; –25 dB	–17.8	–19.3	–20.8	dB
		f = 0.2 kHz; –25 dB	–22.9	–24.4	–25.9	dB
		f = 5 kHz; –25 dB	–18.1	–19.6	–21.1	dB
		f = 10 kHz; –35 dB	–24.4	–25.9	–27.4	dB
α_{CR}	channel separation	f = 1 kHz; see Fig.4	57	63	–	dB
R_{Lmin}	minimum load resistance on output (pins 1 and 20)	12 dB; 1 kHz; 1% THD	10	–	–	kΩ
G_V	voltage gain (pin 9 to 7 or pin 12 to 14)	1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance pins 9 and 12		60	100	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_V	open loop gain pins 12/15 and pins 9/6	10 kHz	80	86	–	dB
		400 kHz	104	110	–	dB
	DC output voltage pins 1 and 20	NR OFF with reference to $V_{CC}/2$	–	–	±0.15	V
Z_O	output impedance		–	50	70	Ω
I_{OGRD}	DC output current capability	to ground	–	–	–2	mA
I_{OVCC}		to V_{CC}	–	–	300	μA
En	equivalent input noise voltage (RMS value)	NR OFF; unweighted; 20 Hz to 20 kHz; $R_S = 0\ \Omega$	–	0.7	1.4	μV
Switching thresholds						
V_{OFF}	NR switch OFF (pin 3)		0	–	$0.2V_{CC}$	V
I_3	NR switch ON		–	open	–100	nA
	equalizing (EQ) switch (pin 11) at 70 μs		$0.5V_{CC}$	–	V_{CC}	V
	equalizing switch at 120 μs		0	–	$0.2V_{CC}$	V
I_{11}	input current		–	–	–1	μA

Note to the characteristics

1. Equals the corresponding decode mode cut with reference to test point level, see Fig.1.



Encode mode: preamp. not used; EQ. amp 20 dB linear.

Decode mode: preamp. 30 dB; EQ. amp 10 dB linear.

Fig.2 Test circuit for frequency response (channel B).

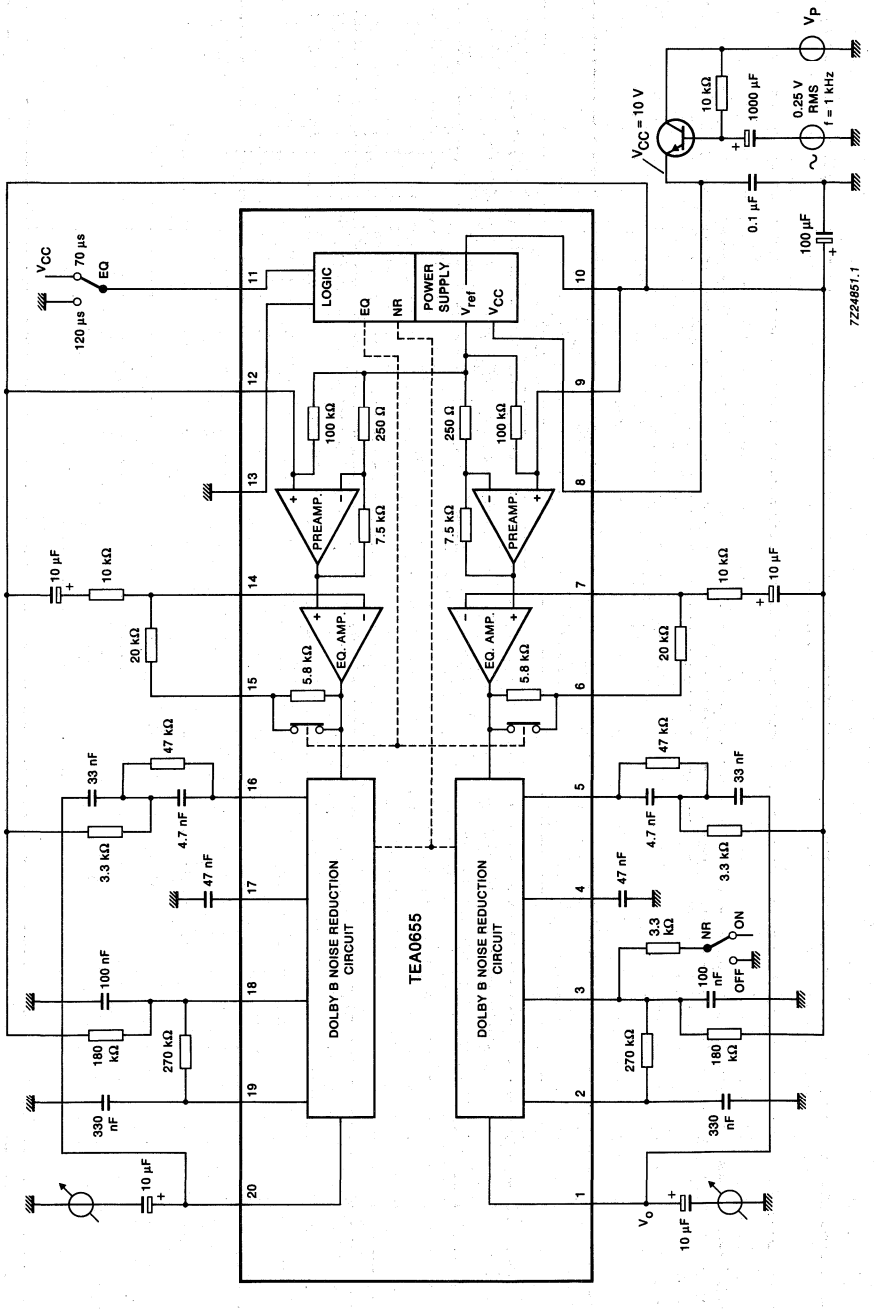


Fig.3 Test circuit for power supply ripple rejection (PSRR).

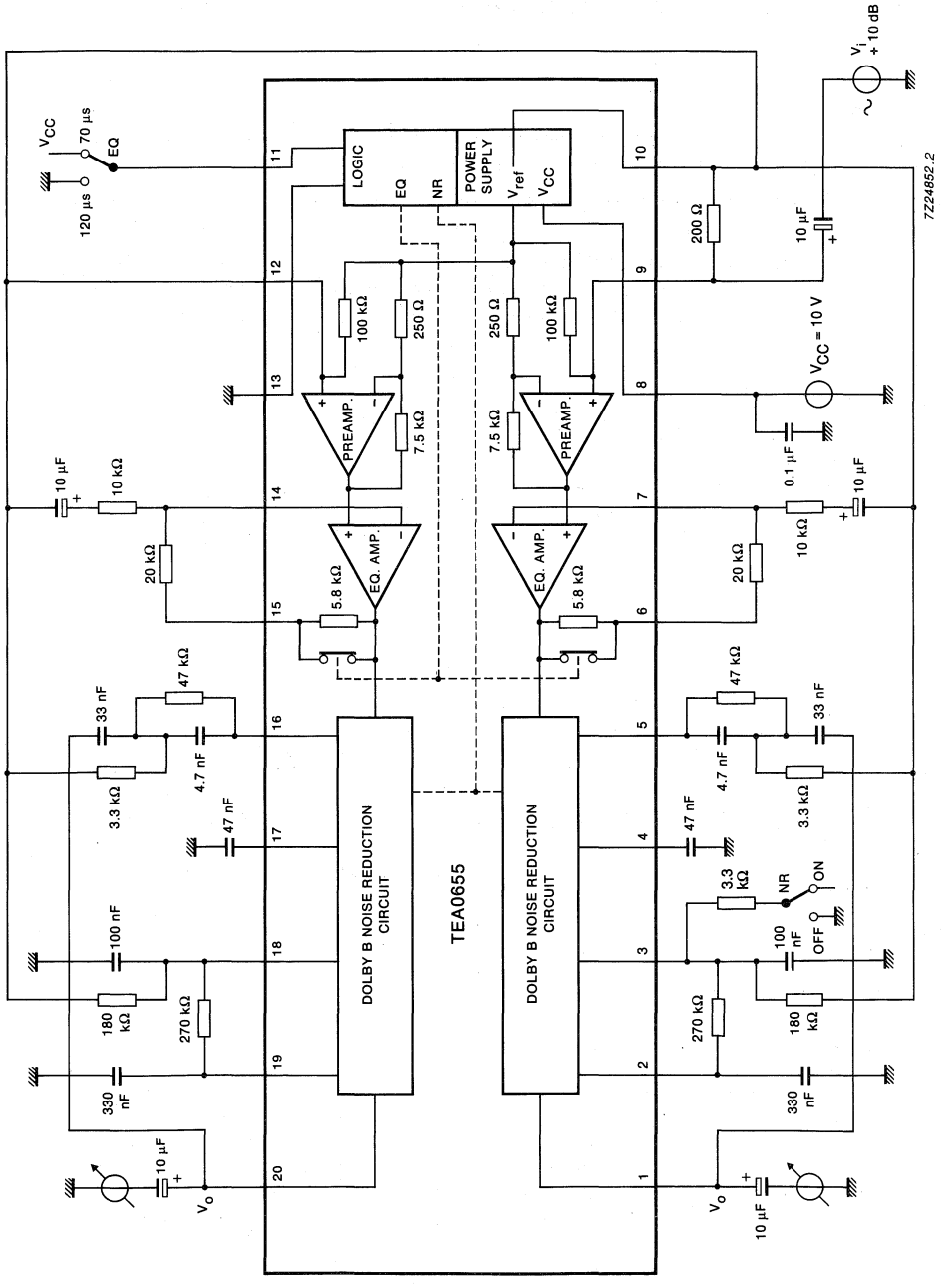


Fig.4 Test circuit for channel separation (α_{CS}).

DUAL DOLBY* B–TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0657 is a monolithic bipolar integrated circuit providing two channels of Dolby B-type noise reduction. The circuit contains all internal electronic switching to provide playback or record functions.

In addition the TEA0657 includes preamplifiers for the playback and record modes and multiplex filter buffers for both channels.

The device will operate with power supplies in the range of 9.0 V to 15.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF so it is advisable to use a regulated power supply or, a supply with a long time constant.

Features

- Dual noise reduction channels
- Full playback/record switching
- Separate playback/record inputs
- Multiplex filter buffers
- Simultaneous switching on both channels
- Dual or single supply operations
- Dolby reference level = 580 mV
- Input sensitivity = 30 mV

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{CC}	9.0	–	15.0	V
Supply current	I_{CC}	–	19	–	mA
Signal plus noise to noise ration					
record mode	(S+N)/N	–	72	–	dB
playback mode	(S+N)/N	–	90	–	dB

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
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PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

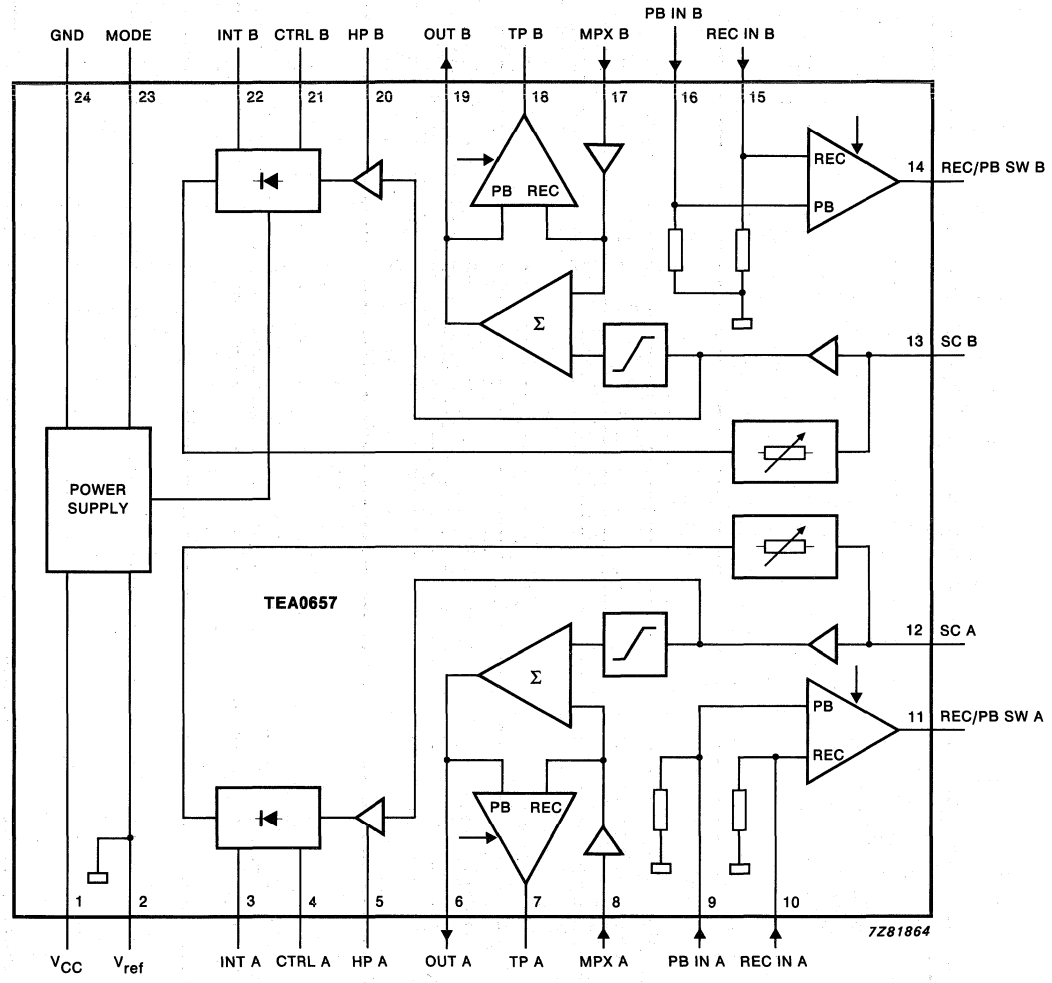


Fig. 1 Block diagram.

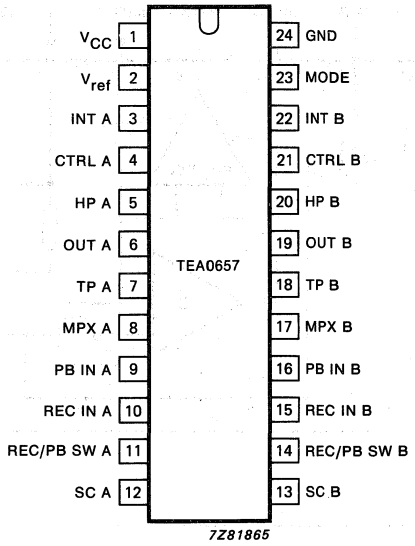


Fig. 2 Pinning diagram.

1	V_{CC}	supply voltage
2	V_{ref}	reference voltage
3	INT A	integrating filter channel A
4	CTRL A	control voltage channel A
5	HP A	high-pass filter channel A
6	OUT A	output channel A
7	TP A	test point channel A, line output channel A
8	MPX A	multiplex buffer channel A
9	PB IN A	playback input channel A
10	REC IN A	record input channel A
11	REC/PB SW A	record/playback switch channel A
12	SC A	side chain channel A
13	SC B	side chain channel B
14	REC/PB SW B	record/playback switch channel B
15	REC IN B	record input channel B
16	PB IN B	playback input channel B
17	MPX B	multiplex buffer input channel B
18	TP B	test point channel B, line output channel B
19	OUT B	output channel B
20	HP B	high-pass filter channel B
21	CTRL B	control voltage channel B
22	INT B	integrating filter channel B
23	MODE	record/playback select switch
24	GND	ground

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 22 is open-circuit and OFF when connected to pin 24 via a 5.1 kΩ resistor (see Fig. 3).
Pin 24 performs the functions of a logic input for noise reduction switching in both channels and provides smoothing for the control signal in one channel. It is important that no voltage is applied to this pin when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel.

Record/playback is achieved by applying a DC voltage to pin 23. The circuit will enable the appropriate input for the selected mode.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	–	16.0	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	–	+ 150	°C
Input voltage (pin 1)	V_I	−0,3	V_{CC}	V
Electrostatic handling (note 1)				

Note to the ratings

Note 1, Classification A:

Human body model; C = 100 pF; R = 1.5 kΩ; V ⩾ 2 kV.
Charge device model; C = 200 pF; R = 0 Ω; V ⩾ 500 V.

CHARACTERISTICS

V_{CC} = 12 V; f = 20 Hz to 20 kHz; T_{amb} = + 25 °C; all levels referenced to 580 mV RMS (0 dB) at TP (pin 7 or 18); test circuit Fig. 4; Record mode; NR ON; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	9	12	15	V
Supply current		I_{CC}	–	19	–	mA
Voltage gain (pins 9 or 10 to 11)	f = 1 kHz	G_v	–	20	–	dB
Voltage gain (pins 8 to 7)	f = 1 kHz	G_v	–	9	–	dB
Channel matching	NR OFF		−0.5	–	+ 0.5	dB
Distortion						
2nd and 3rd harmonic	f = 1 kHz, 0 dB	THD	–	0.08	0.15	%
	f = 10 kHz, + 10 dB	THD	–	0.15	0.3	%
Signal handling; (V_{CC} = 9 V)	1% distortion at 1 kHz		12	–	–	dB
Signal-to-noise plus noise ratio record mode	internal CCIR ARM weighted	(S+N)/N	–	72	–	dB
playback mode	R_S = 10 kHz	(S+N)/N	–	90	–	dB
Supply voltage ripple rejection	f = 1 kHz; 250 mV	SVRR	–	40	–	dB
Frequency response; (referenced to TP)	f = 1 kHz;					
	0 dB	Δf	−1.5	–	−1.5	dB
	−20 dB	Δf	−17.3	−15.8	−14.3	dB
	f = 5 kHz					
	−30 dB	Δf	−23.3	−21.8	−20.3	dB
	−40 dB	Δf	−30.2	−29.7	−28.2	dB
	f = 10 kHz					
	0 dB	Δf	−1.1	0.4	1.9	dB
	−30 dB	Δf	−25.0	−23.5	−22.5	dB
Input resistance; (pins 9, 10, 15 and 16)		R_I	–	50	–	kΩ
Channel separation	0 dB at TP; f = 1 kHz	α_{cr}	–	65	–	dB
Back-to-back frequency response shift;						
as a function of T_{amb}	0 to −70 °C		–	± 0.5	–	dB
as a function of V_{CC}	9 V to 15 V		–	± 0.5	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
PB/REC separation	30 mV; 1 kHz; at playback input, measure V_{OUT}	$\alpha_{PB/REC}$	–	72	–	dB
Minimum load resistance on output; (pins 6 and 9)	12 dB; 1 kHz; 1% THD	R_{Lmin}	10	–	–	kΩ
Switching thresholds						
playback; pin 23	V_{PB}	V_{PB}	0.7 V_{CC}	V_{CC}	–	V
record; pin 28		V_{REC}	–	GND	0.4 V_{CC}	V
NR OFF; pin 22		V_{OFF}	–	–	0.2 V_{CC}	V

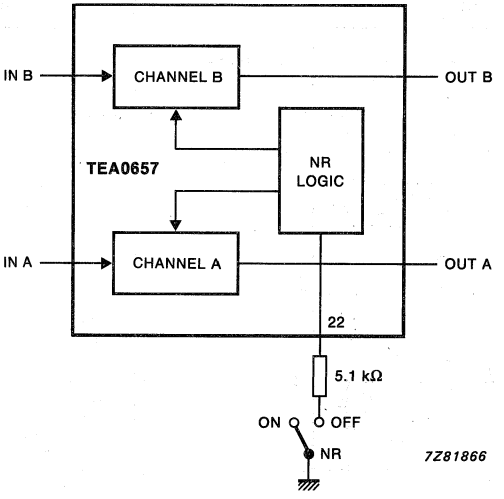
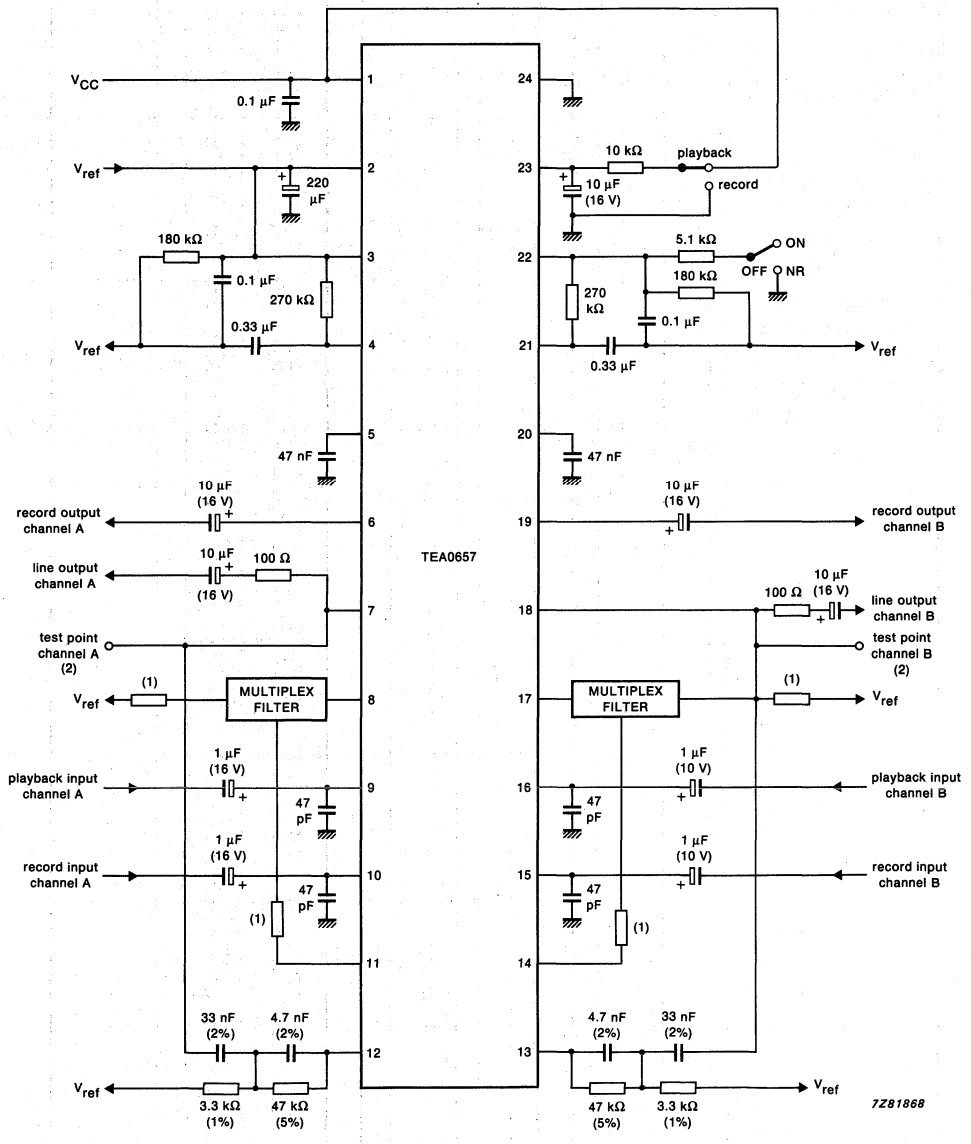


Fig. 3 External NR switch circuit for TEA0657.



All values within ± 10% unless otherwise specified.

Notes:

(1) Value determined by multiplexer in use.
(2) Dolby level = 580 mV at test points.

Fig. 4 Test and application circuit.

DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT117).
TEA0665T: 28-lead mini-pack; plastic (SO28; SOT136A).

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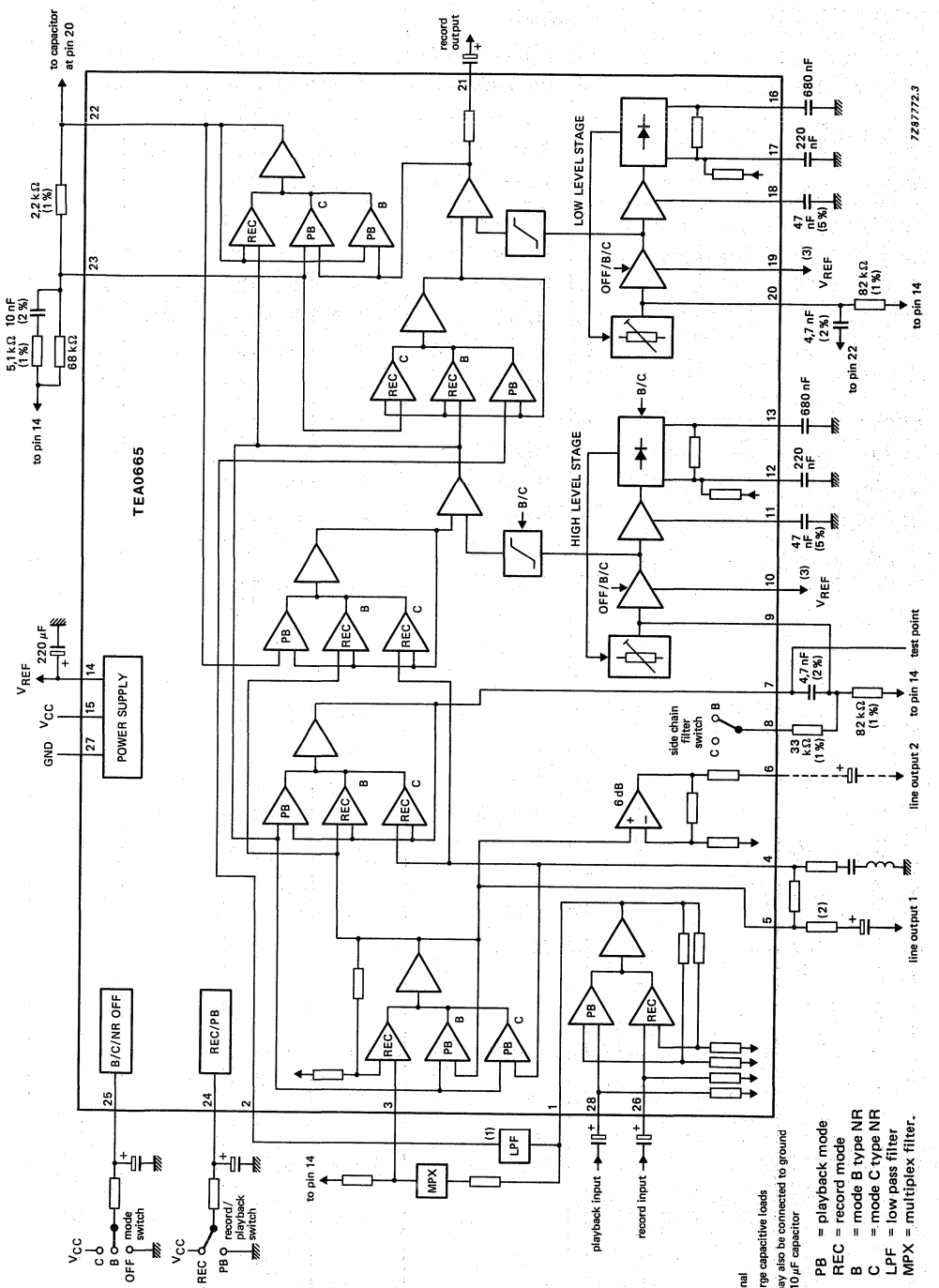


Fig. 1 Block diagram and application circuit.

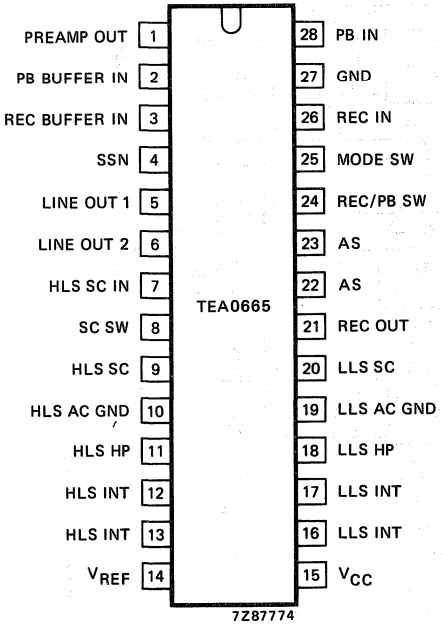


Fig. 2 Pinning diagram.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	playback amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLS SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max. 18	V
Input voltage (pins 26 and 28)	V_I	max. −0,3 to V_{CC}	V
Total power dissipation	P_{tot}	600	mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(± 4)	(± 7)	(± 8)	V
Supply current	OFF	–	no input signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig. 8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		−0,5	0	+ 0,5	dB
Line output 2; amplifier gain V_o/V_i (pin 6 to pin 5)				G_v	+ 5,5	+ 6	+ 6,5	dB
Total harmonic distortion	OFF	1	TPL = 0 dB*	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic distortion	C	1	TPL = 0 dB	THD	–	0,15	0,3	%
			TPL = + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-to-noise ratio	C		R_S = 10 kΩ CCIR/ARM weighted	(S+N)/N	62	66	–	dB

* TPL is Test Point Level.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Frequency response	B	2	TPL = −25 dB		−19,0	−18,0	−17,0	dB
		5	TPL = −40 dB		−30,7	−29,7	−28,7	dB
		10	TPL = −30 dB		−24,5	−23,5	−22,5	dB
	C	0,2	TPL = −40 dB		−33,4	−31,9	−30,4	dB
		1	TPL = −30 dB		−20,1	−18,6	−17,1	dB
		1	TPL = −20 dB		−16,1	−14,1	−12,1	dB
		5	TPL = −0 dB		−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB		−19,1	−17,1	−15,1	dB
		5	TPL = −40 dB		−28,5	−26,5	−24,5	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		$V_{25-27} = 0$ V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, range 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

   The voltage drop across the external time constant resistor must be taken in to account.

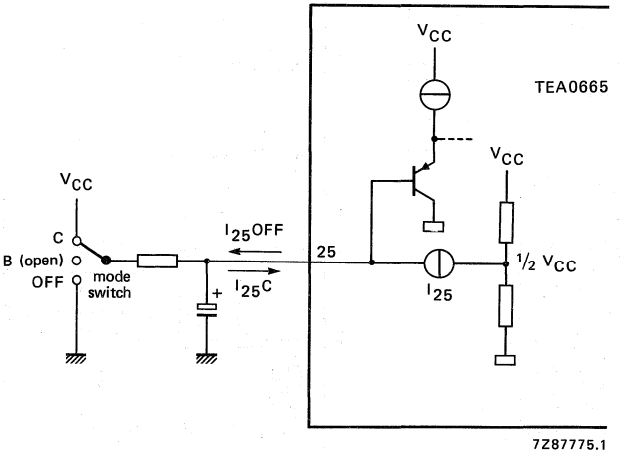


Fig. 3 Mode switch input configuration.

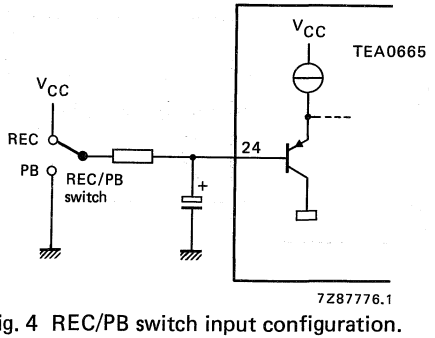
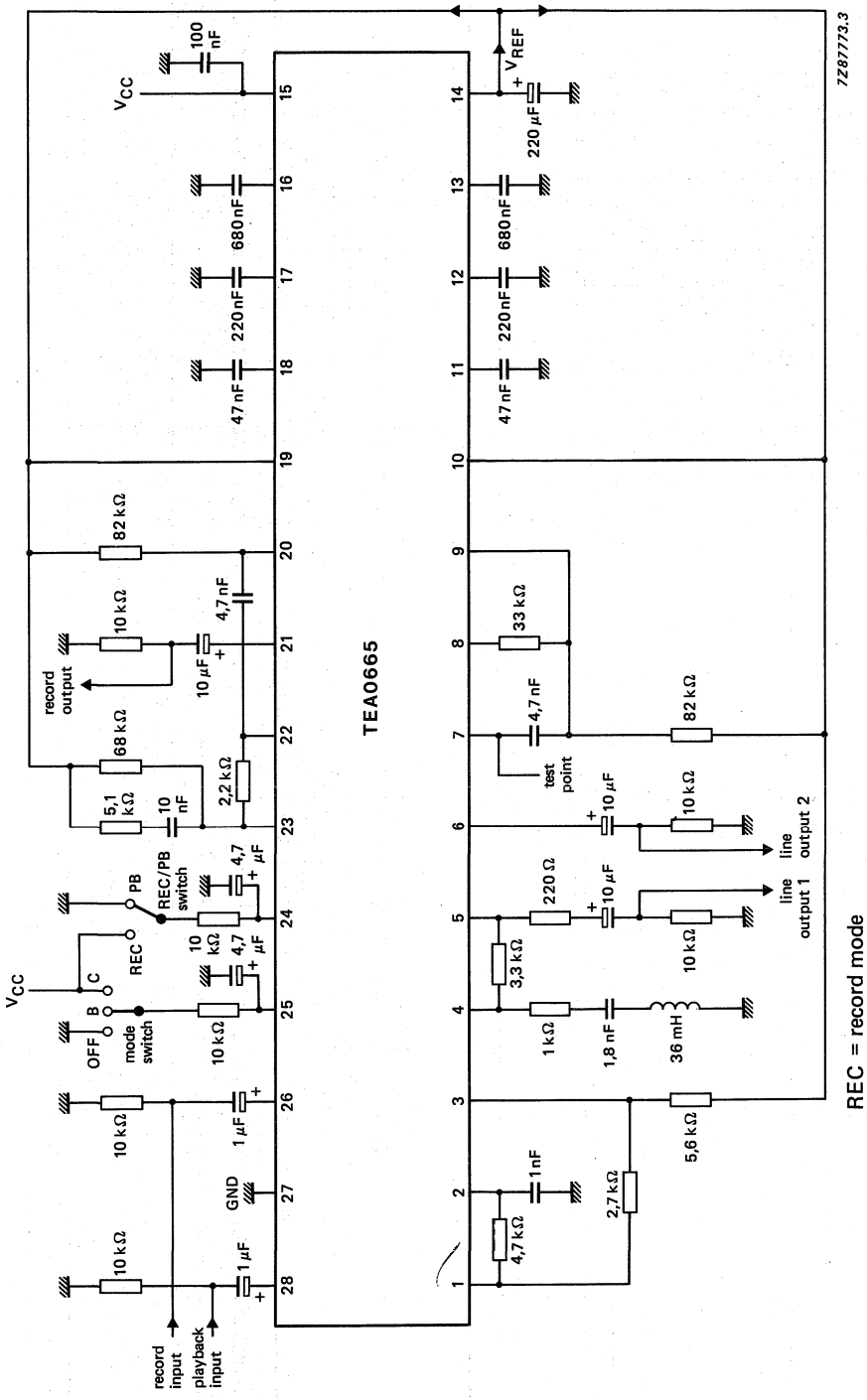


Fig. 4 REC/PB switch input configuration.



REC = record mode
PB = playback mode

Tolerances: resistors 1%
capacitors 1%

Fig. 5 Test circuit.

SYSTEM GRAPHS

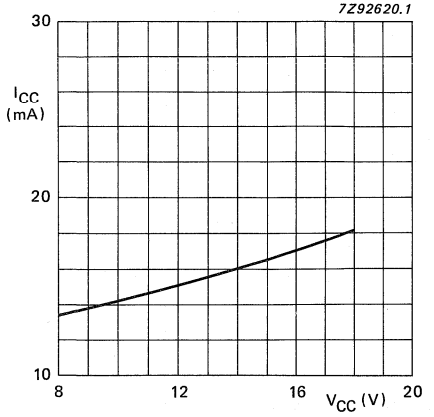


Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

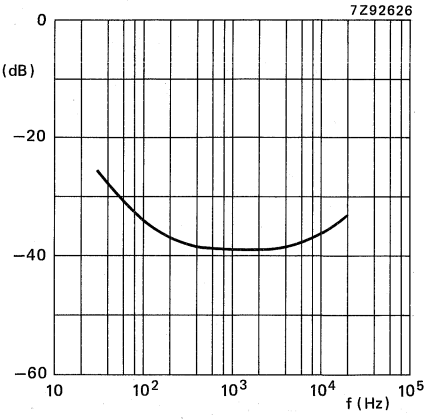


Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

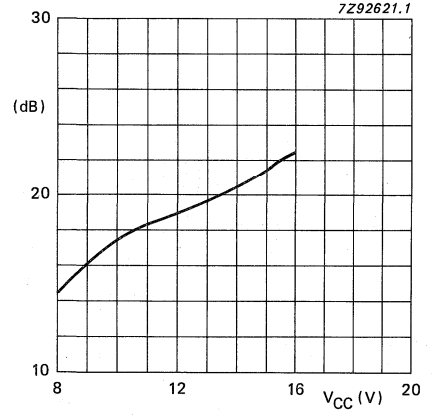


Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

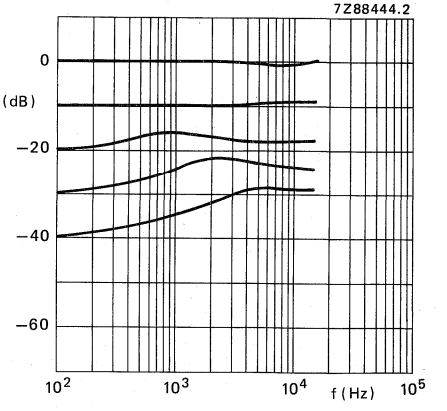


Fig. 9 Encoder frequency response for B-mode.

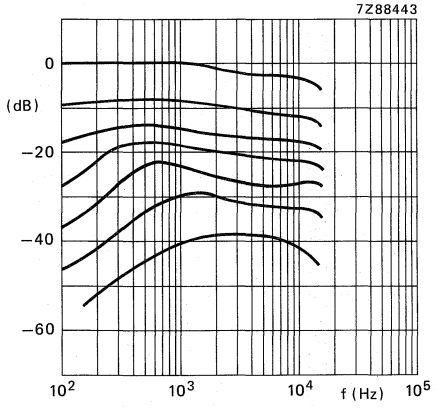


Fig. 10 Encoder frequency response for C-mode.

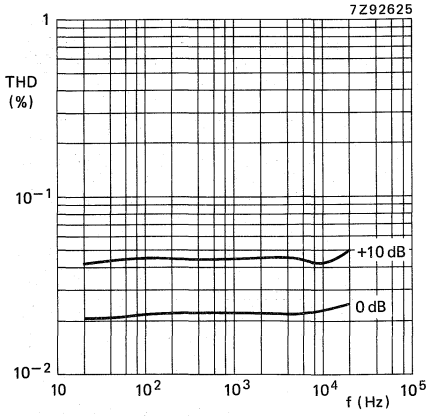


Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

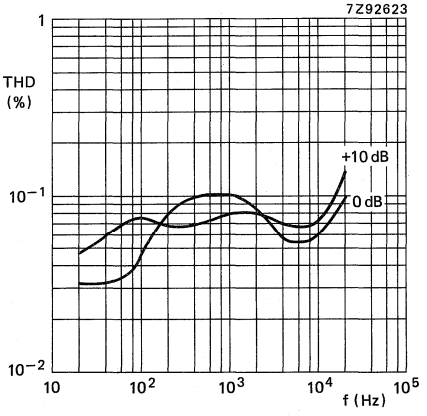


Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

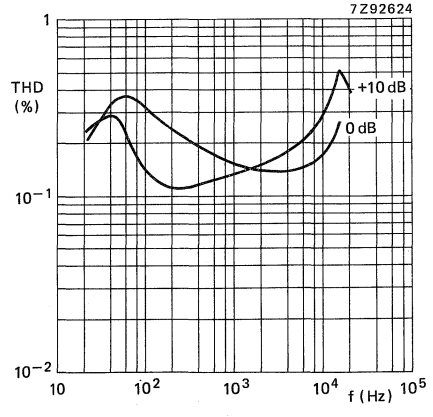


Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

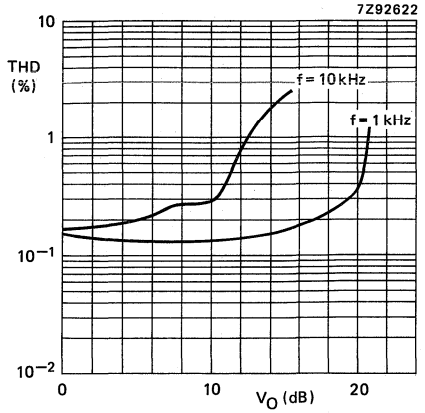


Fig. 14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

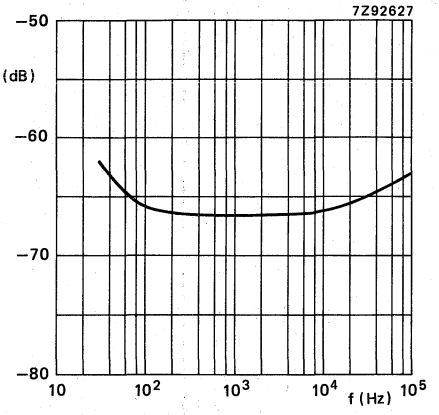


Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

1-CHIP AM RADIO

GENERAL DESCRIPTION

The TEA5551T is a 1-chip monolithic integrated radio circuit which is designed for use as a pocket receiver with headphones in a supply voltage range (V_S) of 1.8 V to 4.5 V.
The circuit consists of a complete AM part and dual AF amplifier with low quiescent current. The AF part has low radiation (HF noise) and good overdrive performance. The dual AF amplifier makes the device suitable for operation in an AM/FM stereo receiver with or without stereo cassette player.
The IC has a 1-pin switch for AM or other applications.

Features

- Low voltage operation (V_S = 1.8 V to 4.5 V)
- Low current consumption (I_{tot} = 5 mA at V_S = 3 V)
- All pins provided with ESD protection

AM part

- High sensitivity (V_i = 1.5 μV for V_o = 10 mV)
- Good IF suppression
- Good signal handling ($V_{i(max)}$ = 80 mV)
- Switch for AM or other applications
- Short waveband (> 40 MHz)

AF part

- A fixed integrated gain of 32 dB
- Few external components required
- Very low quiescent current
- Low HF radiation and good AF overdrive performance
- 0 to 20 kHz limited frequency response
- 25 mW per channel output power in 32 Ω

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	1.8	3.0	4.5	V
Supply current		$I_5 + I_{10}$	–	6	–	mA
AM part	m = 0.3					
RF sensitivity						
RF input voltage						
	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
	S/N = 26 dB	$V_{i(RF)}$	–	15	–	μV
	S/N = 50 dB	$V_{i(RF)}$	–	10	–	mV
AF output voltage	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
Total harmonic distortion	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
Signal handling capability	m = 0.8; THD = 10%	$V_{i(RF)}$	–	80	–	mV
AF part	both channels driven					
Output power	R_L = 32 Ω; THD = 10%					
at V_S = 3.0 V		P_o	–	25	–	mW
at V_S = 4.5 V		P_o	–	60	–	mW
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Channel separation	1 kHz	α	–	50	–	dB

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

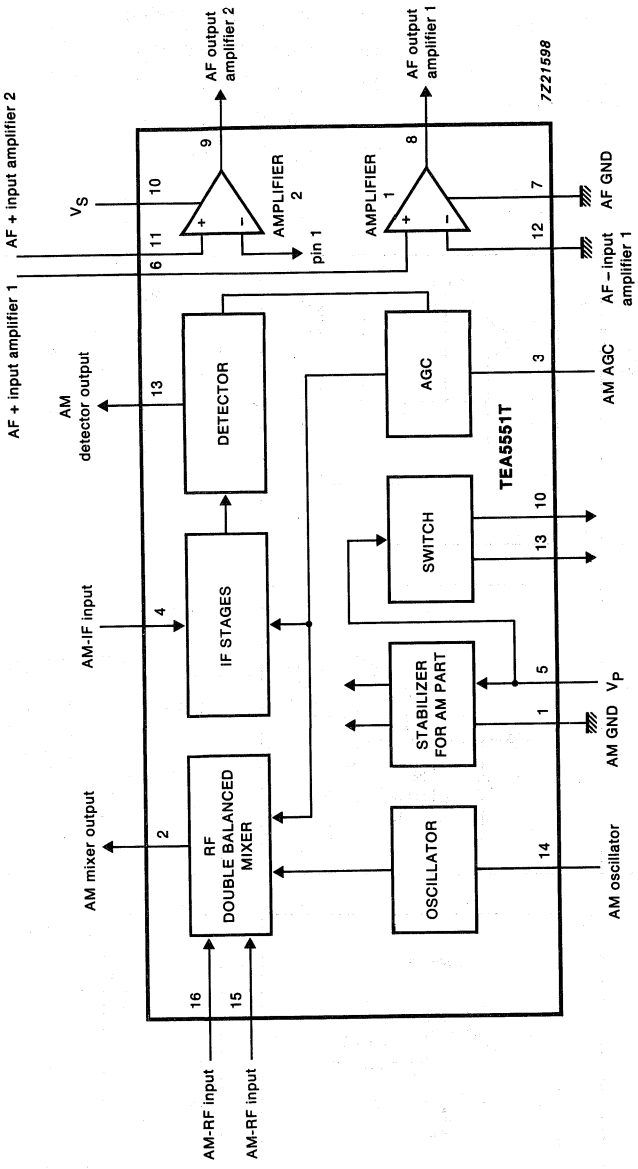


Fig. 1 Block diagram.

PINNING

1	AM GND	9	AF output amplifier 2
2	AM mixer output	10	AF supply voltage (V_S)
3	AM AGC	11	AF + input amplifier 2
4	AM–IF input	12	AF – input amplifier 1
5	AM supply voltage (V_P)	13	AM detector output
6	AF + input amplifier 1	14	AM oscillator
7	AF GND	15	AM–RF input
8	AF output amplifier 1	16	AM–RF input

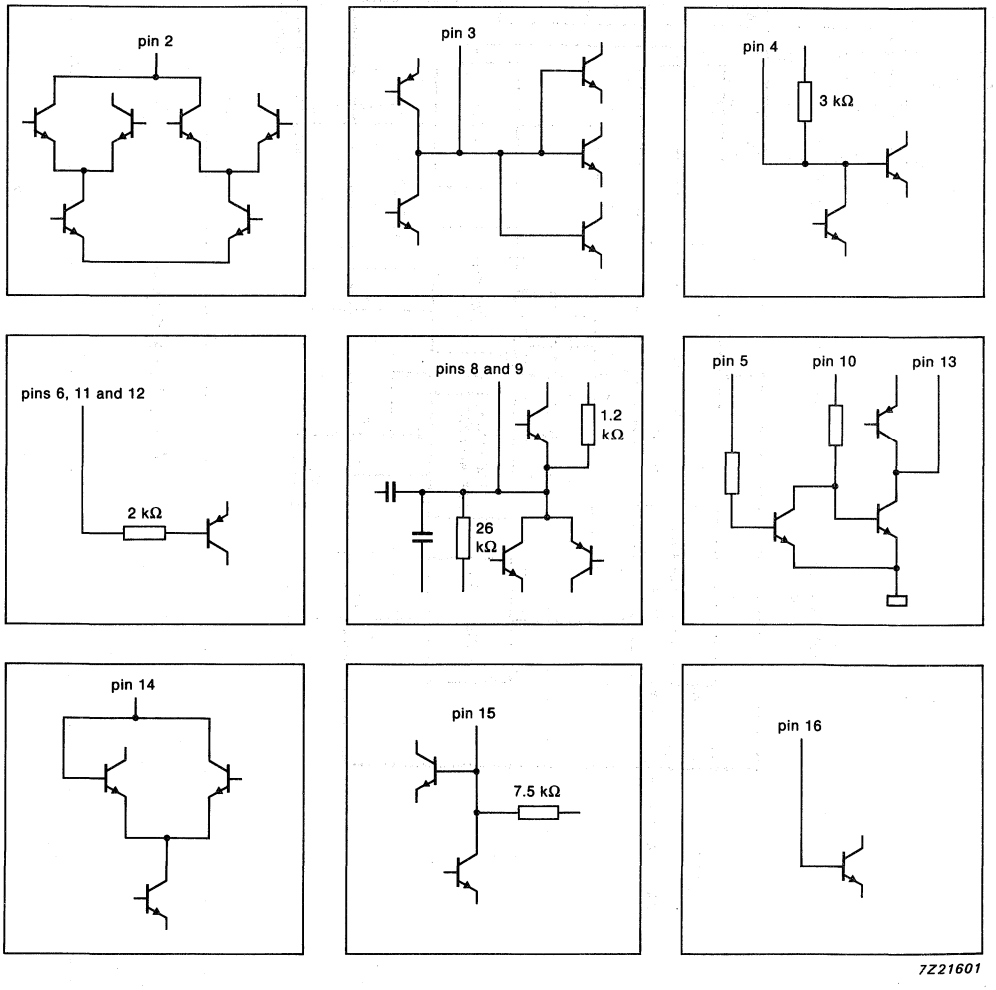


Fig. 2 All pins provided with ESD protection diodes to substrate.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_S	–	6	V
Supply current (peak)		I_M	–	150	mA
Crystal temperature		T_c	–	150	°C
Short-circuit protection	V_S = 4.5 V	t_{sc}	–	5	s
Total power dissipation		P_{tot}	see Fig. 3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+60	°C

QUALITY

In accordance with UZW-BO/FQ-0601.
Operating life endurance verified 2000 hours at T_j = 85 °C.
The product meets the 600 V ESD on all pins (HBM specification UZW-BO/FQ-A302).

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 110 K/W

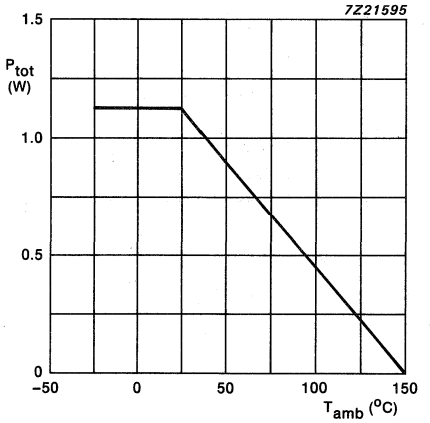


Fig. 3 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 1 and pin 7; all input currents are positive; all parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	1.8	3.0	4.5	V
Voltages					
pin 5	V_5	1.6	2.8	4.3	V
pin 10	V_{10}	1.8	3.0	4.5	V
HF part					
Total current consumption (pin 5)	I_5	–	2.2	–	mA
Oscillator current (pin 14)	I_{14}	–	100	–	μA
Mixer current (pin 2)	I_2	–	200	–	μA
Voltages					
pin 3	V_3	–	150	–	mV
pin 13	V_{13}	–	600	–	mV
pin 15	V_{15}	–	1.1	–	V
pin 16	V_{16}	–	1.1	–	V
AF part					
Total current consumption (pin 10)	I_5	–	4.0	–	mA
Input bias current (pin 11 connected to pin 16)	$I_{11} + I_{16}$	–	40	–	nA
DC output voltage					
pin 8	V_8	–	1.5	–	V
pin 9	V_9	–	1.5	–	V

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input voltage	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
Loss in sensitivity	$V_{o(AF)}$ = 10 mV; V_S = 1.8 V	$\Delta V_{i(RF)}$	–	6	–	dB
Noise						
Signal-to-noise ratio for RF input signal voltage of						
$V_{i(RF)}$ = 2 μV		S/N	–	6	–	dB
$V_{i(RF)}$ = 15 μV		S/N	–	26	–	dB
$V_{i(RF)}$ = 1 mV		S/N	–	46	–	dB
AF output voltage						
	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
	$V_{i(RF)}$ = 1 mV; V_S = 1.8 V	$V_{o(AF)}$	–	55	–	mV
Total harmonic distortion						
	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
	$V_{i(RF)}$ = 80 mV; m = 0.8	THD	–	10	–	%
AGC range						
Change in RF input voltage for 10 dB change in AF output voltage	$V_{i(RF1)}$ = 50 mV	$V_{i(RF1)}/V_{i(RF2)}$	–	86	–	dB
Optimum source impedance		Z_{source}	–	3	–	kΩ
IF suppression						
at $V_{o(AF)}$ = 10 mV	note 1	α	–	20	–	dB
Oscillator (pin 14)	f_{osc} = 1468 kHz					
Oscillator voltage		V_i	–	100	–	mV
	V_5 = 1.5 V	V_i	–	*	–	mV

Note to the AC characteristics

1. $\alpha = \dfrac{V_i \text{ at } f_i = 468 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

AF conditions: f = 1 kHz; R_L = 32 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power						
	THD = 10%	P_o	–	25	–	mW
	THD = 10%; V_S = 1.8 V	P_o	–	8	–	mW
	THD = 10%; V_S = 4.5 V	P_o	–	60	–	mW
Total harmonic distortion	P_o = 10 mW	THD	–	0.5	–	%
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Noise						
Noise output voltage	R_S = 5 kΩ; B = 15 kHz	V_{no}	–	240	–	μV
HF noise output voltage	R_S = 5 kΩ; B = 5 kHz; f = 500 kHz	$V_{no(RF)}$	–	20	–	μV
Input circuit						
Input impedance	pin 11 connected to pin 12	Z_i	–	3	–	MΩ
Mute switch						
AC impedance (pin 13 to ground)	V_5 = 0 V; I_{13} = 0.32 mA	R_S	–	200	–	Ω

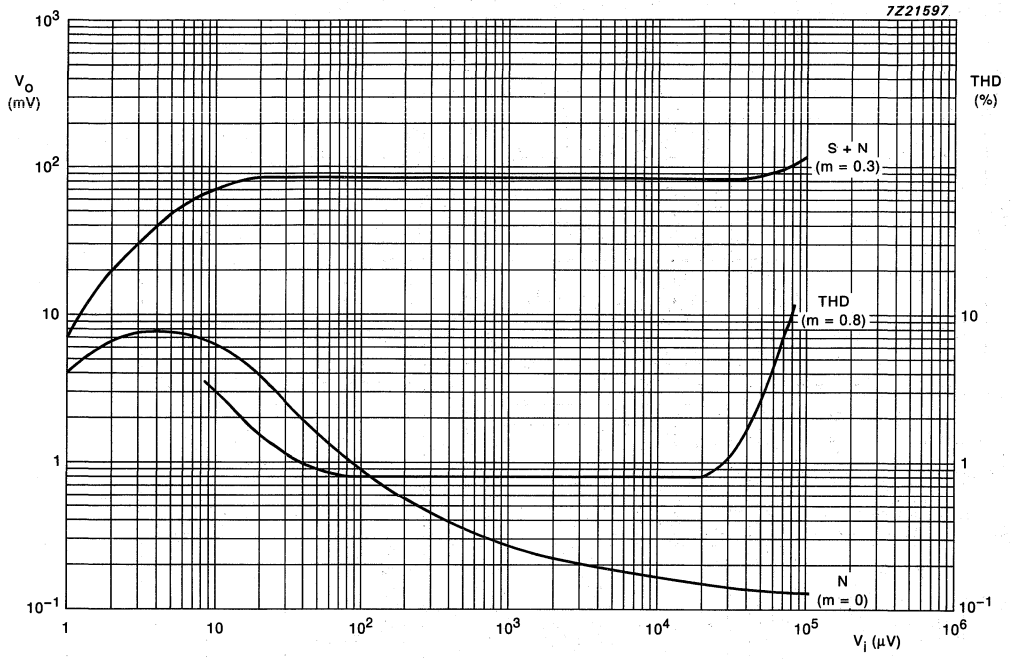


Fig. 4 Typical signal (S) and noise (N) output voltages, where V_o is the AF output voltage at pin 13, as a function of the input voltage V_i. V_i is the input voltage at pin 16. Also shown is the total harmonic distortion (THD).
Conditions: f_o = 1 MHz; f_m = 1 kHz; V_S = 3 V; R_g = 50 Ω; m = 0.3 (unless otherwise specified).

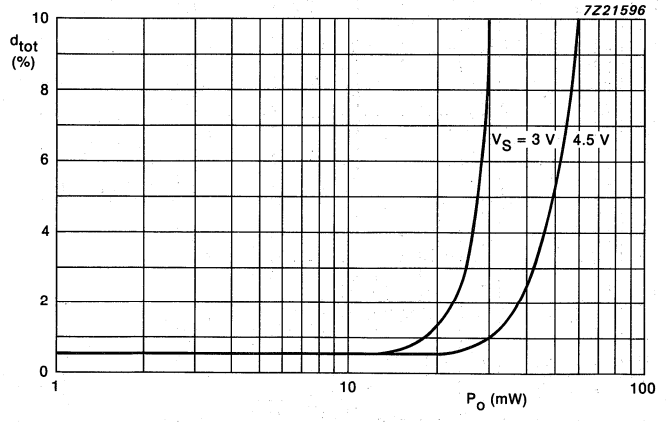
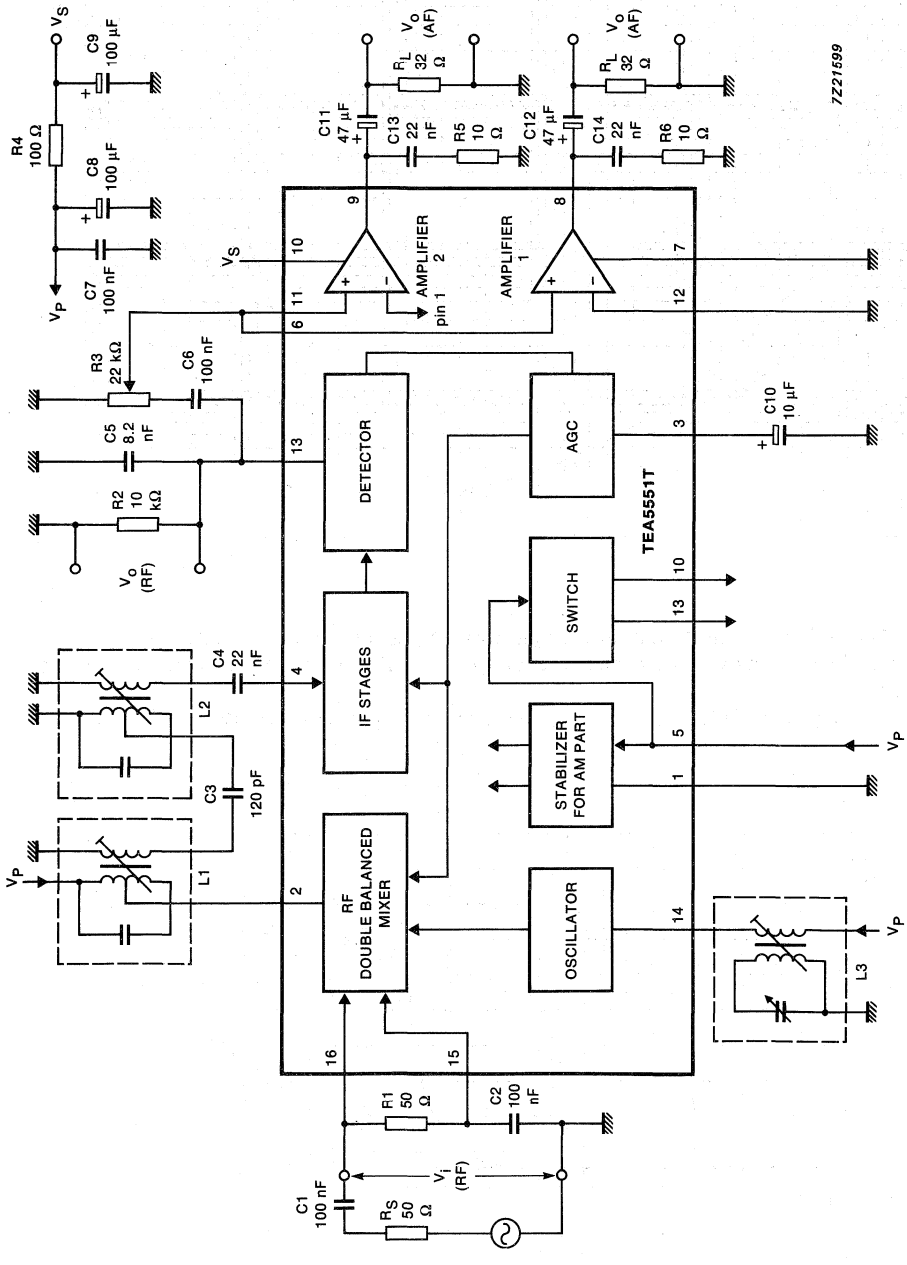


Fig. 5 Total distortion (d_{tot}) as a function of output power (P_o).
Conditions: V_S = 3 V and 4.5 V; R_L = 32 Ω; f = 1 kHz.



Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

Fig. 6 Test circuit.

APPLICATION INFORMATION

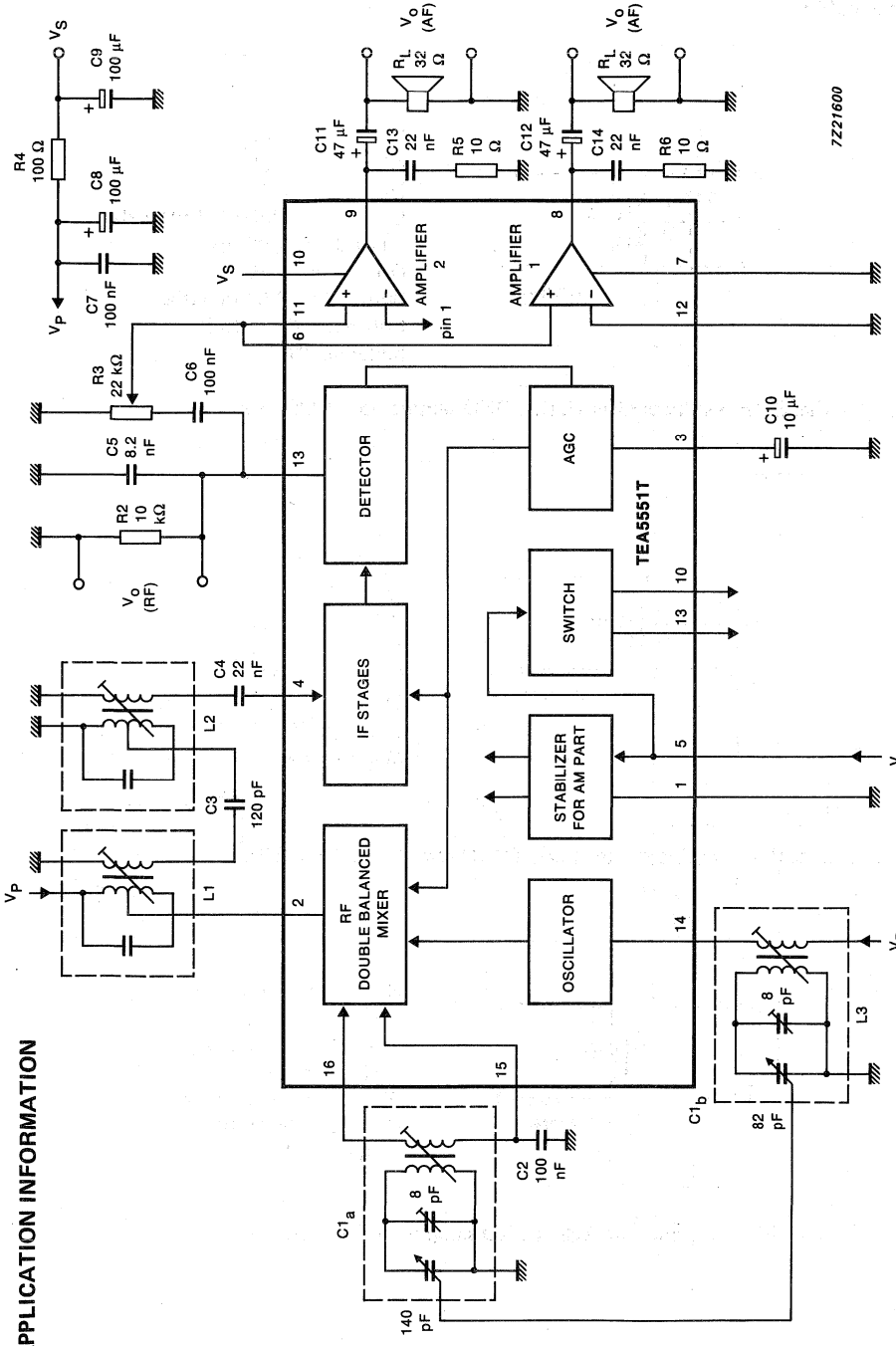
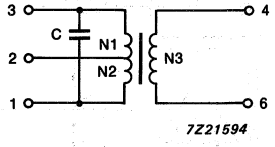


Fig. 7 Application circuit.

Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

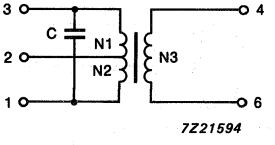
COIL DATA

AM coils (Figs 6 and 7)



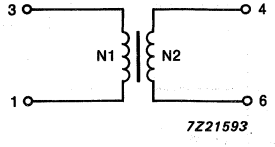
N1 = 60
N2 = 80
N3 = 15
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 8 IF bandpass filter (L1). TOKO sample no. 7MCS2199.



N1 = 125
N2 = 15
N3 = 6
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 9 IF bandpass filter (L2). TOKO sample no. 7MCS2197.



N1 = 90
N2 = 6
L1–L3 = 295 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7BR

Fig. 10 Oscillator coil (L3). TOKO sample no. 7BRS10869X.

RF/IF CIRCUIT FOR AM/FM RADIO

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	I_7	typ.	6,2 mA
AM performance (pin 2) for m = 0,3			
Sensitivity			
at V_o = 10 mV	V_i	typ.	1,7 μV
at S/N = 26 dB	V_i	typ.	16 μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5 %
FM performance (pin 1) for Δf = ± 22,5 kHz			
limiting sensitivity, −3 dB	V_i	typ.	110 μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65 dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3 %
AM suppression at V_i = 10 mV	AMS	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

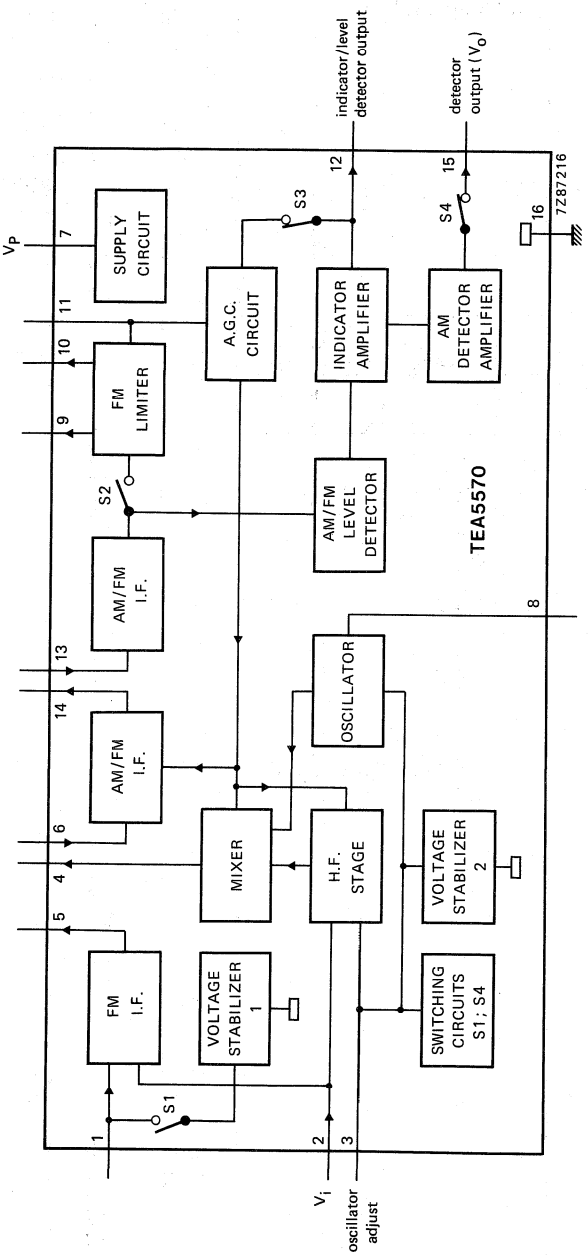


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	V_{n-16}	max.	12 V
Voltage range at pin 8	V_{8-16}		$V_P \pm 0{,}5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}		−55 to +150 °C
Operating ambient temperature range	T_{amb}		−30 to +85 °C

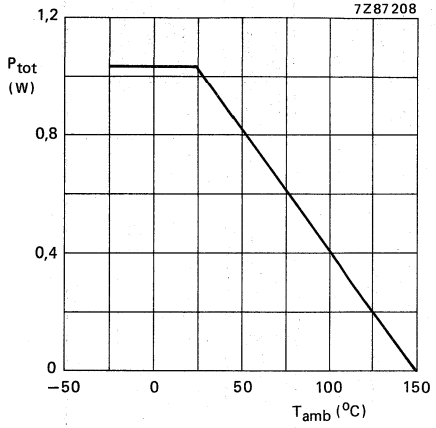


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7-16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	V_{1-16}	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	V_{1-16}	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3-16}$	–	1,42	–	V
at pin 6	V_{6-16}	–	0,7	–	V
at pin 11	V_{11-16}	–	1,4	–	V
at pin 13	V_{13-16}	–	0,7	–	V
at pin 14	V_{14-16}	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	–	1,3		μV
at S + N/N = 26 dB	V_i	–	16	20	μV
at S + N/N = 50 dB	V_i	–	1	–	mV
Signal handling (THD ⩽ 10% at m = 0,8)	V_i	200	–	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	–	0,5	–	%
at V_i = 2 mV (m = 0,8)	THD	–	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	–	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	–	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	–	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at –3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	–	6	–	μV
at S + N/N = 65 dB	V_i	–	1	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	–	0,3	–	%
AM suppression (note 5)	AMS	–	50	–	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	–	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	–	0,25	–	V
at V_i = 2 mV	$V_{12\text{-}16}$	–	1,0	–	V
AM to FM switch					
Switching current at $V_{3\text{-}16} < 1$ V	$-I_3$	–	–	400	μA

Notes to characteristics

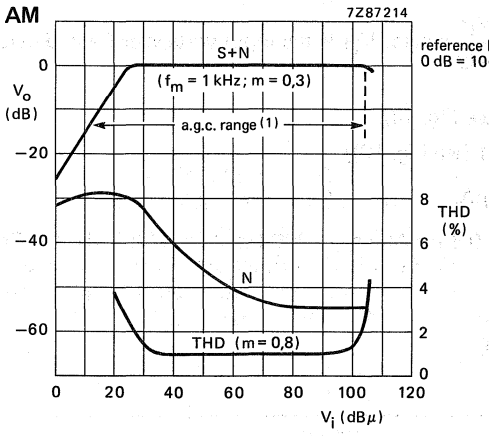
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
   $I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

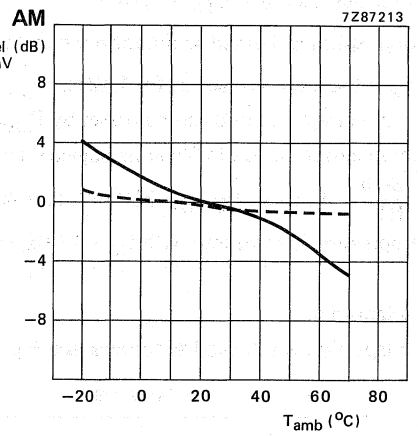
Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

Typical graphs



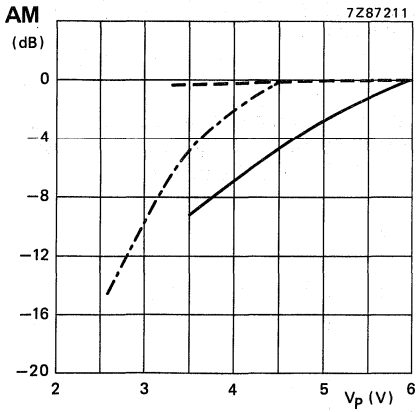
(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.
– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.
—·—·— sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

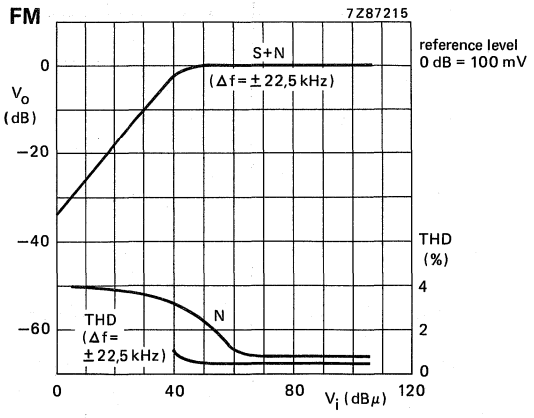
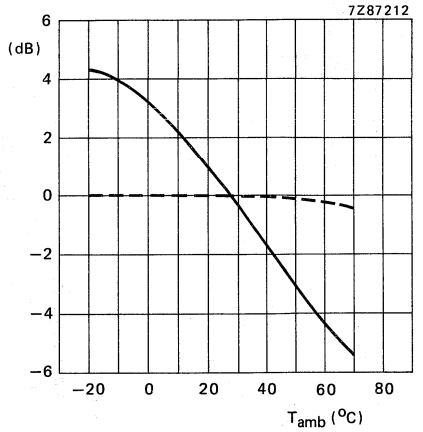


Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

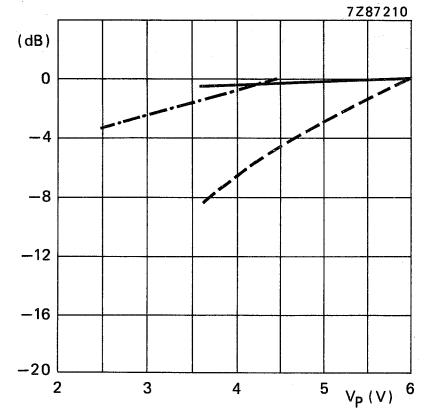
FM



——— sensitivity at −3 dB limiting.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22$ kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

FM



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.
—·—·— sensitivity at −3 dB limiting: V_P = 4,5 V application.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22{,}5$ kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

AM/FM

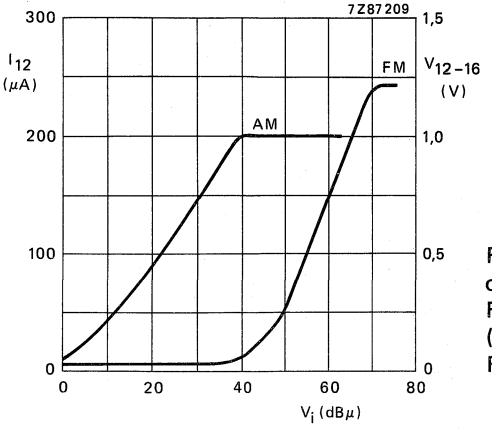


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

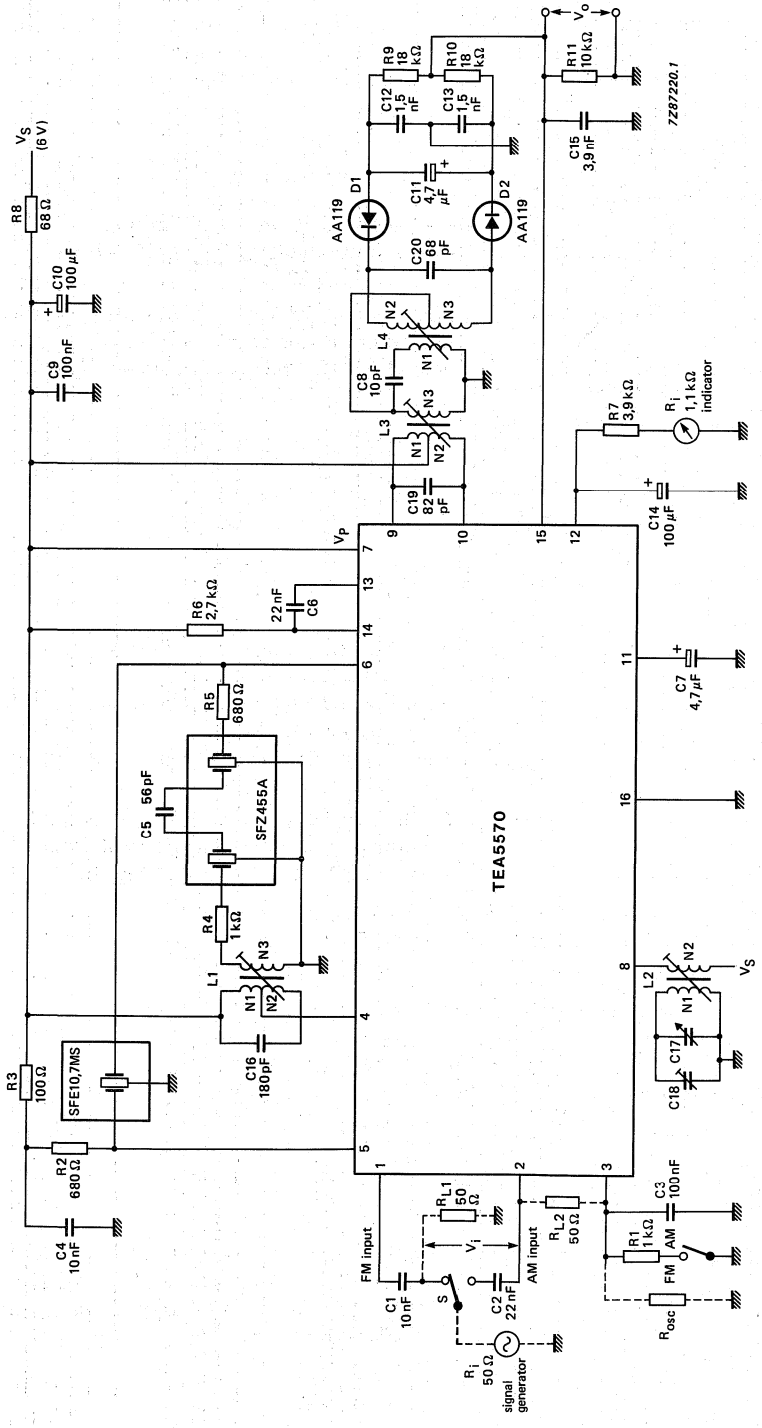


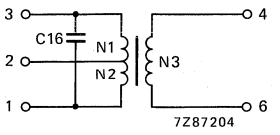
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 = 2{,}7$ kΩ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275$ Ω (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

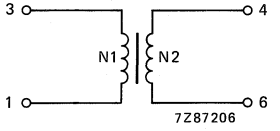
COIL DATA

AM i.f. coils (Fig. 10)



N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

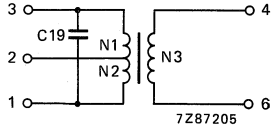
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.



N1 = 90
N2 = 7
Wire = 0,07 mm dia.

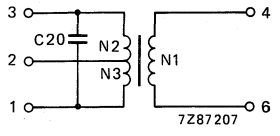
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)



N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

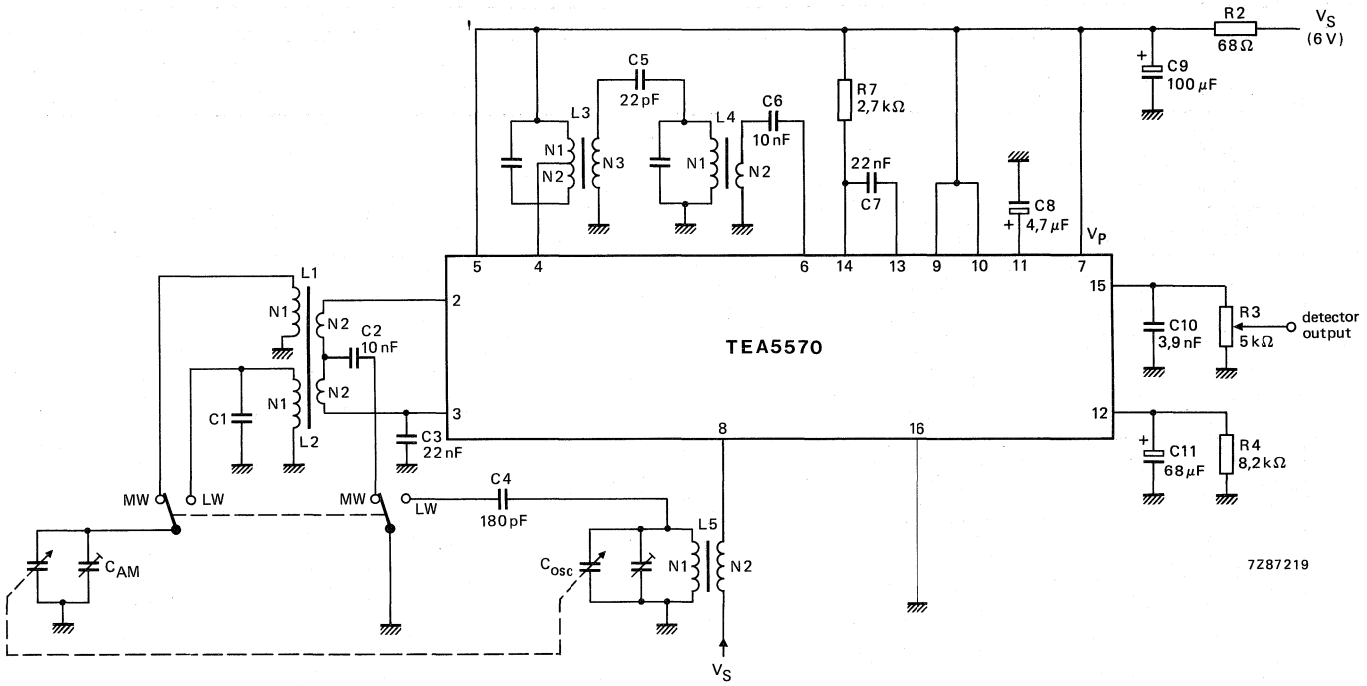


N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



Coil data

L3	N1 = 73	L4	N1 = 146	L5	N1 = 90
	N2 = 73		N2 = 9		N2 = 6
	N3 = 9		C = 180 pF		
	C = 180 pF				

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

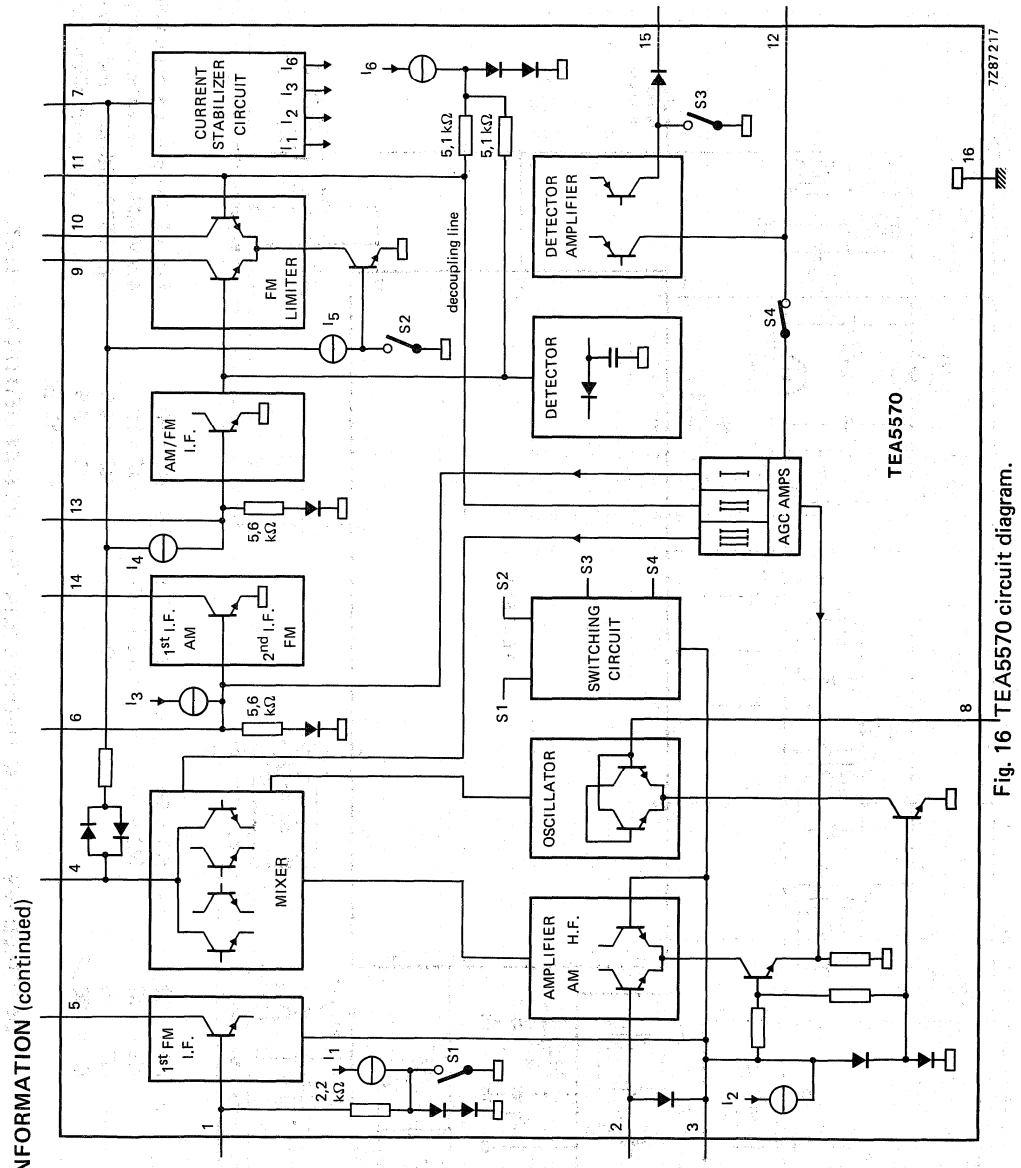


Fig. 16 TEA5570 circuit diagram.

APPLICATION INFORMATION (continued)

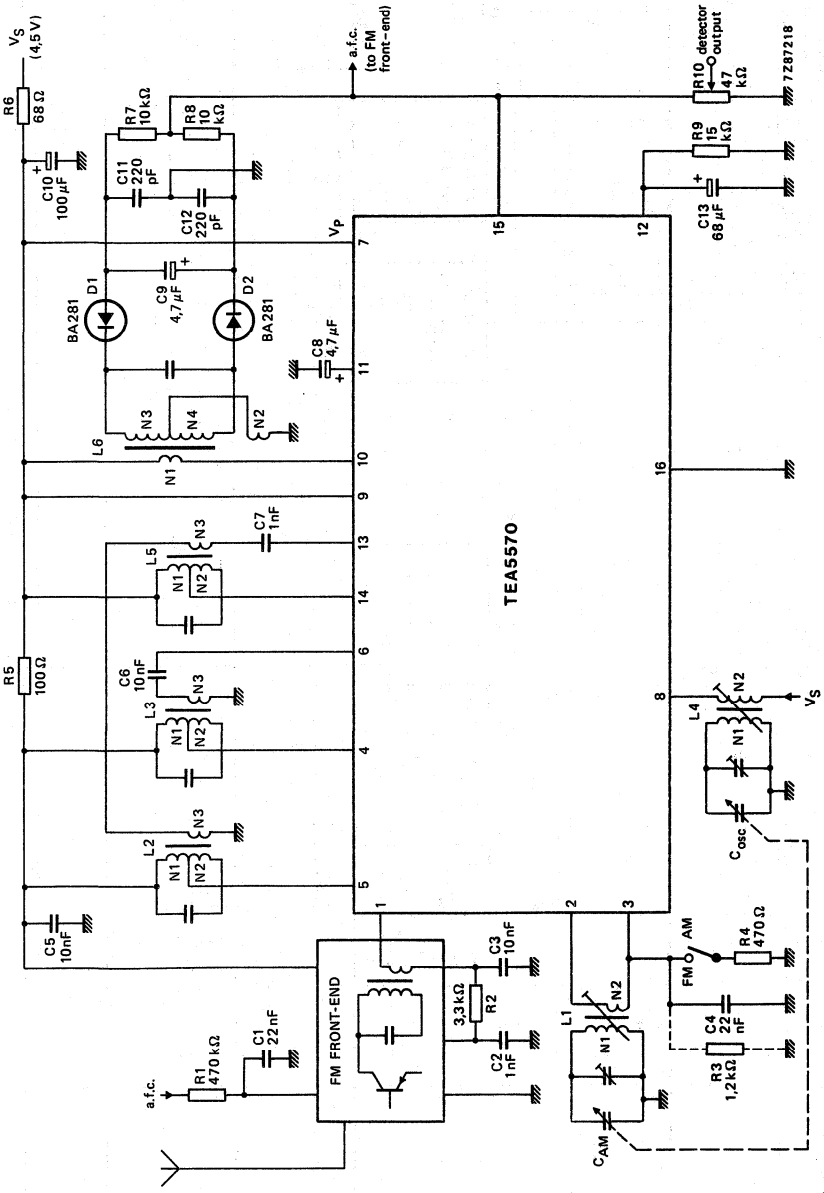


Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.

Coil data

L2	N1 = 3	L3	N1 = 33	L4	N1 = 90	L5	N1 = 33
	N2 = 8		N2 = 113		N2 = 6		N2 = 113
	N3 = 1		N3 = 9				N3 = 9
	C = 82 pF		C = 180 pF				

L6	N1 = 50
	N2 = 50
	N3 = 4,5
	N4 = 6,5
	C = 82 pF

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5580 PLL stereo decoder is for car, portable and mains-fed medium-fi radios and radio recorders. It features a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 50 dB, or up to 60 dB with adjustment of the pilot-cancelling resistor (R3, Figs 3 and 4). Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 3,6 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:
  - third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;
  - phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz pilot tone
- IF filter roll-off compensation

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

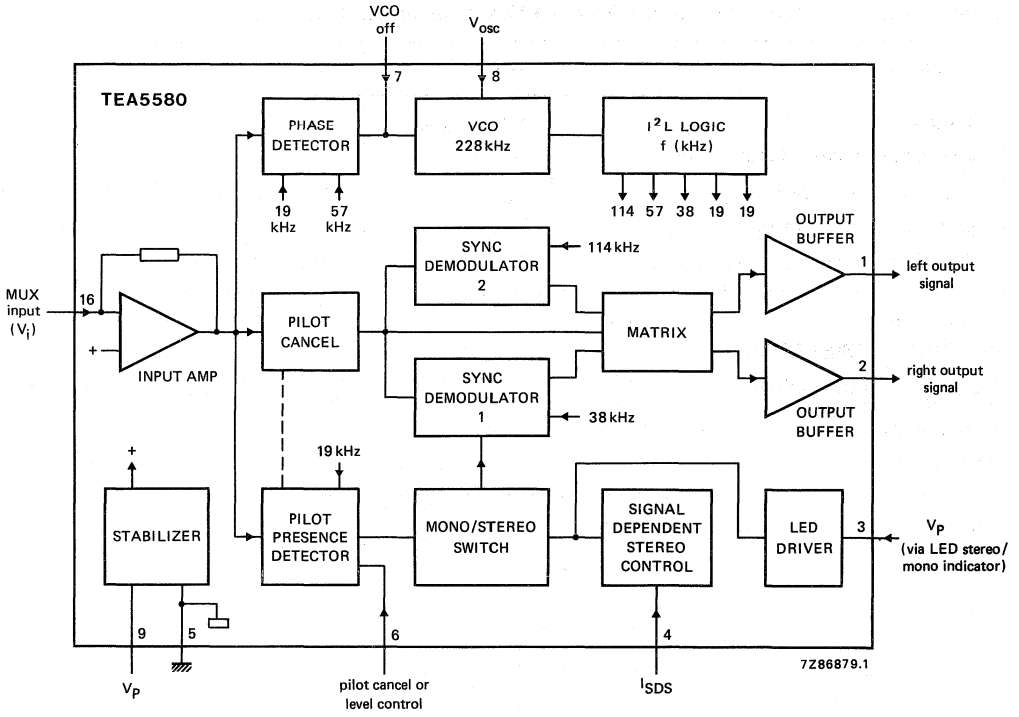


Fig. 1 Block diagram.

Note

Do **not** connect pins 10, 11, 12, 13, 14 or 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pins 3 and 9)	V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)	$-I_{3M}$	–	75	mA
Total power dissipation	P_{tot}	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 75 K/W

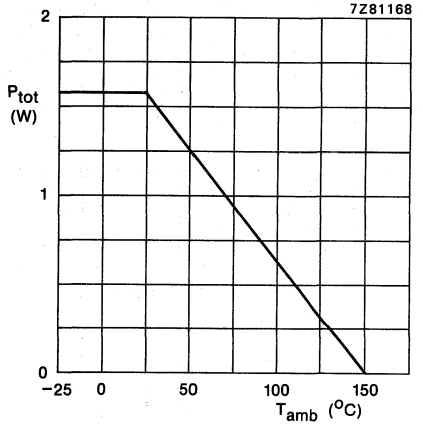


Fig. 2 Power derating curve.

CHARACTERISTICS

Measured in the circuit of Fig. 3; V_P = 7,5 V; T_{amb} = 25 °C; all d.c. voltages are with respect to pin 5; all currents are positive into the IC; a.c. measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV; f_m = 1 kHz; de-emphasizing time = 50 μs; oscillator adjusted to I_{osc} at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R1 and C1 in Fig. 3); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
D.C. Characteristics					
Supply voltage (note 1)	V_P	3,6	7,5	16	V
Total current consumption at V_P = 7,5 V (note 2)	I_P	–	10	13,5	mA
Dissipation at V_P = 7,5 V (note 2)	P_{tot}	–	75	–	mW
Bias voltage (pin 16)	V_{16-5}	–	1,4	–	V
Input current (pin 4)	I_4	–	–	400	μA
D.C. output current (pin 1)	$-I_1$	195	275	390	μA
D.C. output current (pin 2)	$-I_2$	195	275	390	μA
Output current (pin 3) (LED driver transistor)	$-I_3$	–	–	50	mA
Switch "VCO-OFF" voltage at pin 7	V_{off}	–	2,2	–	V
Switch "VCO-OFF" current into pin 7	I_7	–	–	50	μA
A.C. Characteristics					
Overall gain (mono)	Go (V_o/V_i)	7	8	9,5	dB
Gain input amplifier (adjustable) (Fig. 5)	G	0	–	20	dB
AF output voltage (mono) (r.m.s. value)	$V_{1-5} = V_{2-5}$	800	900	–	mV
Output channel unbalance	$\Delta V_o/V_o$	–	± 0,2	± 1,0	dB
Total harmonic distortion at $V_{o(rms)}$ = 0,9 V (note 3)	THD	–	0,2	0,5	%
Total harmonic distortion at $V_{o(rms)}$ = 1,0 V	THD	–	1,0	–	%
Channel separation L = 1; R = 0	α	26	40	–	dB
Signal-to-noise ratio bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
Bandwidth IEC 79 (A-curve)	S/N	–	82	–	dB
Input impedance (external)	$\|Z_i\|$	–	47	–	kΩ
Output impedance (external) R = 12 kΩ; C = 3,9 nF	$\|Z_o\|$	–	9,3	–	kΩ

parameter	symbol	min.	typ.	max.	unit
SDS control (Fig. 6)					
10 dB channel separation	I_4	–	50	–	μA
Full stereo channel separation > 26 dB	I_4	100	–	–	μA
Full mono channel separation < 1 dB	I_4	–	–	10	μA
Stereo/mono switch					
R3 = 180 kΩ; note 4; Fig. 7					
Switching to stereo	V_i	–	18	24	mV
Switching to mono	V_i	8	–	–	mV
Hysteresis	ΔV_i	–	4	–	mV
Carrier and harmonic suppression at the output (note 5)					
Pilot signal suppression f = 19 kHz; R3 = 180 kΩ; note 4; Fig. 4	α_{19}	40	50	–	dB
Subcarrier suppression					
f = 38 kHz	α_{38}	–	50	–	dB
f = 57 kHz	α_{57}	–	50	–	dB
f = 228 kHz	α_{228}	–	80	–	dB
Intermodulation suppression (note 6)					
f_m = 10 kHz; spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	α_3	–	60	–	dB
VWF tone suppression f = 57 kHz (note 7)	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz (note 8)	α_{67}	–	80	–	dB
ACI rejection (note 9)					
f = 114 kHz	α_{114}	–	90	–	dB
f = 190 kHz	α_{190}	–	60	–	dB

Notes see next page.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Ripple rejection					
f = 100 Hz; V_{ripple} = 200 mV; measured including RC network in supply line					
V_P = 7,5 V	RR_{100}	–	42	–	dB
V_P = 6,0 V	RR_{100}	–	46	–	dB
V_P = 3,6 V	RR_{100}	–	35	–	dB
VCO					
Oscillator frequency adjustable with R8	f_{osc}	–	228	–	kHz
Capture range (deviation from 228 kHz centre frequency) V_{pilot} = 9% (note 10)	$\Delta f/f$	–	8	–	%
Temperature coefficient	TC	–	+ 400 x 10^{-6}	–	K^{-1}

Notes to the characteristics

1. Minimum supply voltage only applicable in 6 V portable.
2. Without LED-driver current.
3. Guaranteed for mono, mono + pilot, stereo.
4. Also adjustable.
5. Reference output voltage at 1 kHz (measured channel R, pin 2).
6. Intermodulation suppression (BFC: Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

7. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

8. SCA (Subsidary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})};\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

9. ACI (Adjacent Channel Interference) rejection at:

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}\ ;\ f_s = (3 \times 38\ \text{kHz}) - 110\ \text{kHz}$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})}\ ;\ f_s = (5 \times 38\ \text{kHz}) - 186\ \text{kHz}$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

10. The capture range of the PLL may be decreased to 4% by changing the value of C2 to 470 nF (see Fig. 4), if a small ambient temperature range is provided.

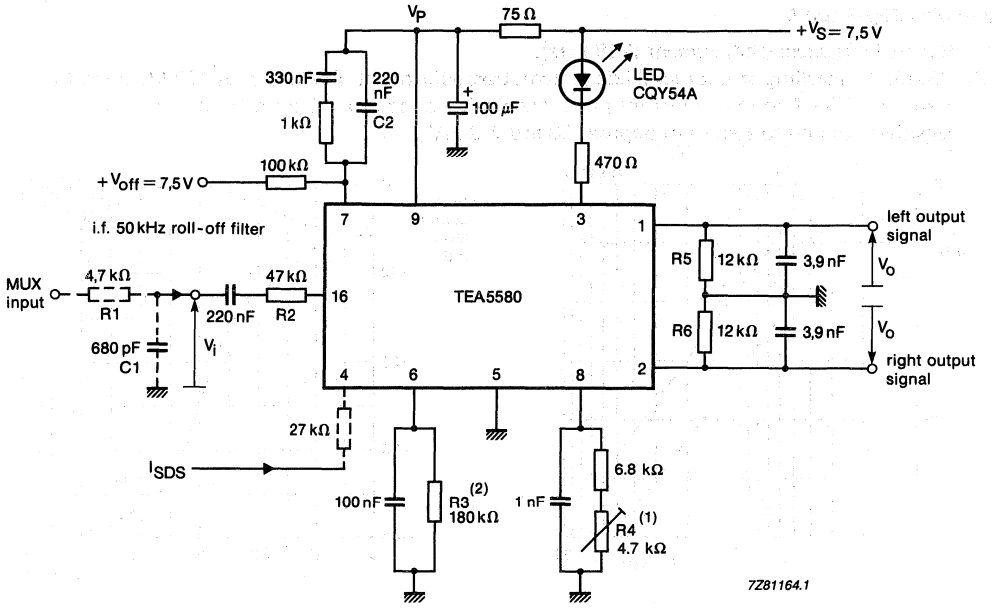


Fig. 3 Car radio application and test circuit.

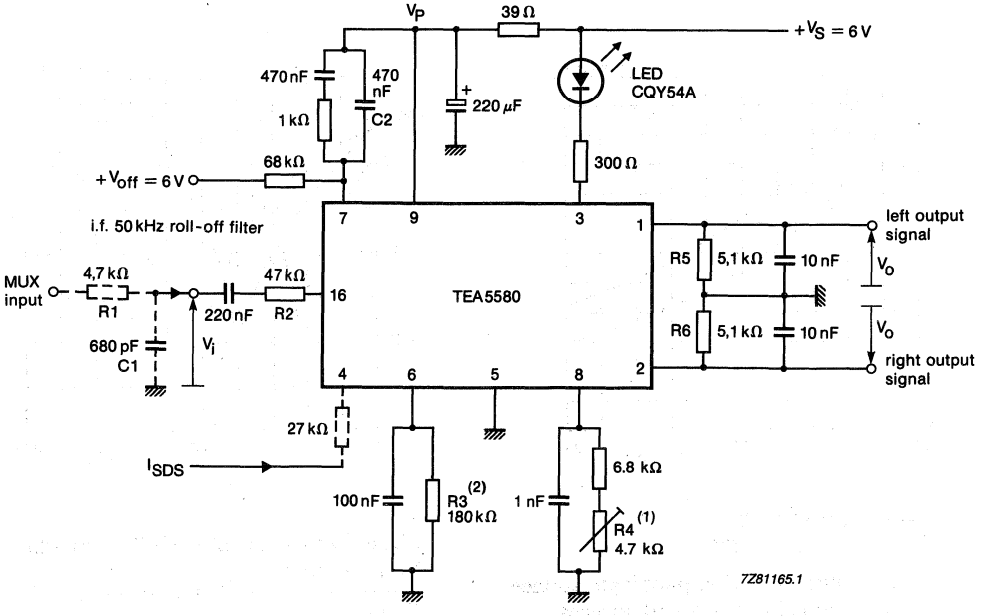
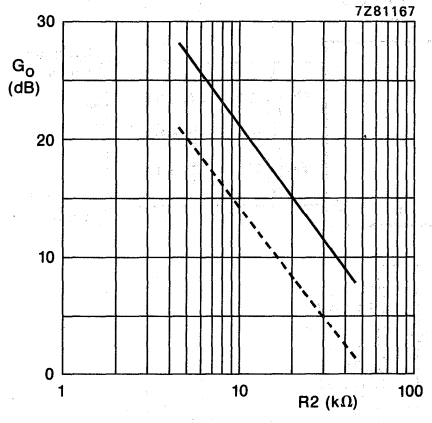


Fig. 4 Portable application circuit.

Notes to Figs 3 and 4

(1) R4: VCO frequency adjustment (228 kHz).

(2) R3: pilot cancelling or pilot level adjustment; best adjustment obtained with 470 kΩ potentiometer (see Figs 7 and 8); adjust for pilot cancellation of approx. 58 dB ± 10 dB and pilot sensitivity (mono to stereo) of approx. 23 mV ± 3 mV.



——— R5 = R6 = 12 kΩ

– – – R5 = R6 = 5,1 kΩ

Fig. 5 Overall gain as a function of input resistance (R2).

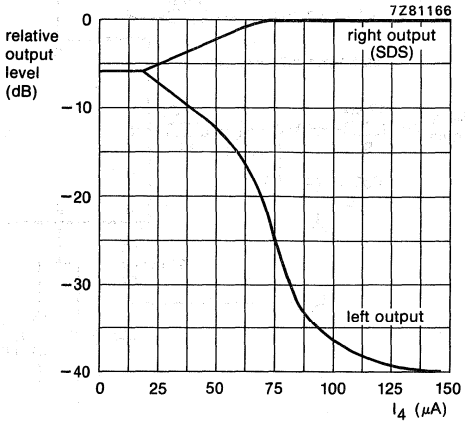
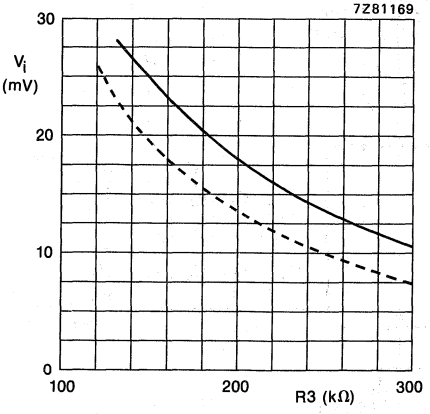


Fig. 6 Relative output level as a function of the signal dependent stereo (SDS) current (I_4); typical curves.



——— stereo "ON"

– – – stereo "OFF"

Fig. 7 Pilot sensitivity: pilot input voltage (V_i) as a function of pilot adjustment resistor R3; typical curves.

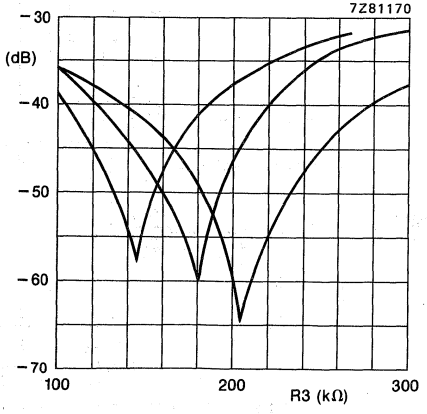


Fig. 8 Random samples of pilot cancelling: $\frac{V_o \text{ (at 19 kHz)}}{V_o \text{ (at 1 kHz)}}$ in dB as a function of R3; $V_{i(p\text{-}p)}$ = 1 V; V_{pilot} = 32 mV (9%).

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5581 PLL stereo decoder is for car and medium-fi radios. It incorporates all the features provided by the TEA5580 together with a source selector, muting circuit and output amplifiers with adjustable gain. It also features a switch for radio or cassette function and a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 40 dB. Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:

  third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;

  phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz stereo pilot tone (up to 25 dB)
- IF filter roll-off compensation
- Source selector for radio or cassette input (typ. 90 dB)
- Mute circuit for 90 dB (typ.) muting of the output level
- Matrix and two output buffers with adjustable gain (max. 20 dB)

PACKAGE OUTLINES

TEA5581 : 16-lead DIL; plastic (SOT38).
TEA5581T: 16-lead mini-pack; plastic (SO16L; SOT162A).

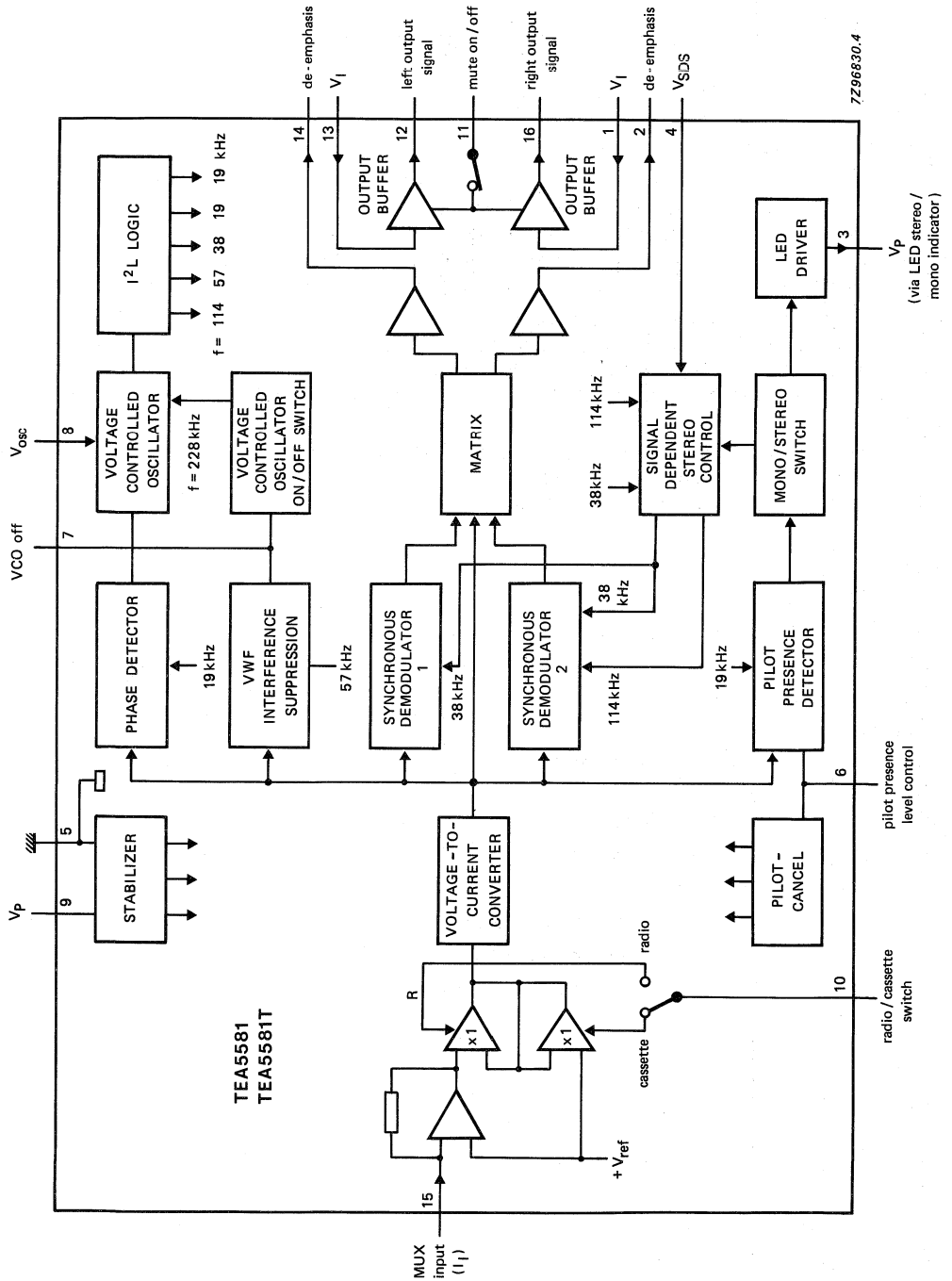


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)		$-I_{3M}$	–	75	mA
Total power dissipation		P_{tot}	see derating curve Fig. 2		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+80	°C
Electrostatic handling *		V_{es}	−600	+600	V

From junction to ambient in free air

SOT38	$R_{th\ j-a}$	75 K/W
SOT162	$R_{th\ j-a}$	95 K/W

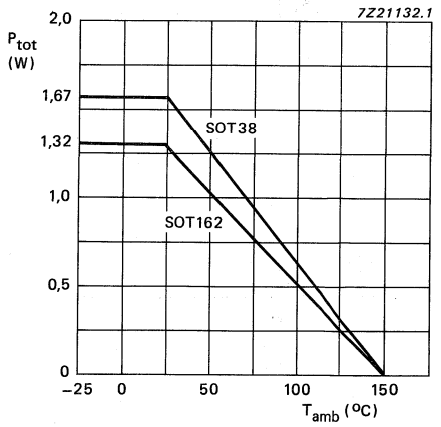


Fig. 2 Power derating curve.

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

DC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; all DC voltages are with respect to pin 5; all currents are positive into the IC.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	R1 = 75 Ω	V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	15	20	mA
Power dissipation		P_{tot}	–	125	–	mW
Voltage						
pin 15		V_{15}	–	2.1	–	V
pins 12 and 16		V_{12}, V_{16}	3.2	3.6	4.0	V
DC output current						
pins 2 and 14		$-I_{14}$, $-I_2$	225	320	450	μA
Output current						
pin 3		$-I_3$	–	–	20	mA
Switch "VCO-OFF"						
voltage		V_7	–	2.2	–	V
Switch "VCO-OFF"						
current		I_7	–	50	75	μA

AC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; AC measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV (9%); f_m = 1 kHz; oscillator adjusted to 228 kHz at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R_S and C_S in Fig. 7); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Transimpedance		V_O/I_I	0.13	0.15	0.17	V/μA
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R3 = 47 kΩ	G_o (V_o/V_i)	9.0	10.0	11.0	dB
AF output voltage (RMS value)		$V_{12} = V_{16}$	0.95	1.14	1.33	V
AF output voltage (RMS value)		$V_2 = V_{14}$	–	–	500	mV
Total harmonic distortion	note 1; $V_{O(rms)}$ = 1 V	THD	–	0.1	0.5	%
Output voltage	THD = 1%	$V_{12} = V_{16}$	–	1.5	–	V
Output channel unbalanced		V_{12}/V_{16}	–	0.2	1.0	dB
Channel separation	IF roll-off frequency = 50 kHz L = 1; R = 0	α	26	40	–	dB
S/N ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
SDS control	see Fig. 6					
Channel separation	V_4 = 1.0 V	α	5	10	15	dB
Full stereo	channel separation ⩾ 26 dB	V_4	–	1.2	1.25	V
Full mono	channel separation ⩽ 1 dB	V_4	0.75	0.8	–	V
Stereo/mono switch	note 2; see Fig. 5; R4 = 180 kΩ					
Switching to:						
stereo		V_{pilot}	–	14	20	mV
mono		V_{pilot}	4	–	–	mV
Hysteresis		ΔV_I	–	4.5	–	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f = 19 kHz; R4 = 180 kΩ; note 2; see Figs 3 and 4	α_{19}	32	40	–	dB
Subcarrier suppression						
f = 38 kHz		α_{38}	–	50	–	dB
f = 57 kHz		α_{57}	–	50	–	dB
f = 228 kHz		α_{228}	–	75	–	dB
Intermodulation suppression	note 4					
f_m = 10 kHz	spurious signal f_s = 1 kHz	α_2	–	50	–	dB
f_m = 13 kHz	spurious signal f_s = 1 kHz	α_3	–	50	–	dB
VWF tone suppression f = 57 kHz	note 5	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz	note 6	α_{67}	–	70	–	dB
ACI rejection	note 7					
f = 114 kHz		α_{114}	–	90	–	dB
f = 190 kHz		α_{190}	–	60	–	dB
Ripple rejection						
Ripple rejection	f = 100 Hz; V_{ripple} = 100 mV; mono	RR_{100}	–	50	–	dB
VCO						
Oscillator frequency adjustable with R5		f_{osc}	–	228	–	kHz
Capture range	deviation from 228 kHz centre frequency; V_{pilot} = 32 mV	$\Delta f/f$	–	6	–	%
Temperature coefficient	uncompensated	TC	–	-200×10^{-6}	–	K^{-1}

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector						
Suppression of MPX signal	$V_{10} \geqslant 2$ V	α	80	90	–	dB
Switching level	cassette to radio					
voltage		V_{IL}	–	–	0.8	V
current		I_{IL}	–	10	25	μA
Switching level	radio to cassette					
voltage		V_{IH}	2.0	–	V_S	V
current		I_{IH}	–	–	1	μA
Output amplifiers						
Gain	note 8; R_6/R_7	G_v	–	–	20	dB
Output impedance		Z_o	–	200	500	Ω
External load impedance		$\|Z_l\|$	5	–	–	kΩ
Suppression (mute)	$V_{11} = \leqslant 0{,}8$ V	α	84	90	–	dB
DC offset voltage at outputs during mute switching	mute OFF-to-ON	ΔV_{12}, ΔV_{16}	–	1.0	–	mV
	mute ON-to-OFF	ΔV_{12}, ΔV_{16}	–	2.0	–	mV
Muting circuit						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2.0	–	V_S	V
Input current	mute ON	I_{IL}	–	10	25	μA
	mute OFF	I_{IH}	–	–	1	μA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Also adjustable.
3. Reference output voltage at 1 kHz (measured channel R, pin 16).
4. Intermodulation suppression (Beat Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 1\ kHz)};\ f_s = (2 \times 10\ kHz) - 19\ kHz$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 1\ kHz)};\ f_s = (3 \times 13\ kHz) - 38\ kHz$$

   measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

5. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 1\ kHz \pm 23\ Hz)}$$

   measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

6. SCA (Subsidiary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 9\ kHz)};\ f_s = (2 \times 38\ kHz) - 67\ kHz$$

   measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

7. ACI (Adjacent Channel Interference) rejection at:

$$\alpha 114 = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 4\ kHz)};\ f_s = (3 \times 38\ kHz) - 110\ kHz$$

$$\alpha 190 = \frac{V_{o(signal)}\ (\text{at } 1\ kHz)}{V_{o(spurious)}\ (\text{at } 4\ kHz)};\ f_s = (5 \times 38\ kHz) - 186\ kHz$$

   measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

8. Maximum permitted value of feedback resistor = 220 kΩ.

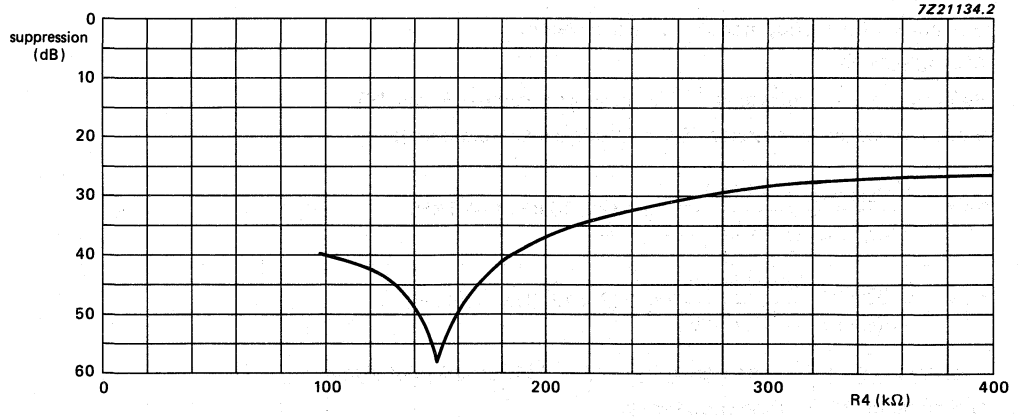
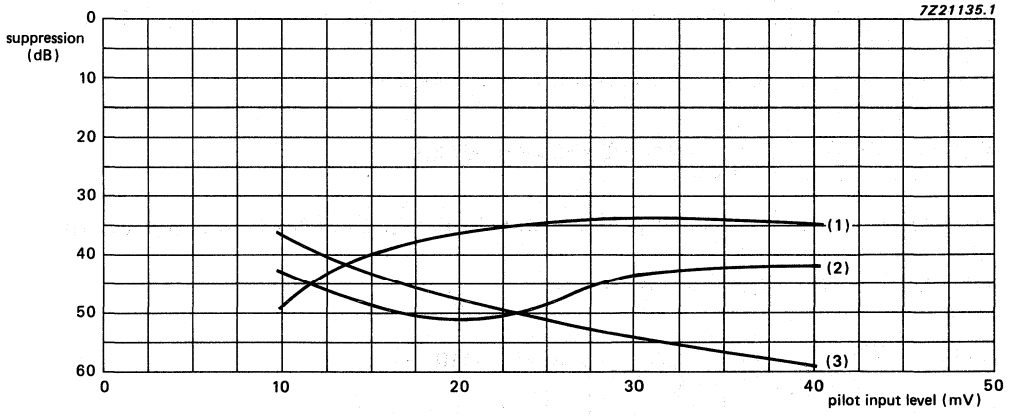
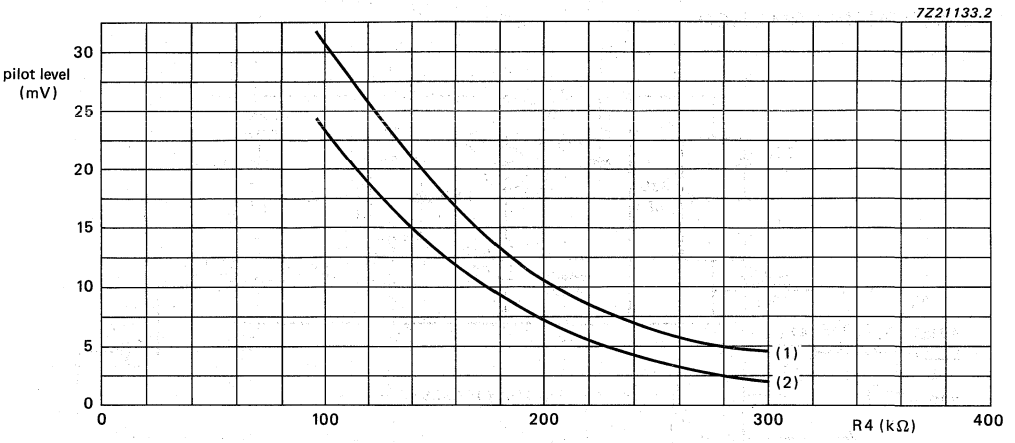


Fig. 3 Pilot suppression plotted against resistance (R4).



(1) 220 kΩ
(2) 180 kΩ
(3) 150 kΩ

Fig. 4 Pilot suppression plotted against pilot input voltage level.



(1) Switching from mono to stereo.
(2) Switching from stereo to mono.

Fig. 5 Pilot sensitivity against resistance (R4).

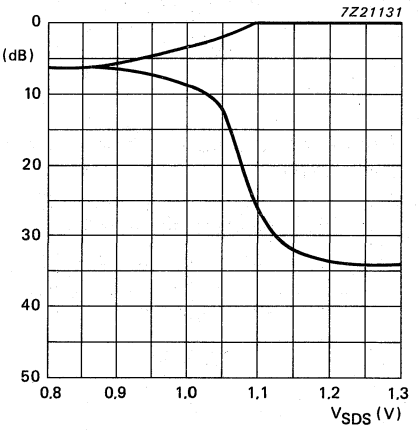
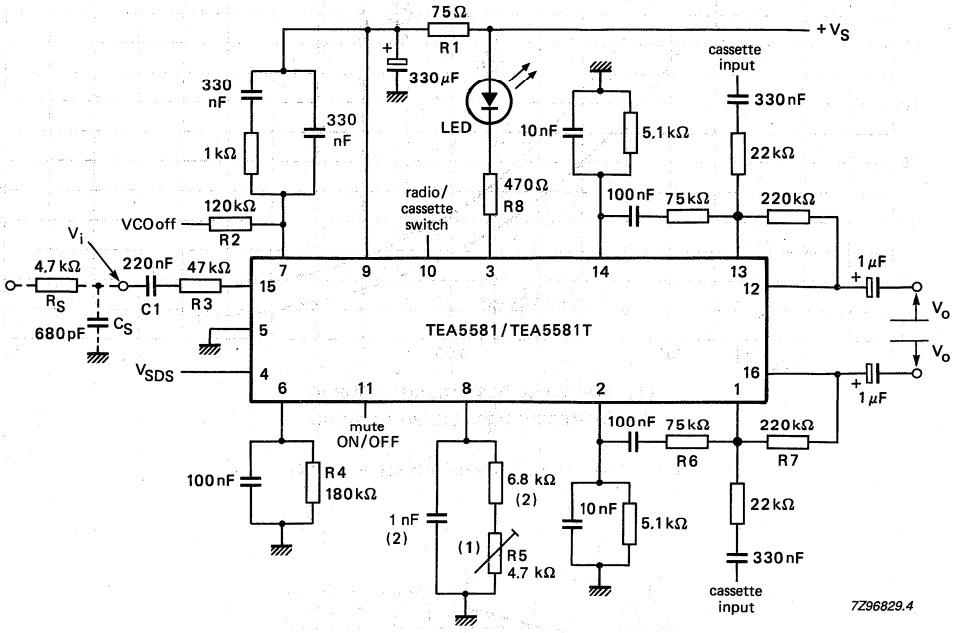


Fig. 6 Channel separation against V_{SDS}.

APPLICATION INFORMATION



(1) 25% tolerance (all other resistors have a 5% tolerance).
(2) 1% tolerance (NP0).

Fig. 7 Application diagram.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591 is an integrated radio circuit which is designed for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. The main advantage of this IC is its ability to operate over a wide range of supply voltages without loss of performance. The AM circuit incorporates a balanced mixer and a 'one-pin' oscillator, which operates in the 0.6 MHz to 30 MHz frequency range, with amplitude control. The circuit also includes an IF amplifier, a detector and an AGC circuit which controls the IF amplifier and the mixer. The FM circuit incorporates an RF amplifier, a balanced mixer and a 'one-pin' oscillator together with two AC coupled IF amplifiers (with distributed selectivity), a quadrature demodulator for the ceramic filter and internal AFC.

Features

- DC AM/FM switch facility
- Three internal separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 9) are ESD protected

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	3.0	15	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 13)	m = 0.3					
RF sensitivity						
RF input voltage	V_o = 10 mV	V_i	–	3.5	–	μV
RF input voltage	(S+N)/N = 26 dB	V_i	–	17	–	μV
Signal plus noise-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.7	–	%
FM performance (pin 1)	Δf = 22.5 kHz					
RF sensitivity						
RF input voltage						
−3 dB before limiting		V_i	–	2.3	4.0	μV
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)	V_i = 3.0 μV	(S+N)/N	23	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

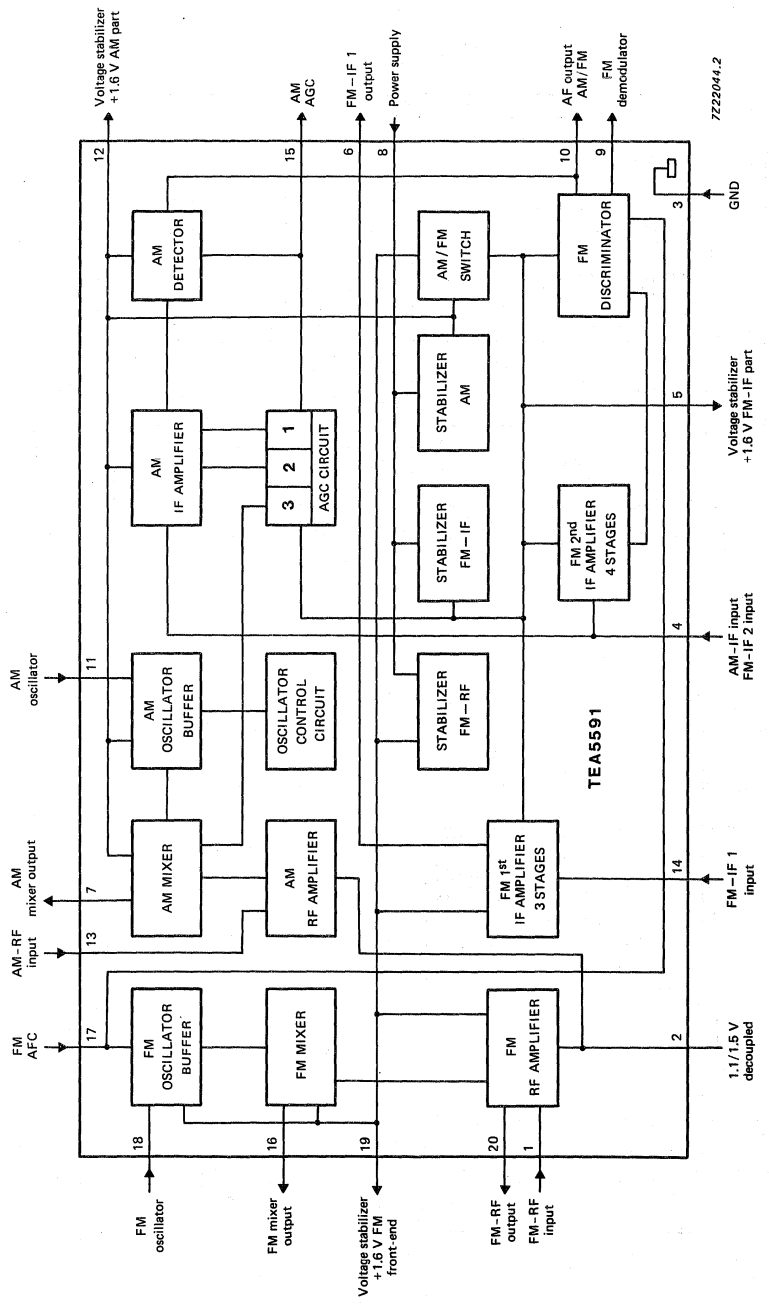


Fig.1 Block diagram.

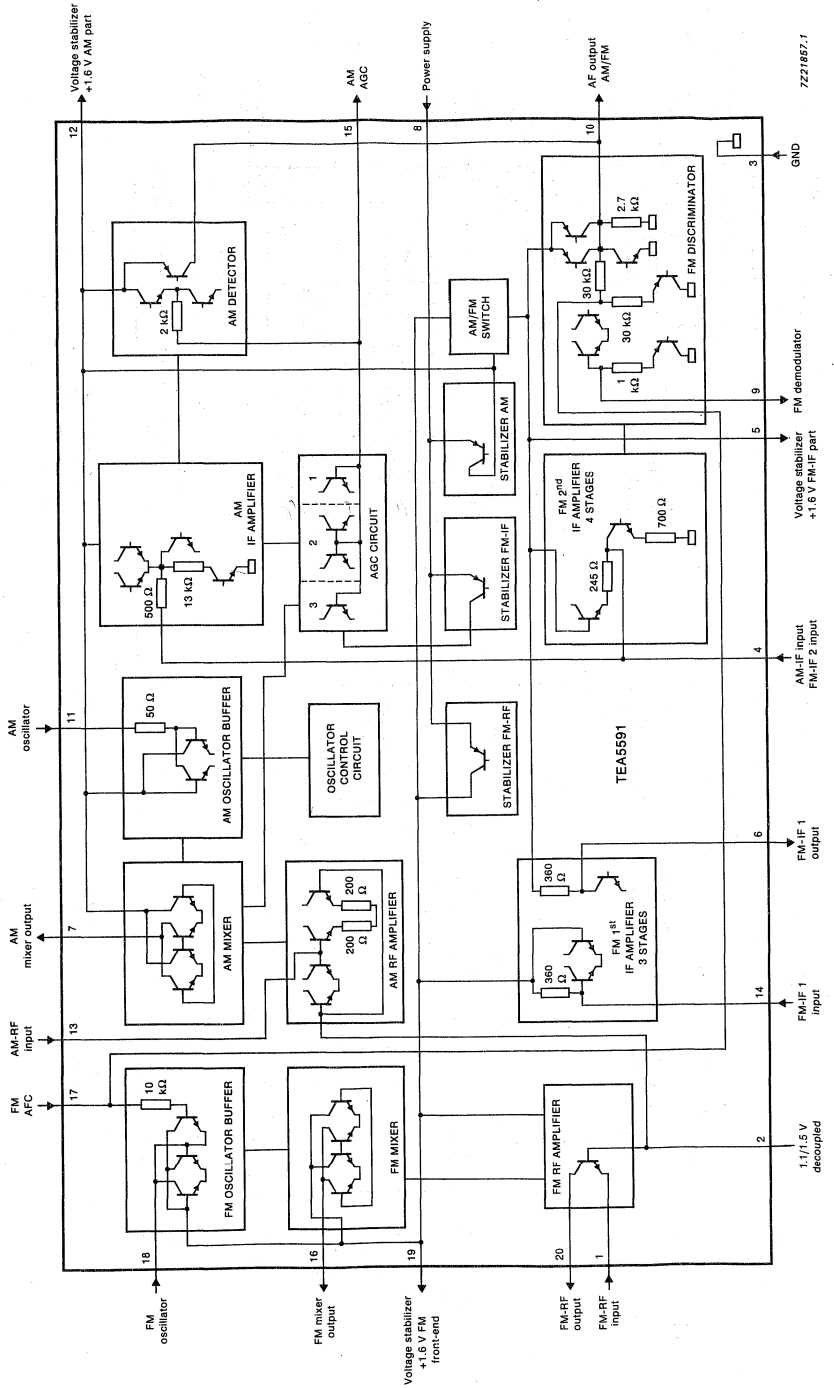


Fig.2 Equivalent circuit diagram.

PINNING

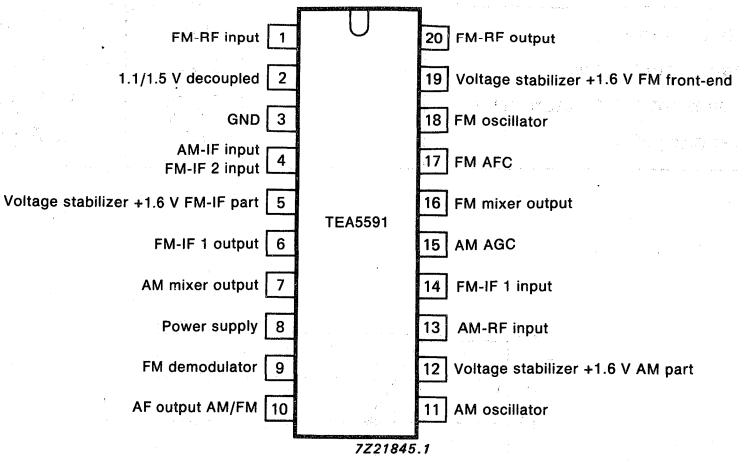


Fig.3 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−15	+ 60	°C
Total power dissipation		P_{tot}	see Fig.4		

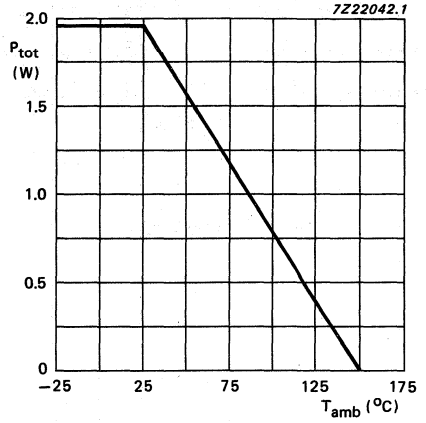


Fig.4 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 3; all input currents are positive; all parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 1		V_1	–	0.90	–	V
pin 2		V_2	–	1.60	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	1.5	1.60	1.75	V
pin 6		V_6	–	1.48	–	V
pin 9		V_9	–	1.05	–	V
pin 14		V_{14}	–	1.63	–	V
pin 17		V_{17}	–	0.60	–	V
pin 19		V_{19}	–	1.60	–	V
Voltages (AM)						
pin 2		V_2	–	1.10	–	V
pin 12		V_{12}	–	1.60	–	V
pin 15		V_{15}	–	1.54	–	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PART						
Input conductance pin 4	f = 0.5 MHz	g_{ie}	–	1.7	–	ms
Input capacitance pin 4	f = 0.5 MHz	C_{ie}	–	5	–	pF
Input conductance pin 13	f = 1.0 MHz	g_{ie}	–	230	–	μs
Input capacitance pin 13	f = 1.0 MHz	C_{ie}	–	13	–	pF
Output conductance pin 7	f = 0.5 MHz	g_{oe}	–	4	–	μs
Output capacitance pin 7	f = 0.5 MHz	C_{oe}	–	4.7	–	pF
Conductance pin 11	f = 1.5 MHz	g_e	–	–6.8	–	ms
Capacitance pin 11	f = 1.5 MHz	C_e	–	25	–	pF
FM PART						
Input conductance pin 4	f = 10.7 MHz	g_{ie}	–	2.7	–	ms
Input capacitance pin 4	f = 10.7 MHz	C_{ie}	–	6	–	pF
Input conductance pin 14	f = 10.7 MHz	g_{ie}	–	2.8	–	ms
Input capacitance pin 14	f = 10.7 MHz	C_{ie}	–	2.5	–	pF
Output conductance pin 6	f = 10.7 MHz	g_{oe}	–	2.8	–	ms
Output capacitance pin 6	f = 10.7 MHz	C_{oe}	–	3.0	–	pF
Output conductance pin 16	f = 10.7 MHz	g_{oe}	–	1.6	–	μs
Output capacitance pin 16	f = 10.7 MHz	C_{oe}	–	4.5	–	pF
Conductance pin 9	f = 10.7 MHz	g_e	–	880	–	μs
Capacitance pin 9	f = 10.7 MHz	C_e	–	3.6	–	pF
Conductance pin 18	f = 100 MHz	g_e	–	–4	–	ms
Capacitance pin 18	f = 100 MHz	C_e	–	10	–	pF

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PERFORMANCE						
RF sensitivity						
AF output voltage for: V_i = 7.5 μV	no AGC	V_o	16	30	40	mV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage of V_i = 17 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	48	–	dB
Optimum source impedance		Z_S	–	1.8	–	kΩ
Noise factor	optimum noise impedance	NF	–	4	–	dB
AGC						
Change in RF input voltage for 10 dB change in output voltage	V_{i1} = 100 mV	V_{i1}/V_{i2}	80	86	–	dB
AF output voltage	V_i = 100 μV	V_o	40	50	60	mV
Total harmonic distortion	V_i = 100 μV to 10 mV	THD	–	0.7	1.5	%
	V_i = 100 μV to 10 mV; m = 0.8	THD	–	3	5	%
	V_i = 80 mV; m = 0.8	THD	–	–	8	%

Transimpedance (Z_{tr}) = v_4/i_7 = 900Ω.

parameter	conditions	symbol	min.	typ.	max.	unit
IF suppression (note 1)	V_o = 30 mV	α	–	20	–	dB
Oscillator (pin 11)						
Input voltage	f_{osc} = 1.5 MHz	V_{osc}	–	150	190	mV
	f_{osc} = 30.5 MHz	V_{osc}	–	150	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
Temperature behaviour	–15 to + 60 °C (only the IC)					
Sensitivity		ΔV_i	–	–2	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	1	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	500	–	Hz
MW		Δf_{osc}	–	300	–	Hz
SW		Δf_{osc}	–	100	–	kHz
Supply voltage behaviour	V_P = 1.8 to 15 V					
Sensitivity		ΔV_i	–	0	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	0.5	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	6	–	kHz
MW		Δf_{osc}	–	0.1	–	kHz
SW		Δf_{osc}	–	30	–	kHz

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

RF conditions: Input frequency 100 MHz; frequency deviation f = ± 22,5 kHz and f_{mod} = 1 kHz

parameter	conditions	symbol	min.	typ.	max.	unit
FM PERFORMANCE						
RF sensitivity						
RF input voltage	−3 dB before limiting	V_{iFM}	–	2.3	4.0	μV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)						
V_i = 3.0 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	60	–	dB
Optimum source impedance		Z_{source}	–	50	–	Ω
Noise factor	optimum source impedance	NF	–	6	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion	V_i = 30 μV to 50 mV	THD	–	0.8	–	%
	V_i = 1 mV; Δf = 75 kHz	THD	–	3	–	%
	V_i = 100 mV; Δf = 75 kHz	THD	–	3	–	%
AM suppression	note 2					
RF input signal	V_i = 100 μV to 10 mV	AMS	–	50	–	dB
Oscillator voltage (pin 18)	f_{osc} = 100 MHz	V_{osc}	–	220	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
IF rejection ratio		IF_{rr}	–	60	–	dB
AFC	f_{osc} = 111.2 MHz					
	V_{17} = 1.4 V	Δf	–	−620	–	kHz
	V_{17} = 0.2 V	Δf	–	+420	–	kHz

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature behaviour	−15 to +60 °C (only the IC)					
RF sensitivity	−3 dB limiting	ΔV_i	–	−6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	−2	–	dB
Oscillator frequency		Δf_{osc}	–	−0.3	–	%
Supply voltage behaviour	Vp = 1.8 to 15 V					
RF sensitivity	−3 dB limiting	ΔV_i	–	6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	0.5	–	dB
Oscillator frequency		Δf_{osc}	–	100	–	kHz
Oscillator voltage		ΔV_{osc}	–	1.0	–	dB

Notes to the AC characteristics

1. $\alpha = \frac{V_i \text{ at } f_i = 455 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$.
2. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

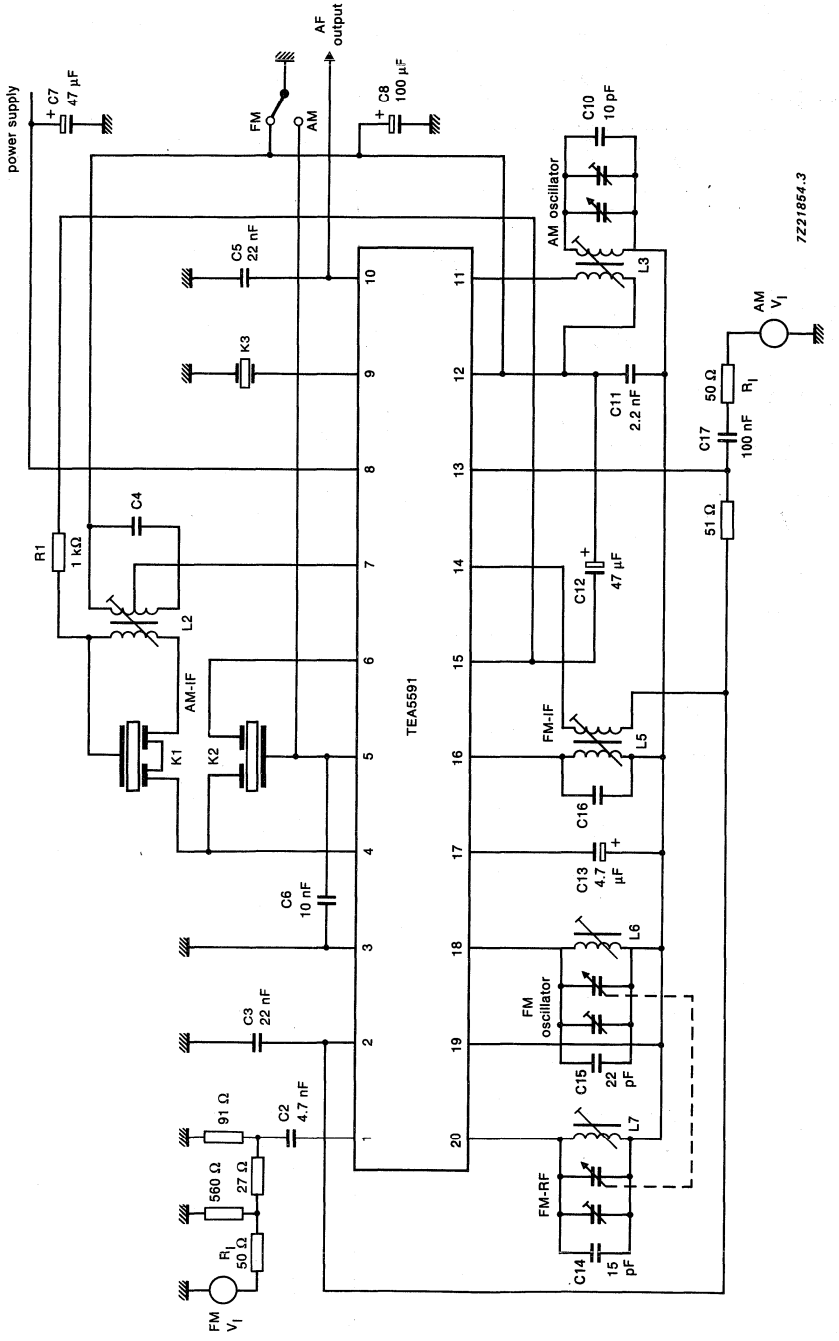


Fig.5 Test circuit.

APPLICATION INFORMATION

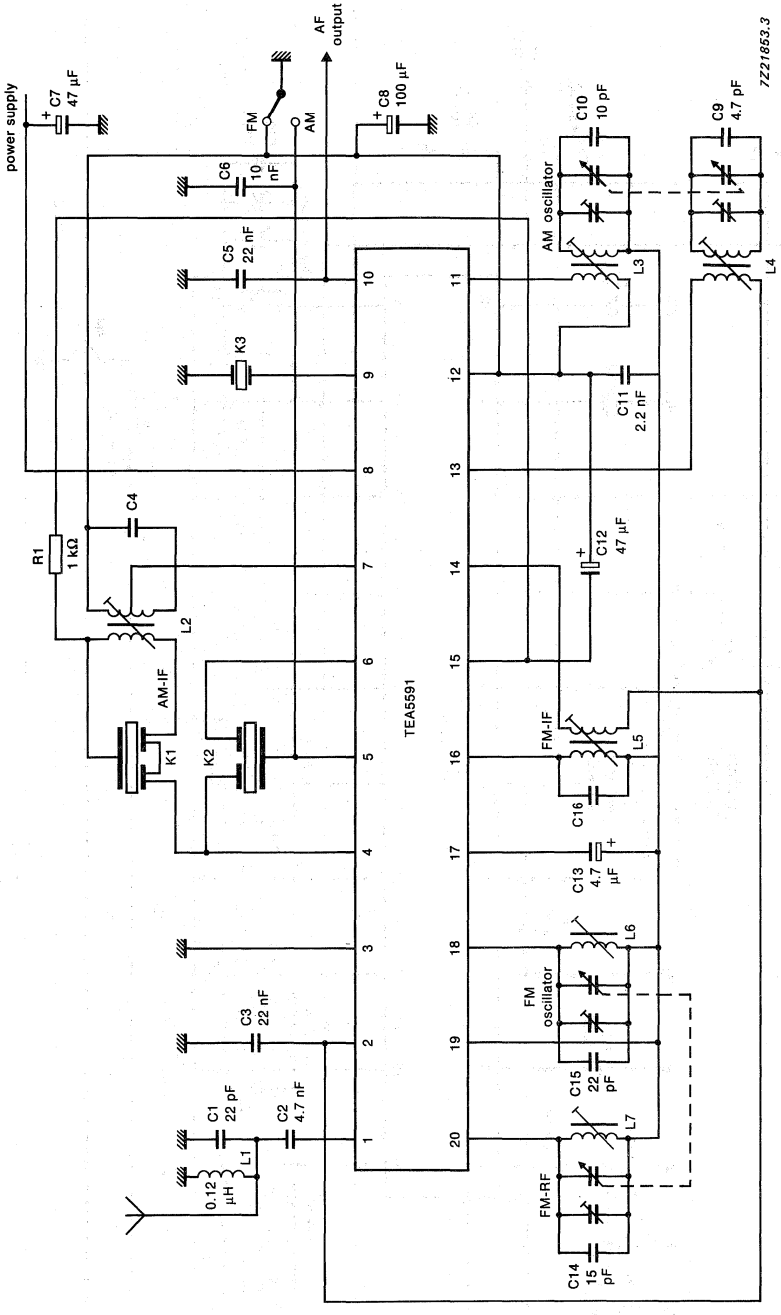
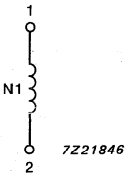


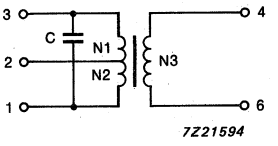
Fig.6 Application diagram.

Component data



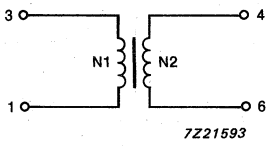
N1 = 4.5
L = 0.12 μH
Wire = 0.8 mm diameter
diameter = 4.5 mm

Fig.7 FM BFP coil (L1).



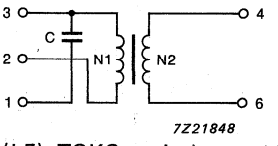
N1 = 132
N2 = 14
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
fo = 468 kHz
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7MCS

Fig.8 AM IF coil (L2). TOKO sample no. 7MCS-7P.



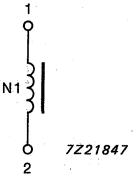
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7BRS

Fig.9 Oscillator coil (L3). TOKO sample no. 7BRS-7P.



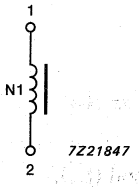
N1 = 11
N2 = 2
C = 85 pF (internal)
fo = 10.7 MHz

Fig.10 FM IF coil (L5). TOKO equivalent no. 119ACS-30120M.



N1 = 1.5
L = 0.03 μH

Fig.11 Oscillator coil (L6). TOKO equivalent no. 301SN-0100.



N1 = 2.5
L = 0.05 μH

Fig.12 FM RF coil (L7). TOKO equivalent no. 301SN-0200.

Ferroceptor coil

L4: N1 = 105; N2 = 10; L = 625 μH

Ceramic Filters

AM IF (K1). SFZ468 HL.
FM IF (K2). SFE10 . 7 MS2.
FM detector (K3). CDA10 . 7 MC1.

Tuning capacitors

AM 140/82 pF
FM 2 x 20 pF

APPLICATION INFORMATION (continued)

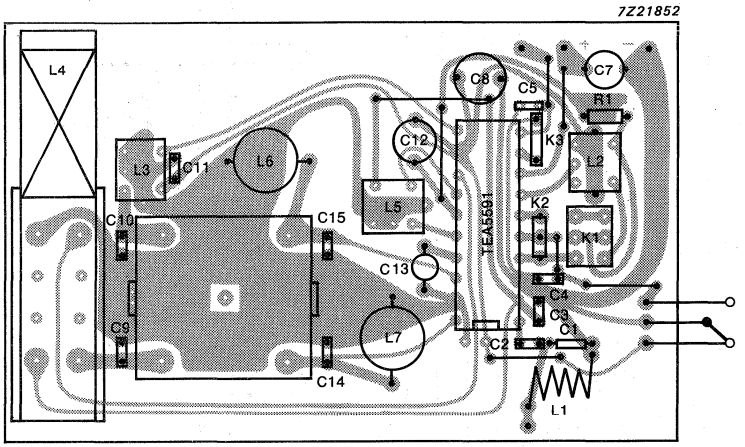


Fig.13 Printed-circuit board component side, showing component layout. For circuit diagram see Fig.6.

Physical dimensions of the printed circuit board = 5.0 x 8.1 cm.

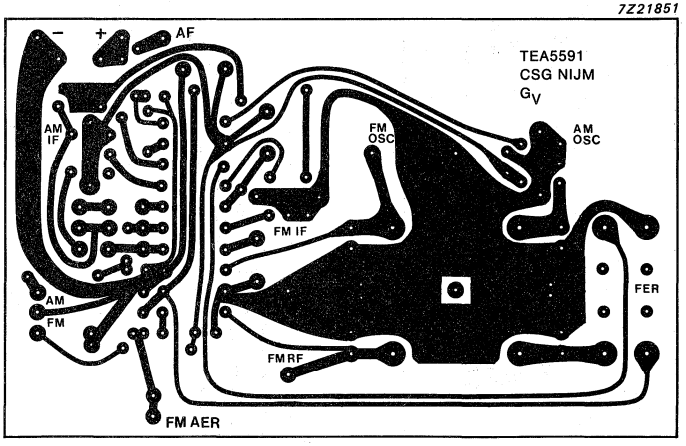


Fig.14 Printed-circuit board showing track side.

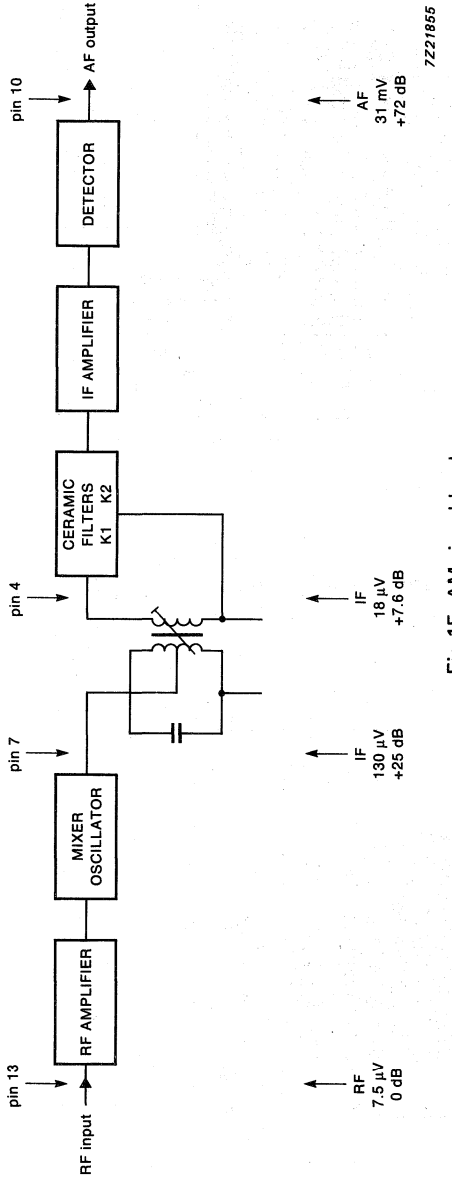


Fig.15 AM signal levels.

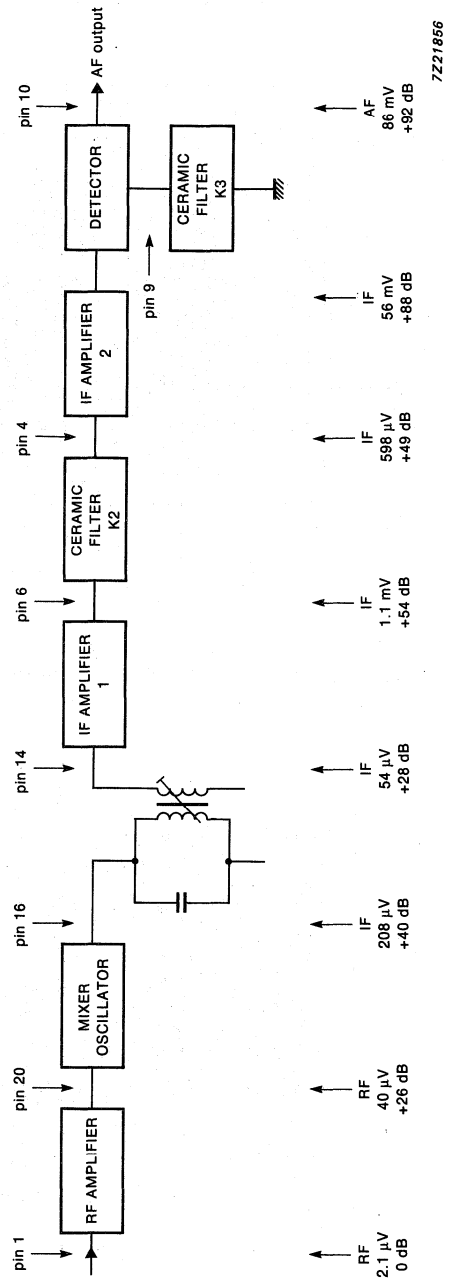


Fig.16 FM signal levels.

APPLICATION INFORMATION (continued)

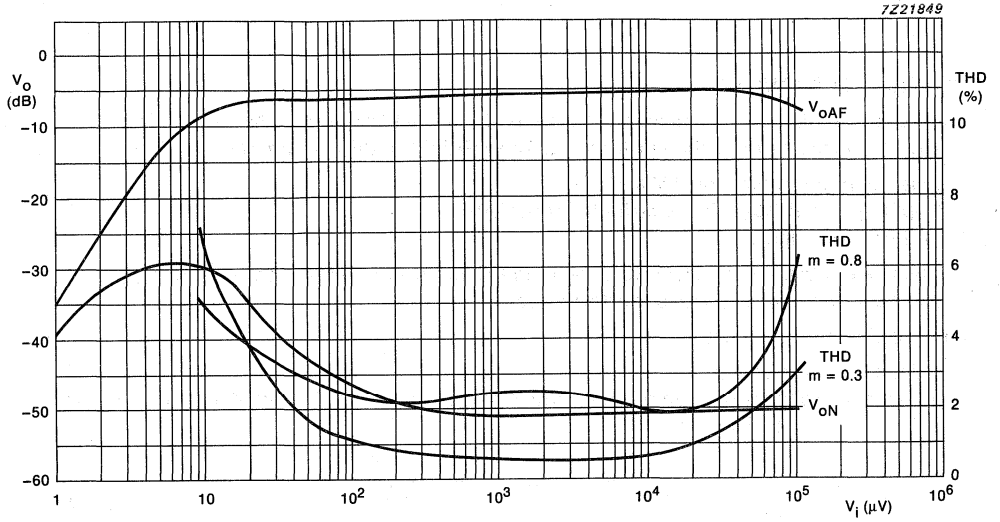


Fig.17 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV, and total harmonic distortion (THD) as a function of input voltage (V_i) at pin 13. Measured in test circuit Fig.5. AM AGC is measured at f_i = 1 MHz; f_{mod} = 1 kHz; m = 0.3. AM distortion is measured at f_i = 1 MHz; f_{mod} = 1 kHz.

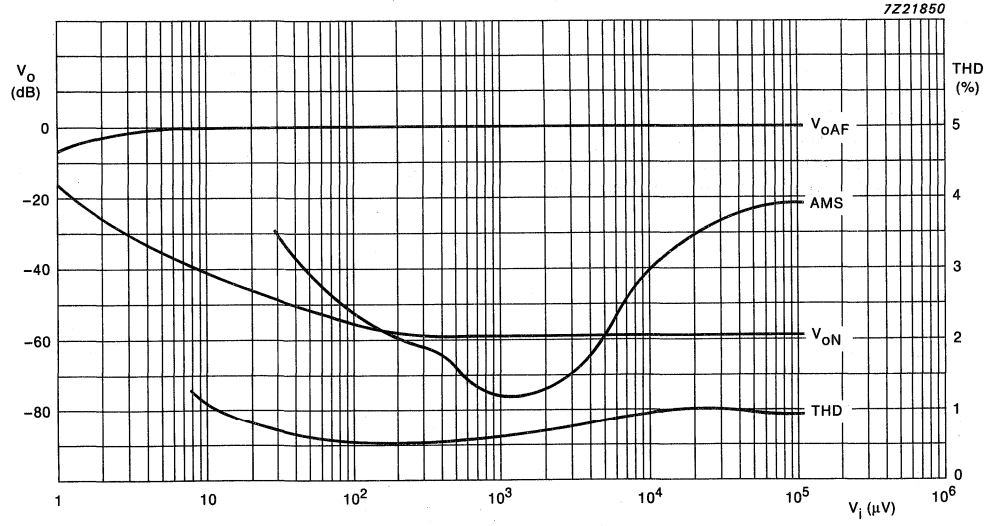


Fig.18 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV; AM suppression (AMS) and total harmonic distortion (THD) as a function of input voltage (V) at pin 1. Measured in test circuit Fig.5 at f_i = 98 MHz; f_{mod} = 1 kHz; Δf 22.5 kHz. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591A is a 24-pin integrated radio circuit, derived from the TEA5591 and is designed for use in AM/FM portable radios and clock radios. The TEA5591A differs from the TEA5591 in that it has:

- Separate IF input pins for AM and FM
- A split-up AM-IF stage (for distributed selectivity)
- An LED driver indicator

The main advantage of the TEA5591A is its ability to operate over a wide range of supply voltages (1.8 to 15 V) without any loss of performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- A split-up IF amplifier
- A detector
- An AGC circuit which controls the IF amplifier and mixer.

The FM circuit incorporates:

- An RF input amplifier
- A double balanced mixer
- A 'one pin' oscillator
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- LED AM/FM indicator
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 10) are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	–	15	V
Total current consumption						
AM part		I_P	–	14	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 1)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S + N)/N = 26 dB	V_i	–	17	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S + N)/N	–	48	–	dB
AF output voltage		V_o	–	45	–	mV
Total harmonic distortion		THD	–	0.7	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 2)	note 2					
Limiting sensitivity	−3 dB	V_i	–	2.3	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S + N)/N	–	26	–	dB
	V_i = 1 mV	(S + N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling		V_i	–	100	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

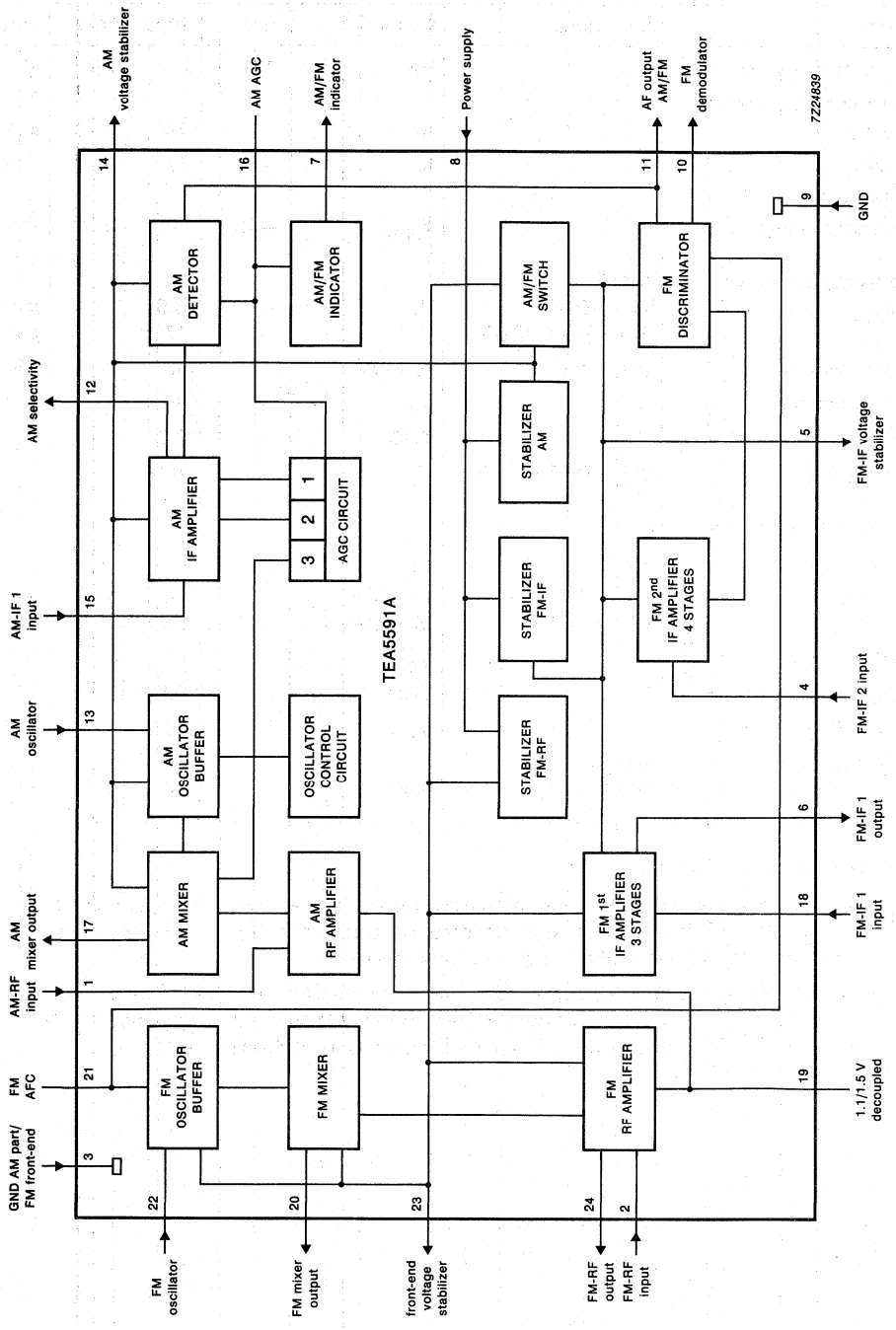


Fig.1 Block diagram.

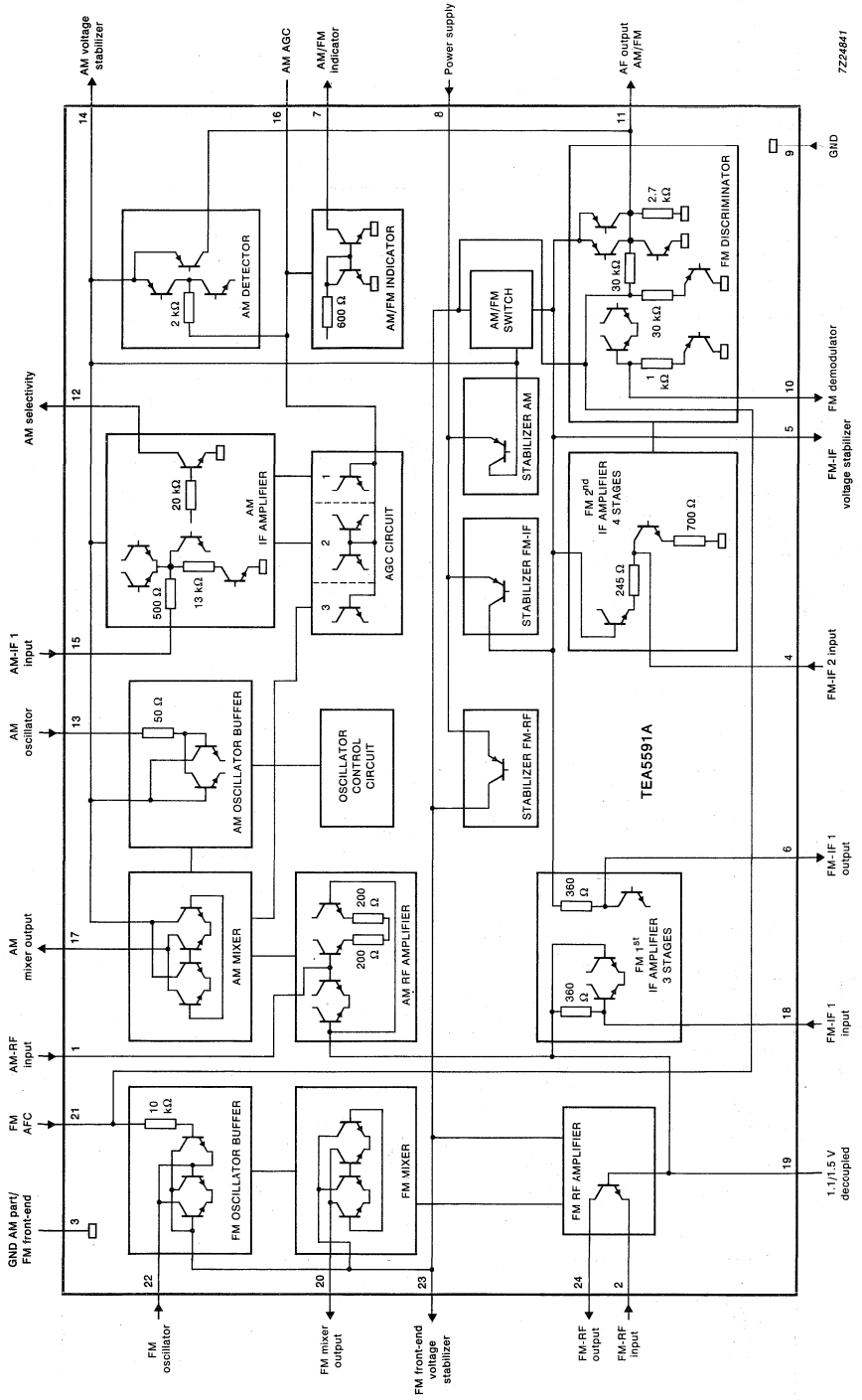


Fig.2 Equivalent circuit diagram.

PINNING

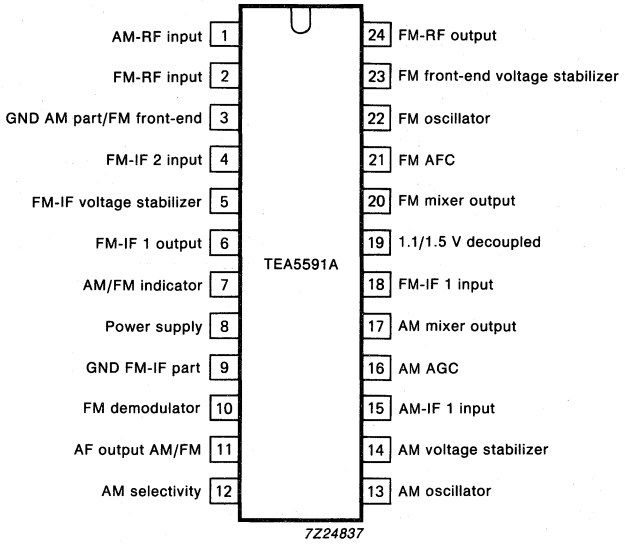


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
LED current (pin 7)		I_7	–	*	mA
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−15	+60	°C
Electrostatic handling**		V_{es}	−1000	+1000	V

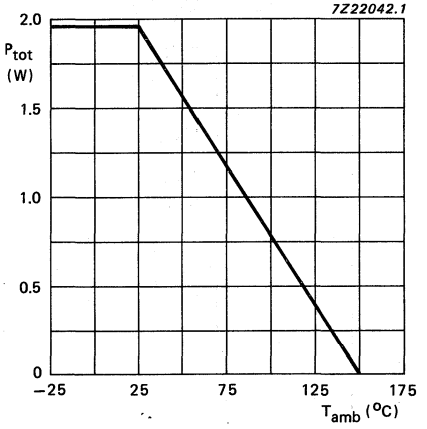


Fig.4 Power derating curve.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 3 and pin 9; all input currents are positive; all parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 2		V_2	–	0.90	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	–	1.60	–	V
pin 6		V_6	–	1.48	–	V
pin 10		V_{10}	–	1.05	–	V
pin 18		V_{18}	–	1.60	–	V
pin 19		V_{19}	–	1.58	–	V
pin 21		V_{21}	–	0.69	–	V
pin 23		V_{23}	–	1.60	–	V
Voltages (AM)						
pin 14		V_{14}	–	1.60	–	V
pin 16		V_{16}	–	1.54	–	V
pin 19		V_{19}	–	1.10	–	V
Total current consumption	note 1					
AM part		I_P	–	14	19	mA
FM part		I_P	–	17	23	mA

Note to the DC characteristics

1. Without LED current.

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM part						
AM front end (pin 1 to 17)	note 1					
Conversion transconductance	V_i = 10 mV; V_{AGC} (pin 16) = V_{14} − 0.1 V	S_C	9.3	12	13.5	mA/V
	V_i = 10 mV; V_{AGC} (pin 16) = V_{14} − 0.45 V	S_C	0.75	1.1	1.3	mA/V
IF suppression	note 2; V_i = 10 mV	α	20	26	–	dB
Oscillator (pin 13)						
Voltage	f = 1.5 MHz	V_{osc}	110	175	200	mV
	f = 1.5 MHz; V_P = 1.5 V	V_{osc}	60	160	–	mV
IF and detector part (pin 15 to 11)	note 3					
IF sensitivity; AF output voltage	no AGC; V_i = 45 μV	V_o	12	20	55	mV
Signal + noise to noise ratio for an IF input	no AGC; V_i = 45 μV	S+N/N	23	25	–	dB
AF output voltage	V_i = 1 mV	V_o	35	45	60	mV
Total harmonic distortion	V_i = 10 mV; m = 80%	THD	–	1	2.2	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	*	*	μA
	V_i = 1 mV	I_{ind}	*	*	–	mA
Overall performance (pin 1 to 11)	note 4					
Total harmonic distortion	V_i = * mV	THD	–	4.5	8	%

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
FM part						
FM front end (pin 2 to 20)	note 5					
Conversion transconductance	V_i = 1 mV	S_C	7.5	11	13.5	mA/V
Oscillator (pin 22)						
Voltage	V_{AFC} (pin 21) = 0.8 V	V_{osc}	155	200	245	mV
	V_{AFC} = 0.8 V V_P = 1.5 V	V_{osc}	60	120	–	mV
AFC control; change in oscillator frequency	V_{AFC} = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = –0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	–620	–	kHz
IF and demodulator part (pin 18 to 11)	note 6					
IF sensitivity; AF output voltage	note 7 V_i = 100 μV	V_o	–3	–1	0	dB
Signal + noise to noise ratio for an IF input	V_i = 100 μV; out of limiting	S+N/N	26	30	–	dB
AF output voltage	V_i = 1 mV	V_o	75	90	120	mV
Total harmonic distortion	Δf = 75 kHz V_i = 50 mV	THD	–	3	–	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	–	20	μA
	V_i = 1 mV	I_{ind}	0.6	1	1.9	mA

Notes to the AC characteristics

1. Input frequency = 1 MHz; output frequency = 468 kHz.
2. $$\alpha = \frac{(V_o \text{ at } f_i = 1 \text{ MHz})}{(V_o \text{ at } f_i = 468 \text{ kHz})}$$
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

APPLICATION AND TEST INFORMATION

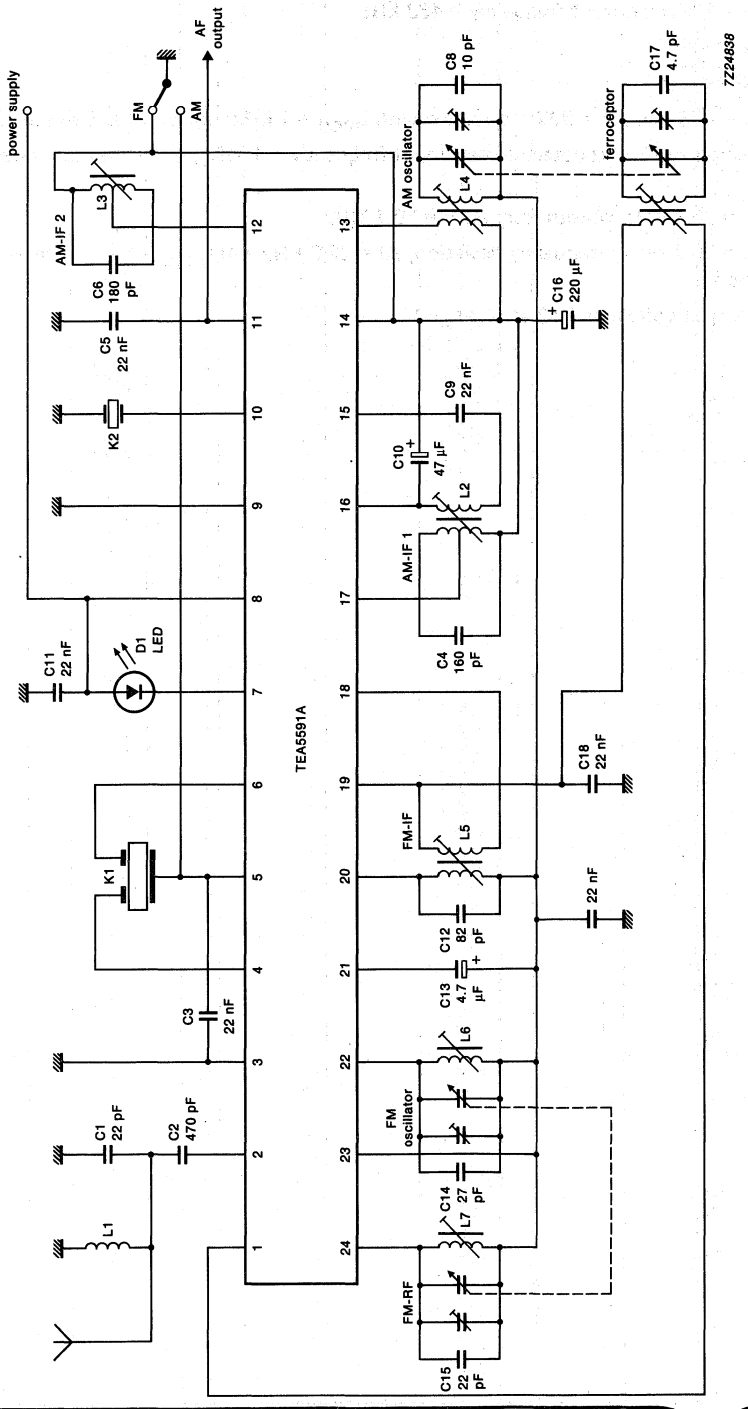


Fig.5 Application circuit.

DEVELOPMENT DATA

APPLICATION AND TEST INFORMATION (continued)

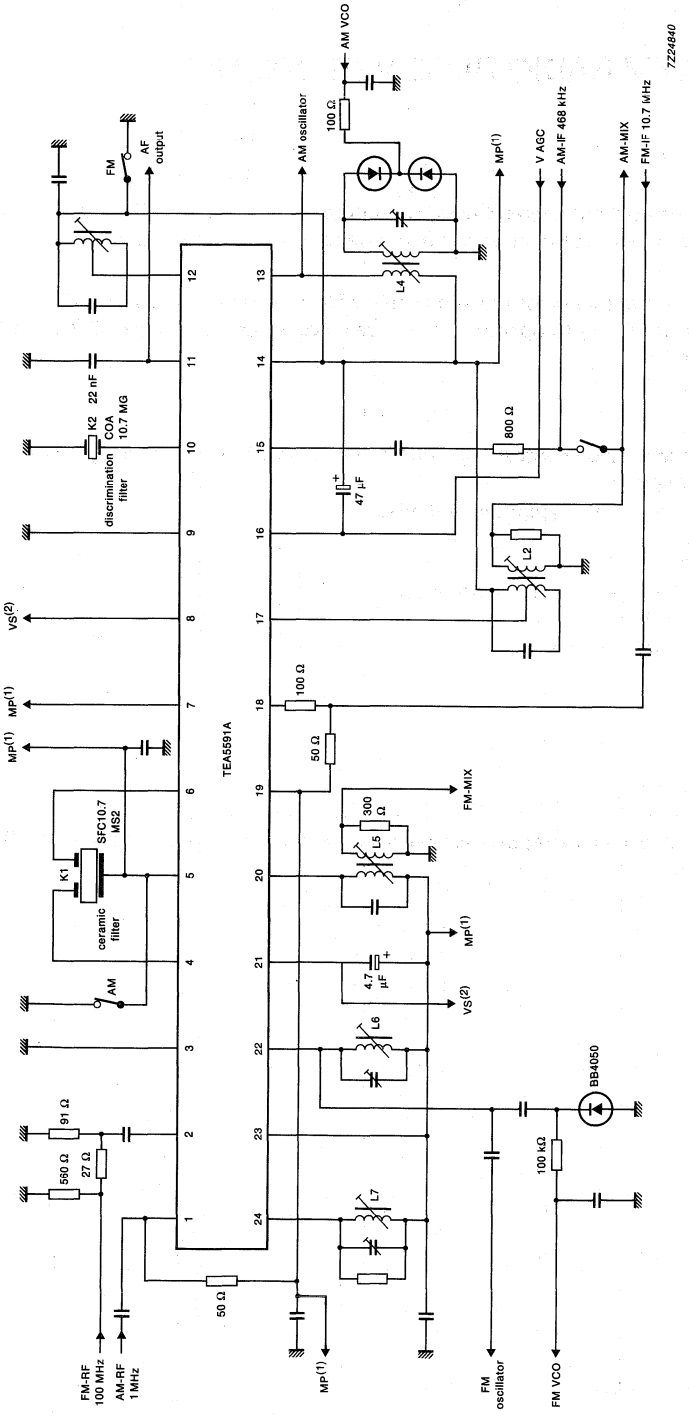


Fig.6 Test circuit.

(1) MP = measurement pin.
(2) VS = voltage source.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5592 is a 24-pin integrated radio circuit designed for use in all personal audio and car radio sets especially those sets with in- and out-door aerials that have to fulfill the FTZ (Amtsblatt) requirements.

The AM-IF and FM-IF stages are designed for the application of lumped selectivity. The main advantage of the TEA5592 is its ability to operate over a wide range of supply voltages (2.7 to 15 V) without any loss in performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (designed for FTZ (Amtsblatt) radio sets)
- A 5-stage IF amplifier
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (2.7 to 15 V)
- All pins are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+85	°C
AM performance (pin 13)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	1.5	–	μV
	(S+N)/N = 26 dB	V_i	–	15	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	55	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 22)	note 2					
Limiting sensitivity	−3 dB	V_i	–	1.8	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S+N)/N	–	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage		V_o	–	110	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

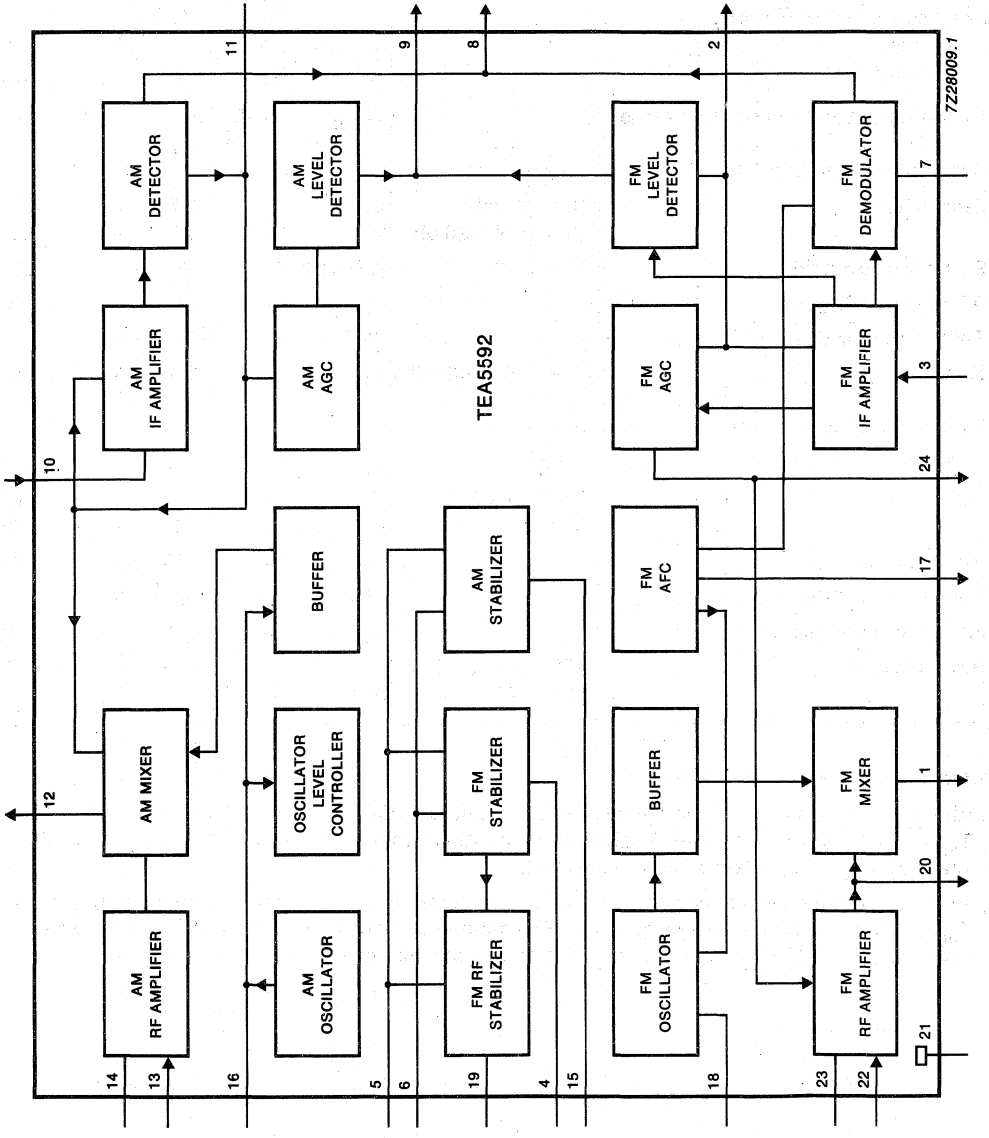


Fig.1 Block diagram.

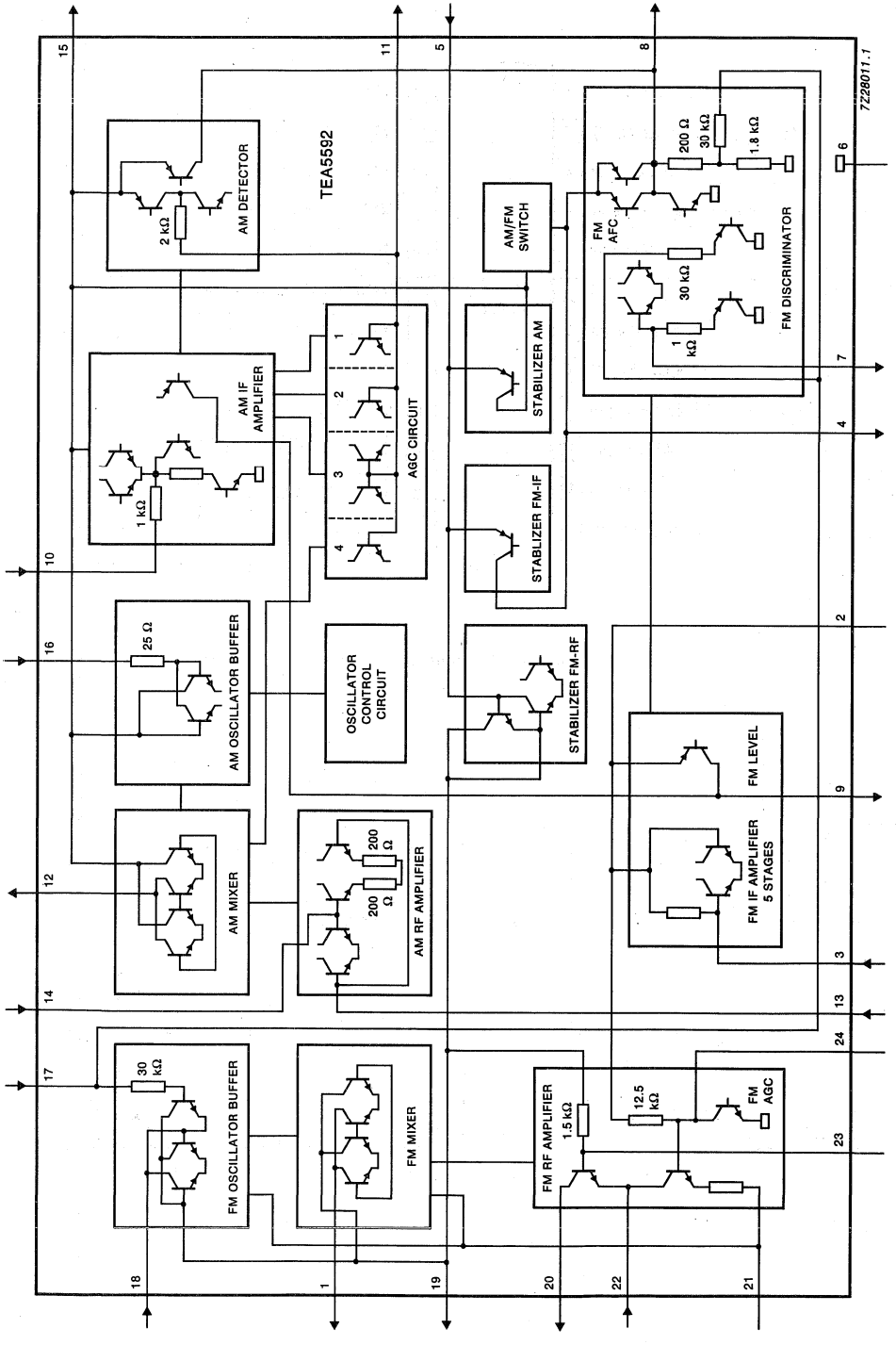


Fig.2 Equivalent circuit diagram.

PINNING

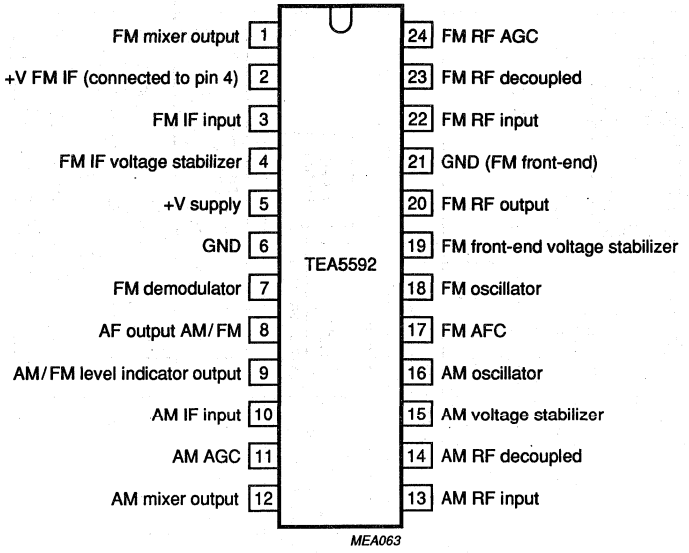


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 5)		V_P	–	15	V
Total power dissipation		P_{tot}	see Fig.3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−40	+85	°C
Electrostatic handling *		V_{es}	−2000	+2000	V

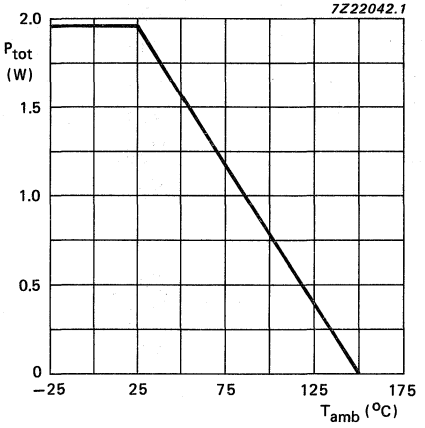


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 6 and pin 21; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 2		V_2	–	2.4	–	V
Pin 4		V_4	–	2.4	–	V
Pin 7		V_7	–	1.15	–	V
Pin 8		V_8	–	1.15	–	V
Pin 17		V_{17}	–	0.8	–	V
Pin 19		V_{19}	–	1.6	–	V
Pin 22		V_{22}	–	0.9	–	V
Pin 23		V_{23}	–	1.6	–	V
Pin 24		V_{24}	–	1.0	–	V
Voltages (AM)						
Pin 8		V_8	–	0.2	–	V
Pin 10		V_{10}	–	0.8	–	V
Pins 13 and 14		V_{13}, V_{14}	–	1.1	–	V
Pin 15		V_{15}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	19	mA
FM part		I_P	–	17	23	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.11) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM section						
AM front end (pin 13 to 12)	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 11) = V_{15} - 0.1 V	S_C	9.1	11.5	14	mA/V
	$V_{AGC} = V_{15}$ - 0.45 V	S_C	0.78	1.1	1.39	mA/V
IF suppression	note 2; V_o = 10 mV	α	20	30	–	dB
Oscillator (pin 16)						
Voltage	f = 1.5 MHz	V_{osc}	110	160	200	mV
	f = 1.5 MHz; V_P = 2.25 V	V_{osc}	60	–	–	mV
IF and detector section (pin 10 to 8)	note 3					
IF sensitivity;						
AF output voltage	no AGC; $V_{i(IF)}$ = 70 μV	V_o	27	40	55	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 70 μV	S+N/N	20	26	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	40	55	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	–	1	3	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	95	mV
	$V_{i(IF)}$ = 200 μV	V_9	–	200	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	450	600	mV
Overall performance (pin 13 to 8)	note 4					
Total harmonic distortion	V_i = 50 mV	THD	–	1.5	4	%

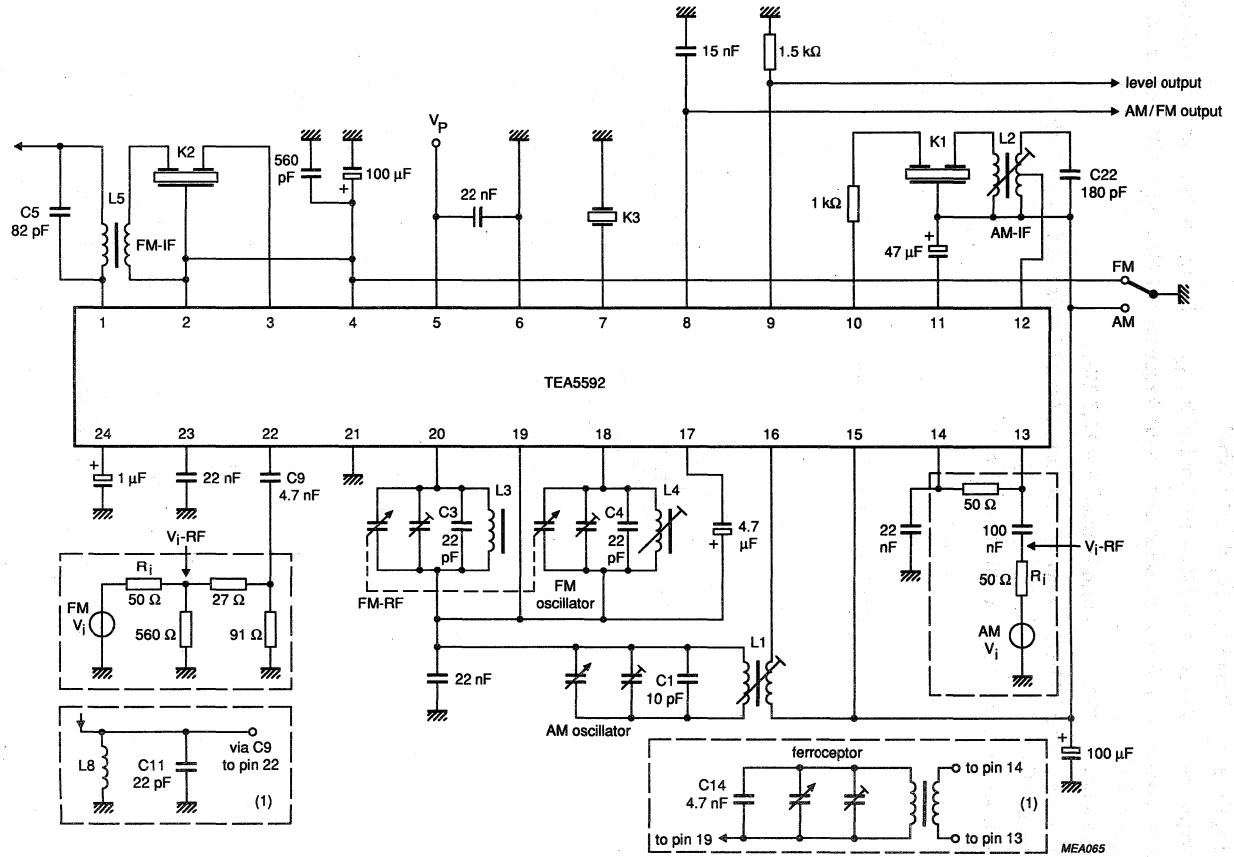
parameter	conditions	symbol	min.	typ.	max.	unit
FM section						
FM front end (pin 22 to 1)	note 5					
Conversion transconductance	V_i = 1 mV; V_{AGC} (pin 24) = 1.1 V	S_c	9	14	19	mA/V
	V_i = 1 mV; V_{AGC} (pin 24) = 0.8 V	S_c	4	8	10	mA/V
Oscillator (pin 18)						
Voltage	V_{AFC} = 0.8 V	V_{osc}	–	–	310	mV
	V_{AFC} = 0.8 V; V_P = 2.25 V	V_{osc}	95	200	–	mV
AFC control; change in oscillator frequency	V_{AFC} (pin 17) = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = −0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	−620	–	kHz
IF and demodulator section (pin 3 to 8)	note 6					
IF sensitivity;	note 7					
AF output voltage	$V_{i(IF)}$ = 70 μV	V_o	−3	−1	0	dB
Signal + noise-to-noise ratio for an IF input	$V_{i(IF)}$ = 70 μV no limiting	S + N/N	20	30	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	80	110	130	mV
Total harmonic distortion	Δf = 75 kHz; $V_{i(IF)}$ = 50 mV	THD	–	1	–	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	20	mV
	$V_{i(IF)}$ = 500 μV	V_9	–	260	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	550	670	mV

DEVELOPMENT DATA

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz.
2. α = 20 log (V_i at f_i = 468 kHz) / (V_i at f_i = 1 MHz).
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

APPLICATION AND TEST INFORMATION



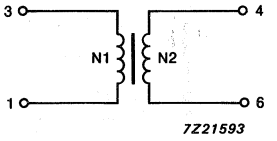
(1) In application the input circuits can be replaced by ferroceptor and aerial input circuit.

Fig. 5 Application circuit.

APPLICATION AND TEST INFORMATION (continued)

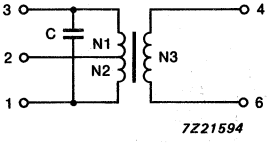
Component data

COILS



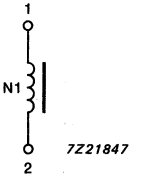
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type TOKO 7BRS

Fig.6 AM oscillator coil (L1).



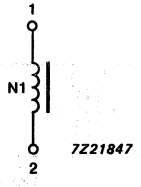
N1 = 135
N2 = 13
N3 = 5
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MCS

Fig.7 AM-IF coil (L2).



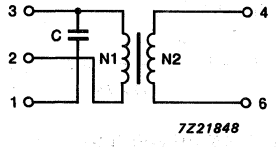
N1 = 2.5
L = 0.066 μH

Fig.8 FM-RF coil (L3). TOKO equivalent no. 301SN-0200.



N1 = 1.5
L = 0.04 μH

Fig.9 FM oscillator coil (L4). TOKO equivalent no 301SN-0100.



N1 = 11
N2 = 2
C = 82 pF (internal)
f_o = 10.7 MHz

Fig.10 FM-IF coil (L5). TOKO equivalent no. 301-20N

CERAMIC FILTERS

AM-IF (K1). SFU468B.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1.

TUNING CAPACITORS

AM section – 140/82 pF
FM section – 2 x 20 pF

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

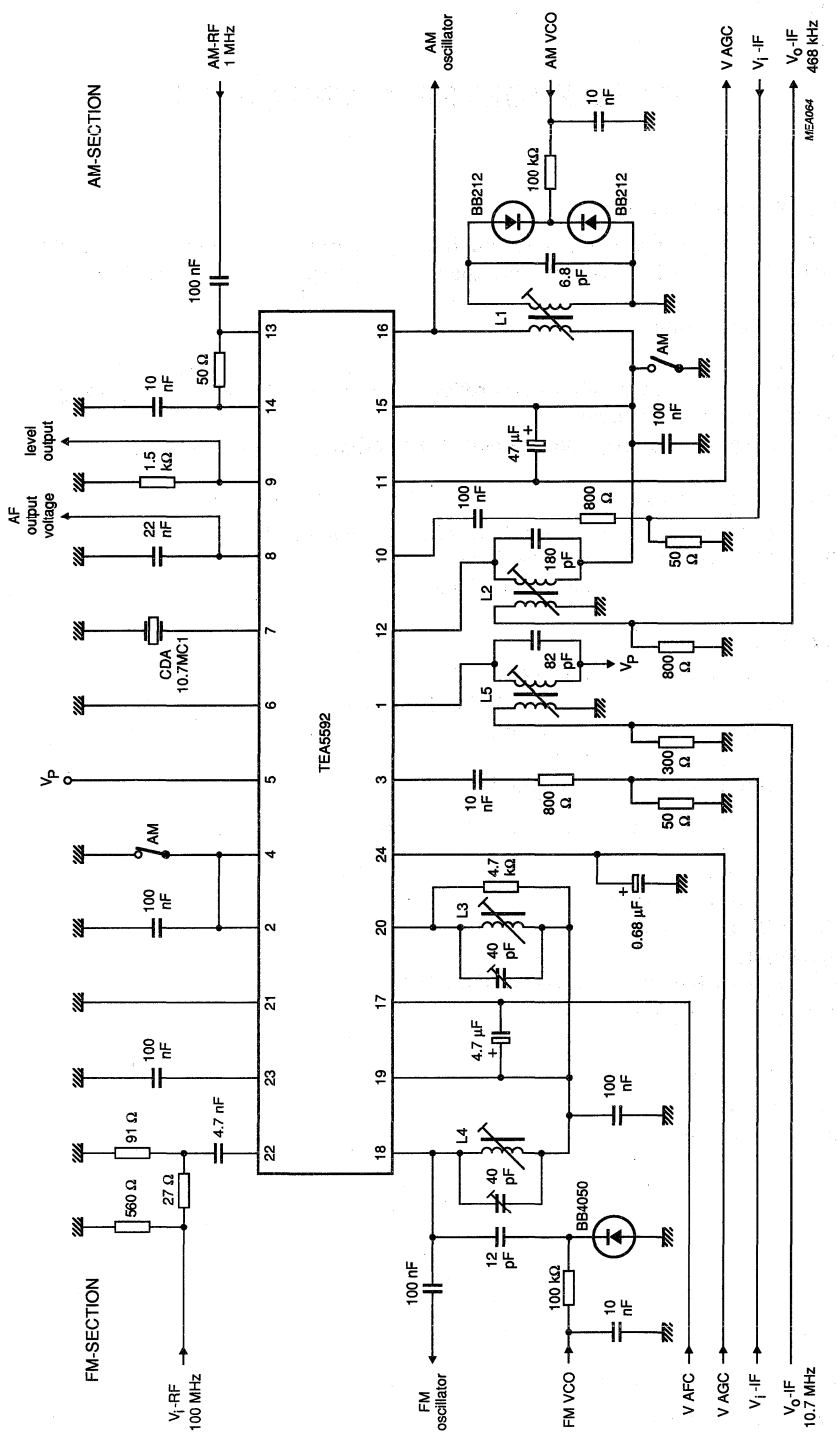


Fig.11 Factory test circuit.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5594 is a 32-pin integrated radio circuit designed for use in all Electronic Tuned Radio (ETR) sets especially those sets which have to fulfil the immunity requirements of CENELEC.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the LW/MW frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (fulfilling the "out of band" CENELEC requirements)
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator with a ceramic filter

The TEA5594 also contains:

- Oscillator output buffers for AM and FM
- A combined AM/FM IF counter output buffer with counter "enable" function
- A field strength level detector for AM and FM
- A soft mute circuit at FM, adjustable
- An extra IF amplifier to split up IF filtering

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Supply voltages 2.7 to 15 V
- A local distance switch facility (LOCAL-DX) at FM
- All pins are ESD protected

PACKAGE OUTLINE

32-lead shrink DIL; plastic (SOT232).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	24	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+85	°C
AM performance (pin 22)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S+N)/N = 26 dB	V_i	–	16	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 30)	note 2					
Limiting sensitivity	−3 dB; note 3	V_i	–	2.5	–	μV
Signal-to-noise ratio	V_i = 3 μV	(S+N)/N	–	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	50	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
3. Soft mute switched off.

DEVELOPMENT DATA

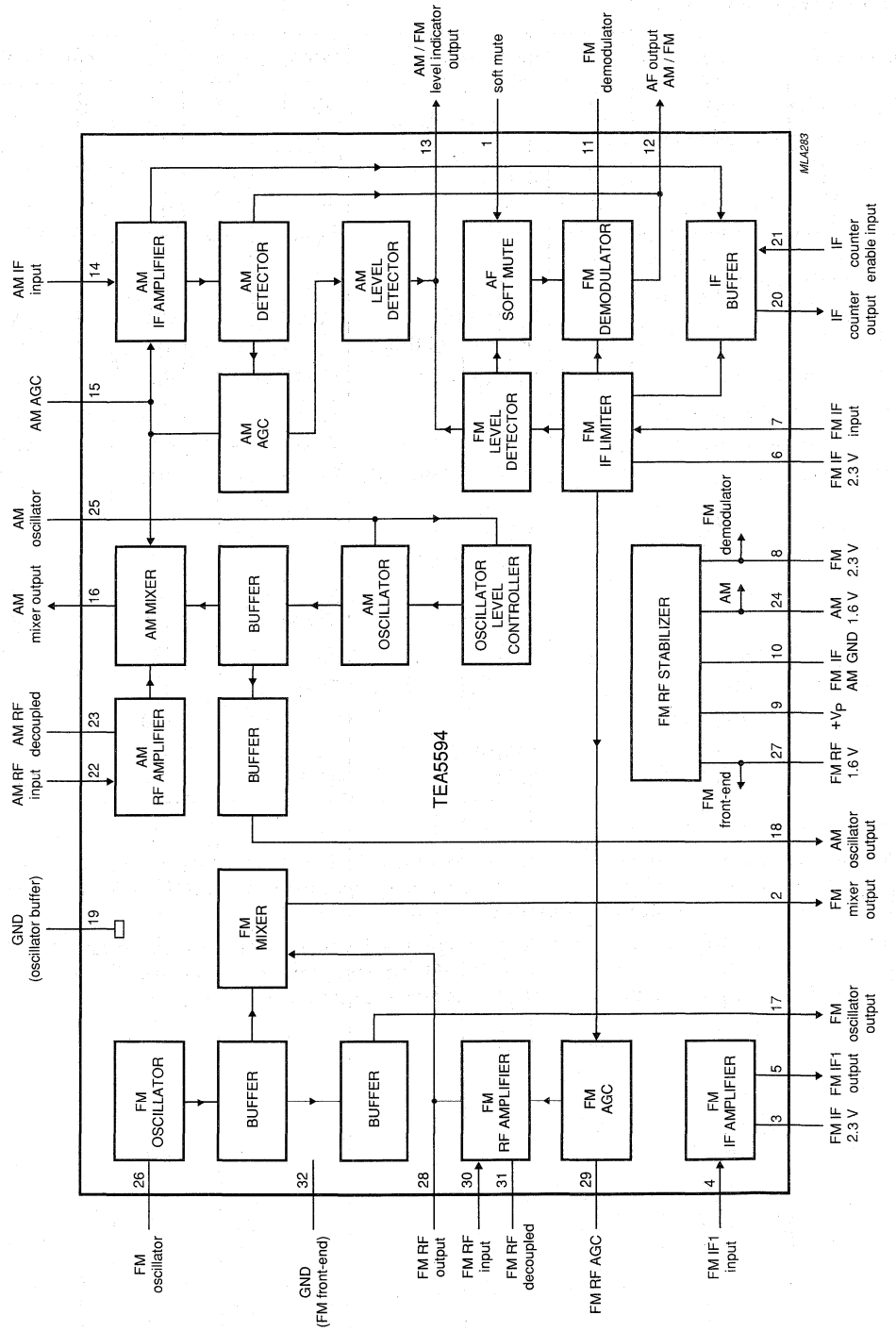


Fig.1 Block diagram.

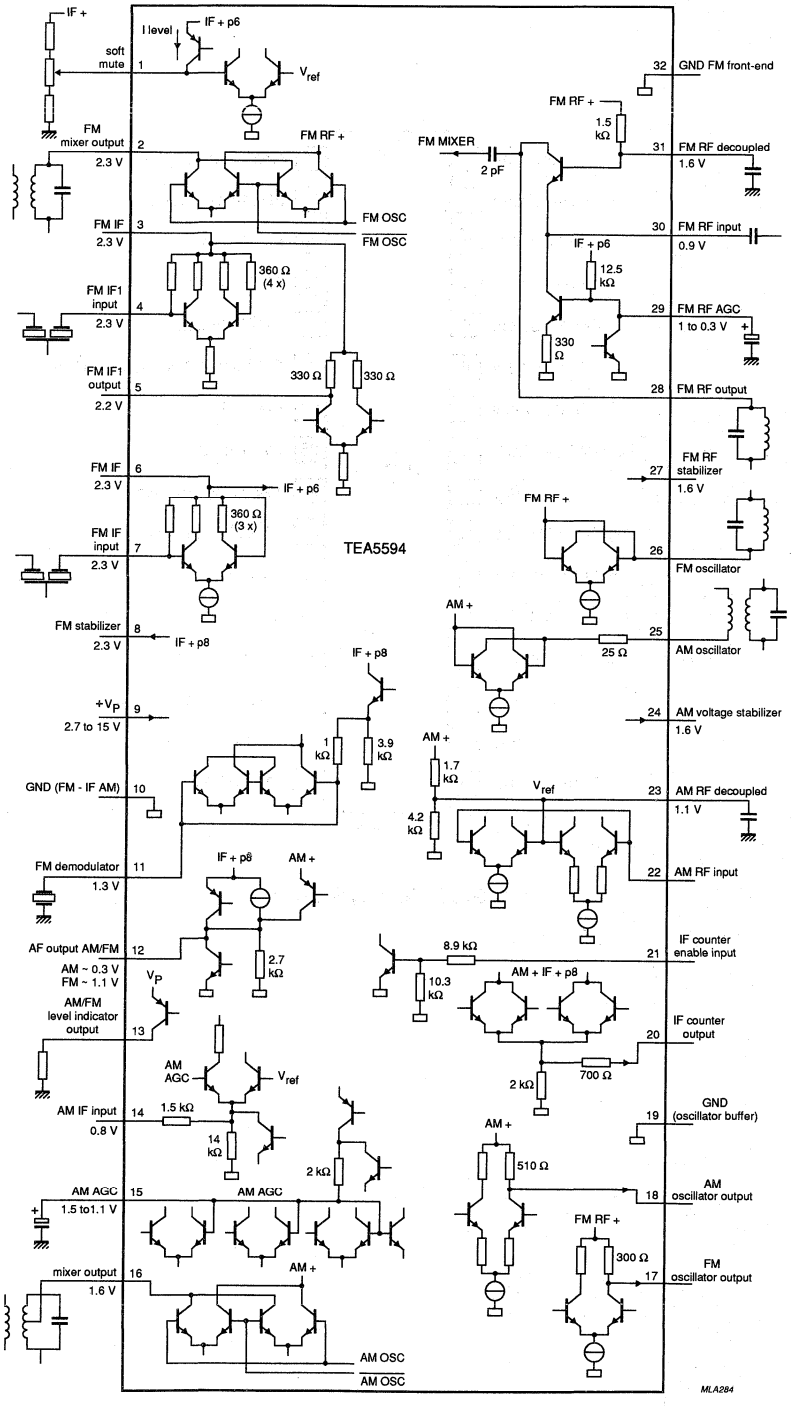


Fig.2 Equivalent circuit diagram.

PINNING

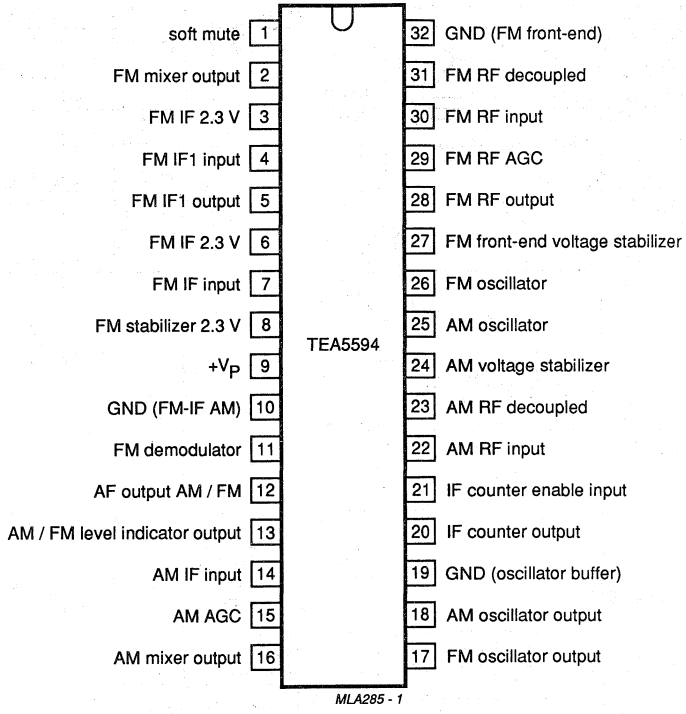


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 9)		V_P	–	18	V
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Electrostatic handling*		V_{es}	−2000	+ 2000	V

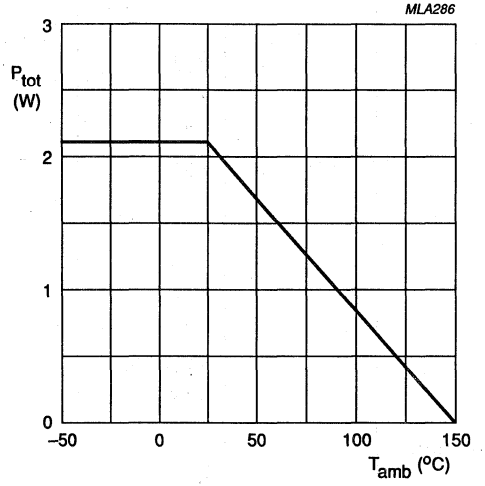


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 10, pin 19 and pin 32; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage V_P = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 4		V_4	–	2.3	–	V
Pin 5		V_5	–	2.2	–	V
Pin 7		V_7	–	2.3	–	V
Pin 8		V_8	–	2.3	–	V
Pin 12		V_{12}	–	1.15	–	V
Pin 27		V_{27}	–	1.6	–	V
Pin 29		V_{29}	–	1.0	–	V
Pin 30		V_{30}	–	0.9	–	V
Pin 31		V_{31}	–	1.6	–	V
Voltages (AM)						
Pin 12		V_{12}	–	0.2	–	V
Pin 14		V_{14}	–	0.8	–	V
Pin 15		V_{15}	–	1.54	–	V
Pins 22 and 23		V_{22}, V_{23}	–	1.1	–	V
Pin 24		V_{24}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	*	mA
FM part		I_P	–	24	*	mA

DEVELOPMENT DATA

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.6) at nominal supply voltage V_P = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
AM SECTION						
AM front end	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 15) = V_{24} - 0.1 V	S_C	*	13.5	*	mA/V
	$V_{AGC} = V_{24}$ - 0.45 V	S_C	*	1.2	*	mA/V
IF suppression	note 2	α	20	30	–	dB
Oscillator (pin 25)						
Voltage	f = 1.5 MHz	V_{osc}	–	160	*	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{18}	*	140	–	mV
IF and detector part	note 3					
IF sensitivity; AF output voltage	no AGC; $V_{i(IF)}$ = 90 μV	V_o	30	40	60	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 90 μV	S+N/N	22	24	30	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	35	50	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	0.75	2	5	%
	$V_{i(IF)}$ = * to * mV; m = 30%	THD	–	*	–	%
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	560	*	mV
	$V_{i(IF)}$ = 200 μV	V_{13}	*	3200	*	mV
	$V_{i(IF)}$ = 10 mV	V_{13}	*	6600	*	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
AM IF counter output buffer						
Counter "enable"						
Output voltage (peak-to-peak value)		V_{20}	100	125	–	mV
Counter "disable"						
Suppression of 468 kHz		V_{20}	–40	–	–	dB
Overall performance	note 4					
Total harmonic distortion	$V_{i(RF)}$ = 50 mV	THD	–	–	8	%
Signal handling	THD = * %; m = 0.8%		–	*	–	
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
FM SECTION						
FM front end	note 5					
Conversion transconductance	$V_{i(RF)}$ = 1 mV; V_{AGC} = 1.1 V	S_c	16	24	32	mA/V
	$V_{i(RF)}$ = 1 mV; V_{AGC} = 0.8 V	S_c	5	10	15	mA/V
Oscillator (pin 26)						
Voltage		V_{osc}	–	250	–	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{17}	*	270	–	mV
IF and demodulator part	note 6					
IF sensitivity	note 7					
AF output voltage	$V_{i(IF)}$ = 40 μV no mute	V_o	–3	–1	0	dB
	with mute	V_o	–20	–30	–40	dB
AM suppression	note 8	α	–	*	–	dB
Signal + noise-to-noise ratio for an IF input	no mute; $V_{i(IF)}$ = 40 μV	S+N/N	28	46	50	dB
	$V_{i(IF)}$ = 1 mV	S+N/N	–	*	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	*	85	*	mV
Total harmonic distortion	$V_{i(IF)}$ = 50 mV Δf = 75 kHz	THD	–	1	–	%
	Δf = 22.5 kHz	THD	–	*	–	%

* Value to be fixed.

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	2600	*	mV
	$V_{i(IF)}$ = 50 μV	V_{13}	*	5750	*	mV
	$V_{i(IF)}$ = 1 mV	V_{13}	*	6250	*	mV
AM/FM IF counter output buffer						
Counter "enable"	note 5					
Output voltage (peak-to-peak value)		V_{20}	–	130	–	mV
Counter "disable"						
Suppression of 10.7 MHz		V_{20}	–40	–	–	dB
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
AM/FM switch						
FM OFF/AM ON		$V_{8\text{-}10}$	–	0	0	V
FM ON/AM OFF		$V_{24\text{-}10}$	–	0	0	V

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N2/N3}{R}$ (see TR2 Component data)
   Where R = 1.2 kΩ (total impedance at pin 16).
2. α = 20 log (V_i at f_i = 468 kHz)/(V_i at f_i = 1 MHz); V_o = 10 mV; no AGC.
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; R_{source} = 800 Ω unless otherwise specified.
4. Front-end connected to IF plus detector part (see Fig.5). Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N1/N2}{R}$ (see TR3 Component data)
   Where R = 6.6 kΩ (total impedance at pin 2).
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at $V_{i(IF)}$ = 1 mV;
   No mute : $V_1 = V_8$;
   With mute : V_1 = 0 V.
8. AM suppression is measured with AM only: m = 0.8% and f_{mod} = 1 kHz referred to AF output at FM only: Δf = 75 kHz and f_{mod} = 1 kHz.

* Value to be fixed.

APPLICATION AND TEST INFORMATION

For coil information see Component data.

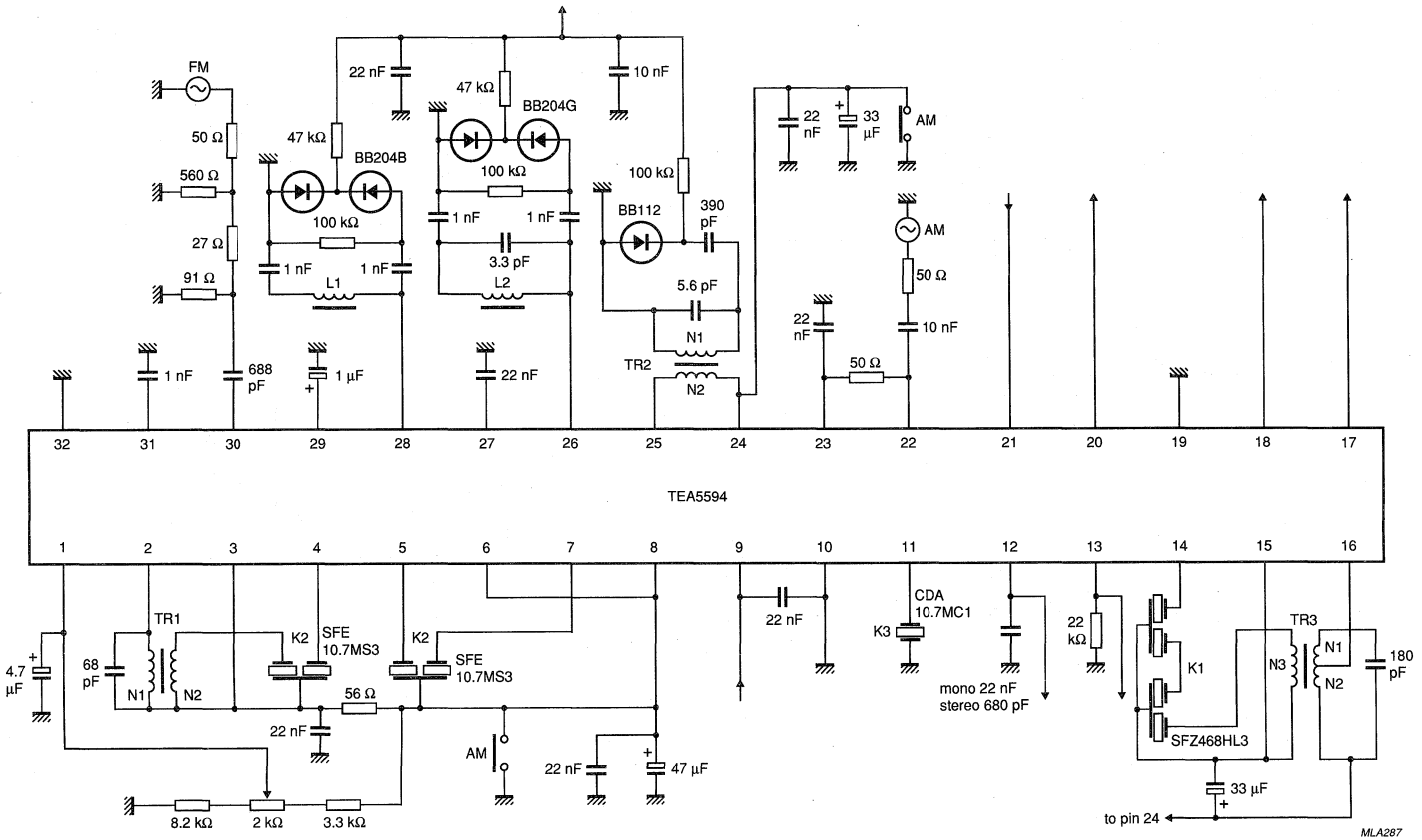


Fig.5 Application circuit for evaluation.

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

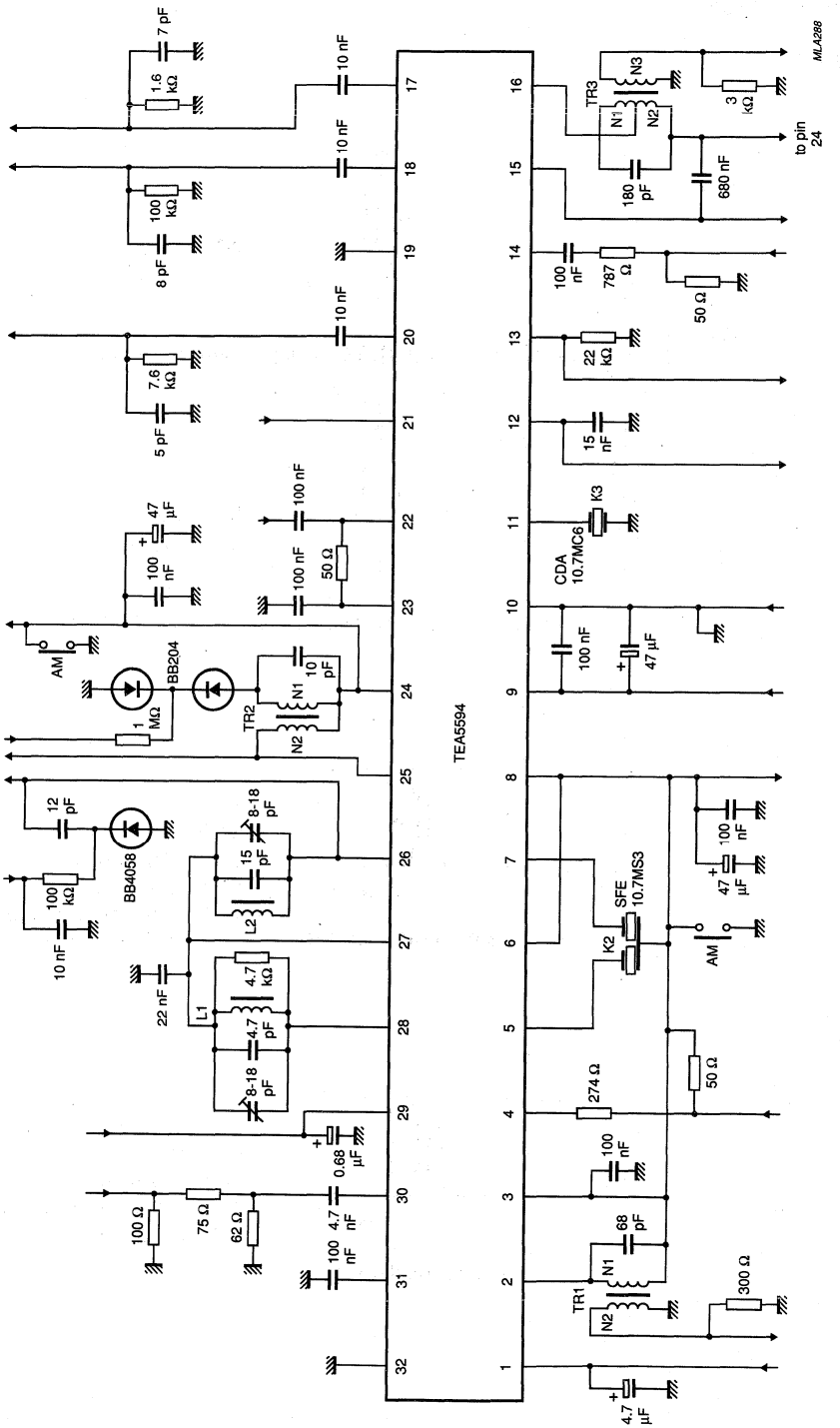
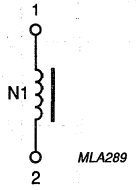


Fig.6 Factory test circuit.

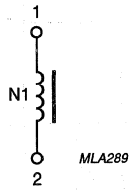
Component data

COILS



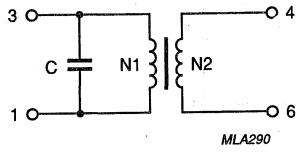
N1 = 4.5
L = 100 μH

Fig.7 FM-RF coil (L1). TOKO equivalent no. MC115.



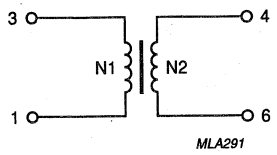
N1 = 4.5
L = 94 μH

Fig.8 FM oscillator coil (L2). TOKO equivalent no. A294SNS-1004NK.



N1 = 12
N2 = 2
C = 68 pF (internal)
f_o = 10.7 MHz
Wire = 0.07 mm diameter
Coil type TOKO 119BCS-A6515BQG

Fig.9 FM-IF coil (TR1).

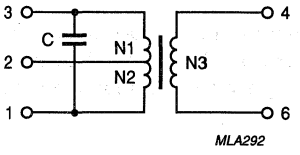


N1 = 55
N2 = 55
Lprim = 106 μH
Wire = 0.05 mm diameter
Coil type TOKO 7MCS

Fig.10 AM oscillator coil (TR2).

Component data (continued)

COILS



N1 = 139
N2 = 15
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MC

Fig.11 AM-IF coil (TR3).

CERAMIC FILTERS

AM-IF (K1). SFZ468HL3.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1 (MC6).

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I^2C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

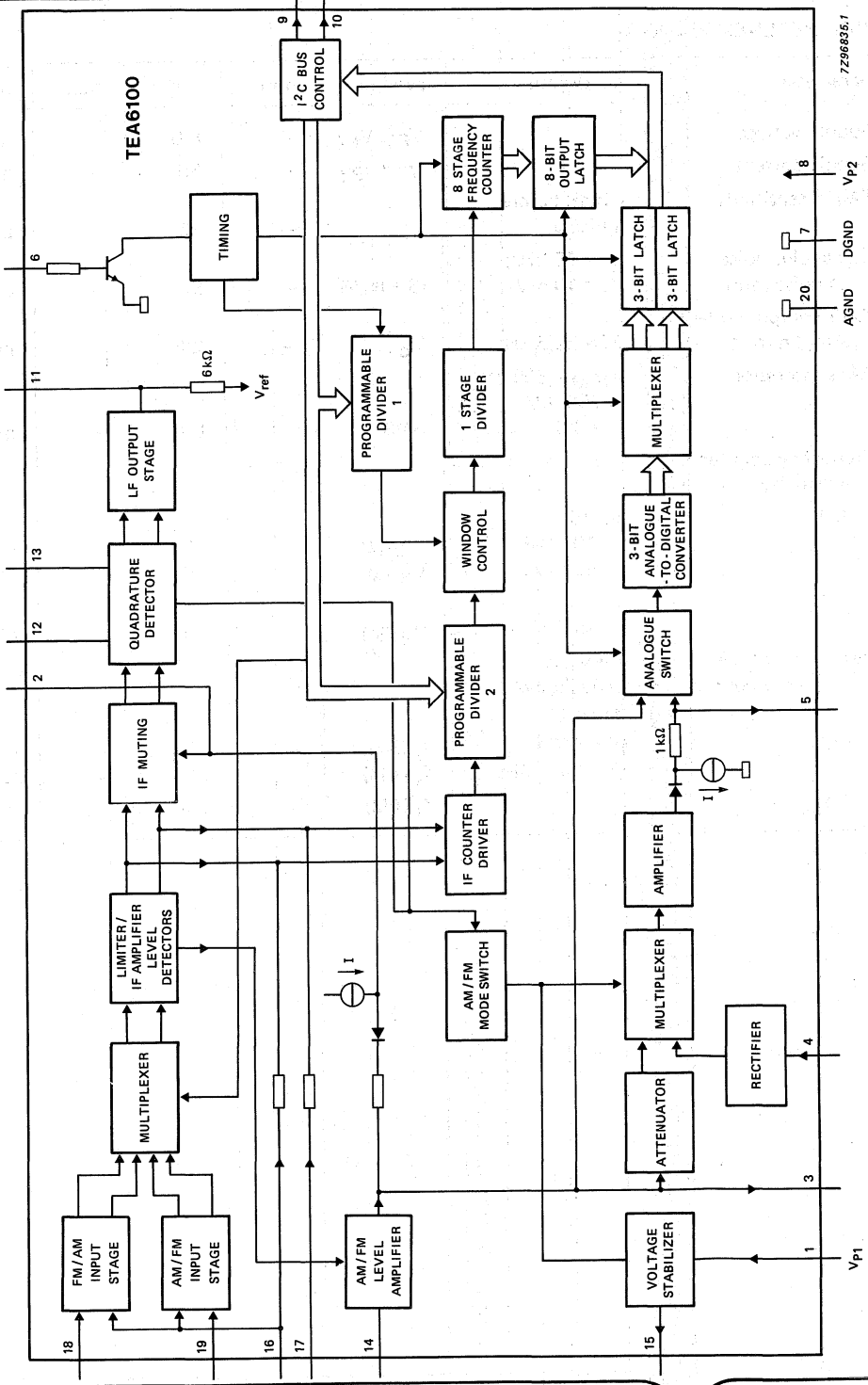


Fig. 1 Block diagram.

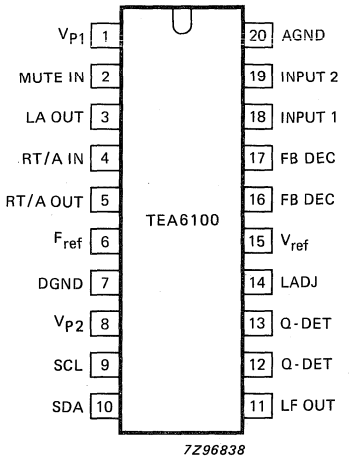


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the –3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

word	position	
	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '–3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

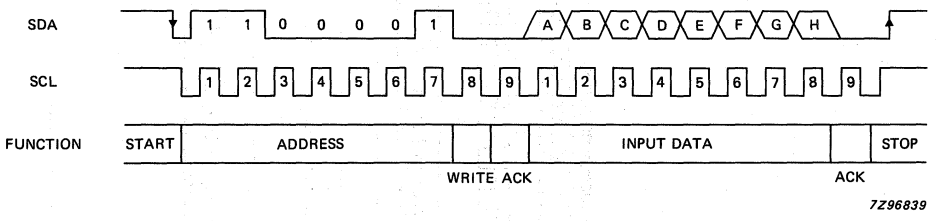


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

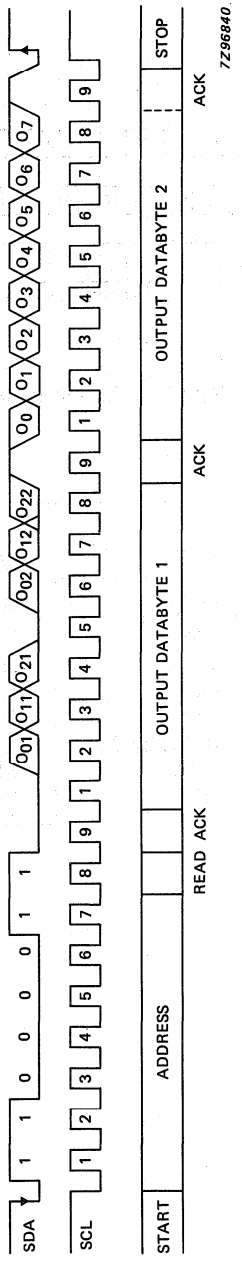


Fig. 4 Output data format waveforms.

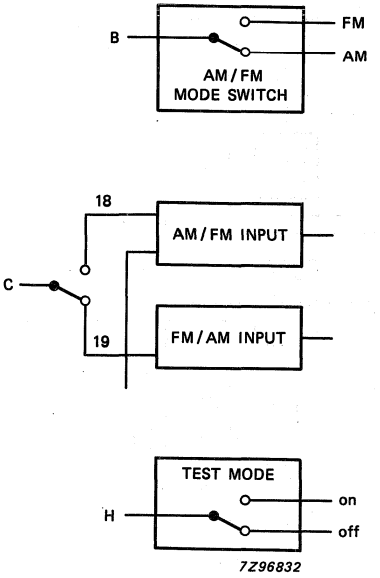


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

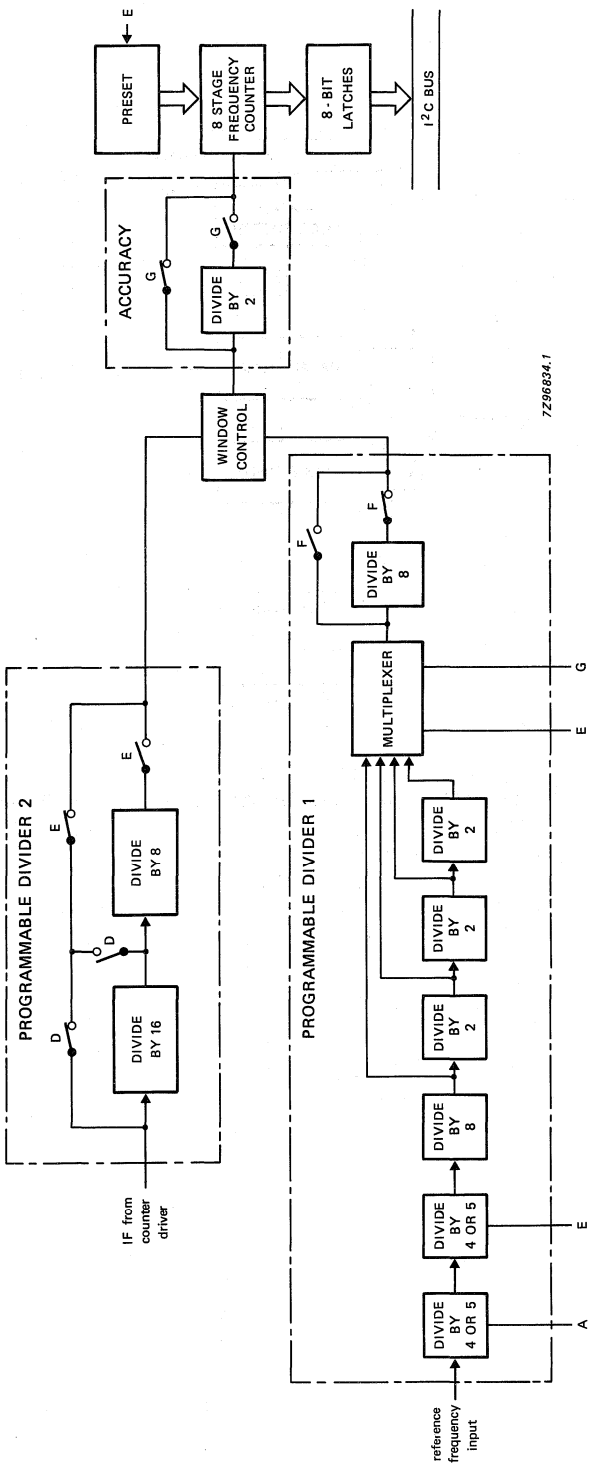


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

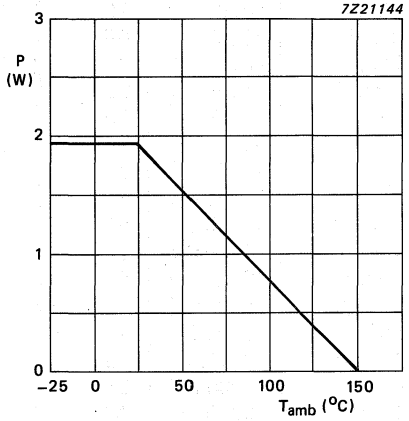


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8; $V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec*
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\|Z_o\|$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec*
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

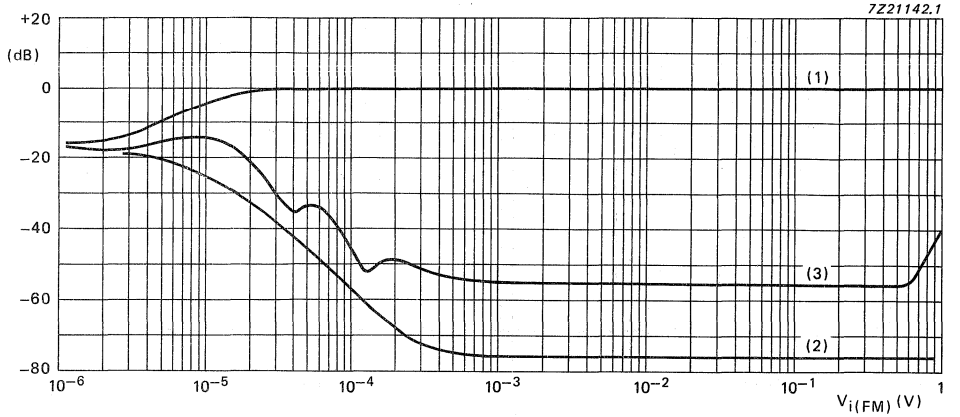
* V/dec = voltage per decade.

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I^2C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

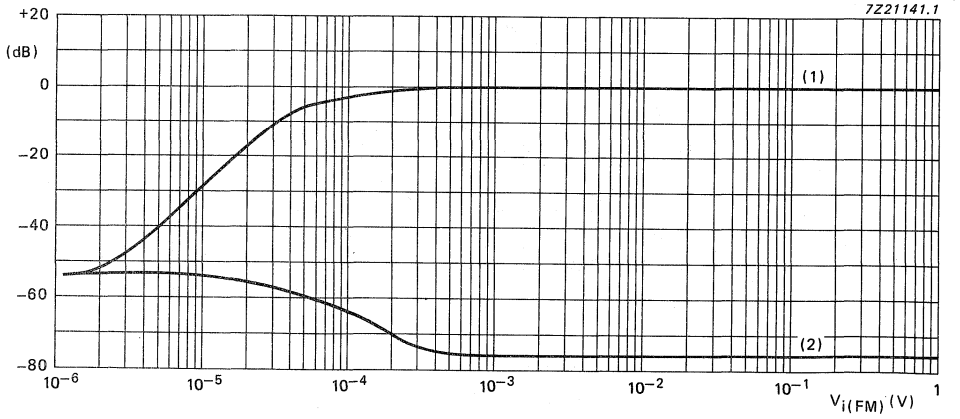
Notes to the characteristics

1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

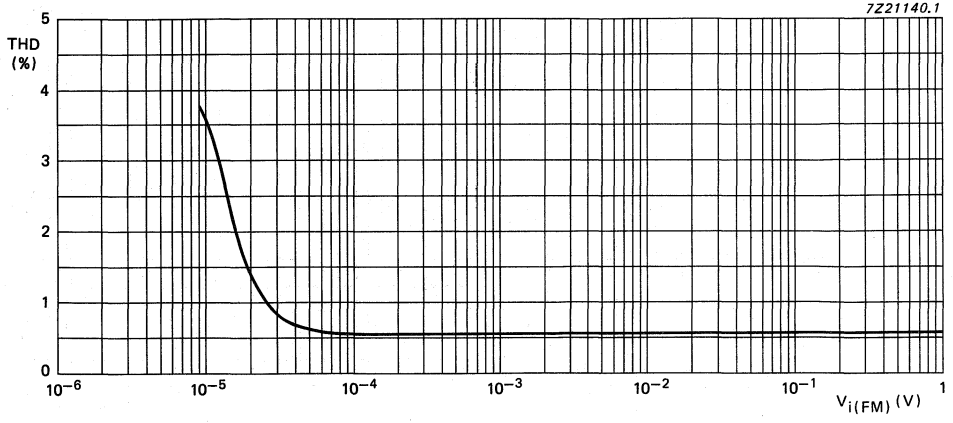
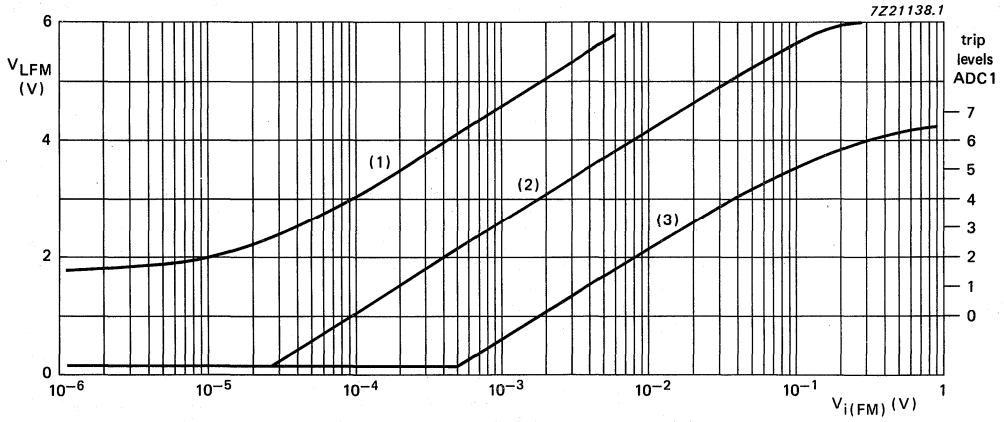
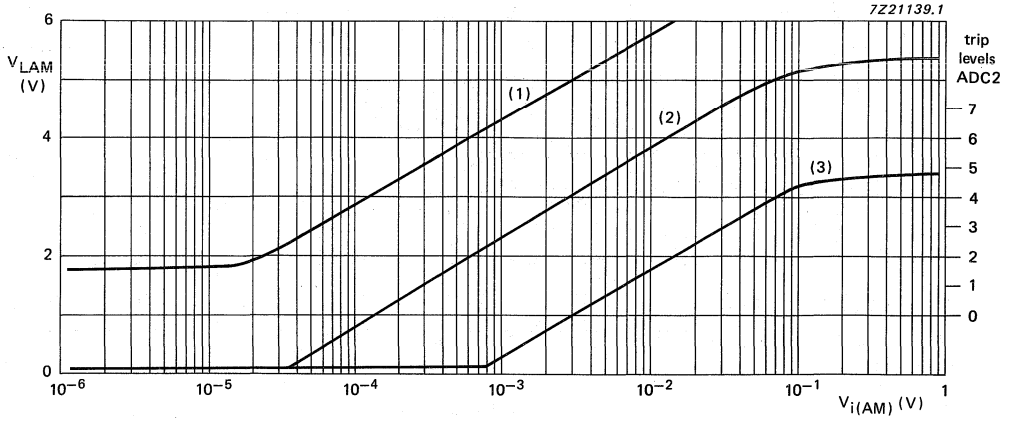


Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

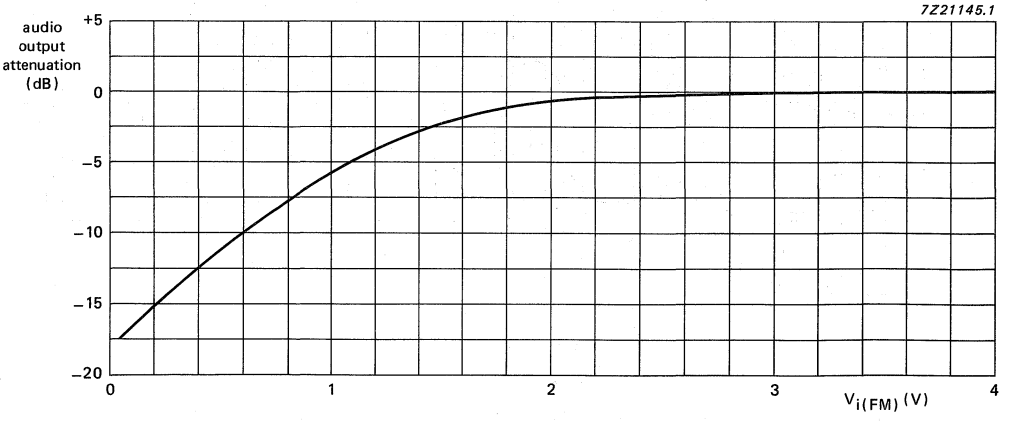
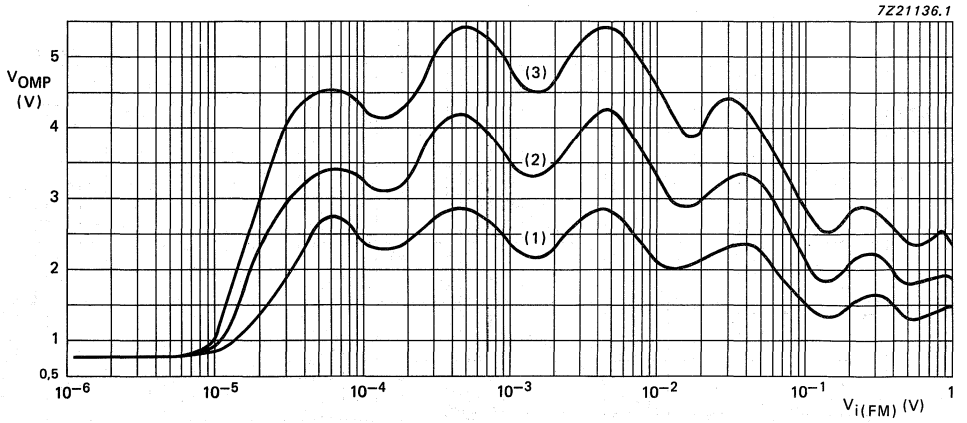
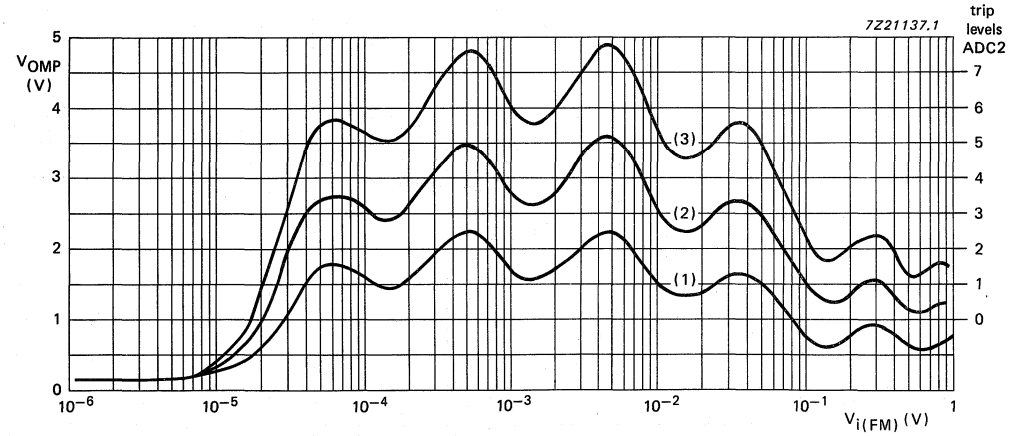


Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

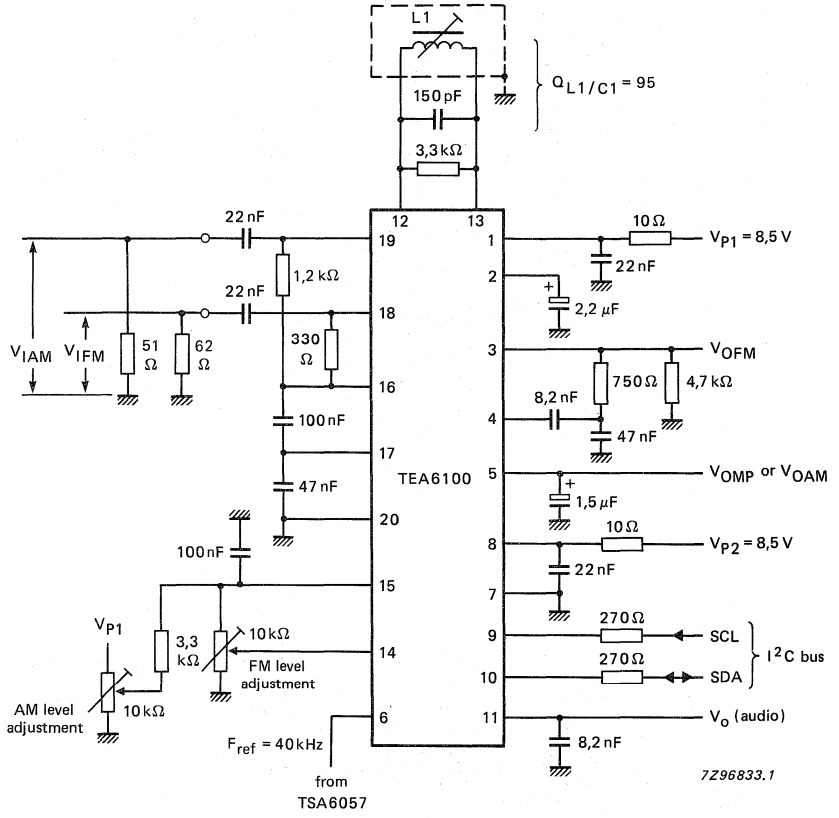


Fig. 13 Application diagram.

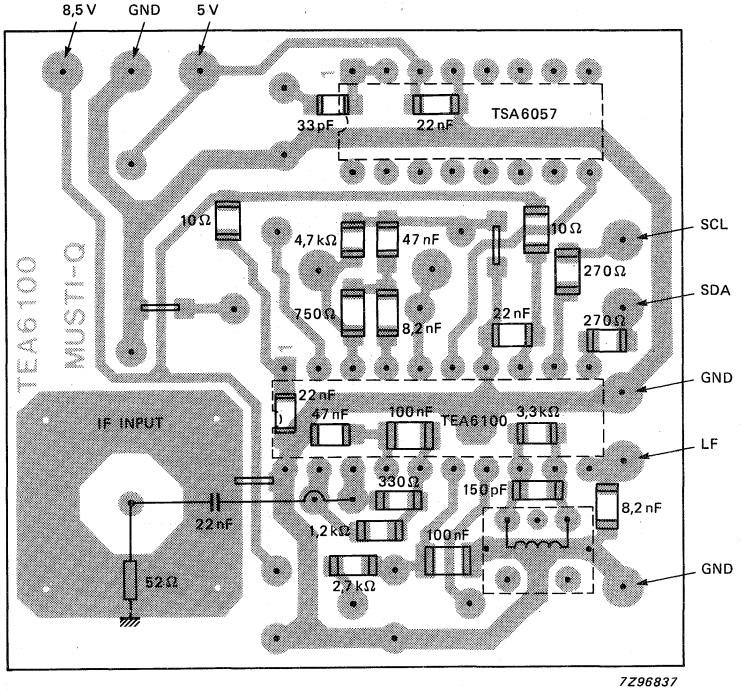


Fig. 14 Track side of printed circuit board.

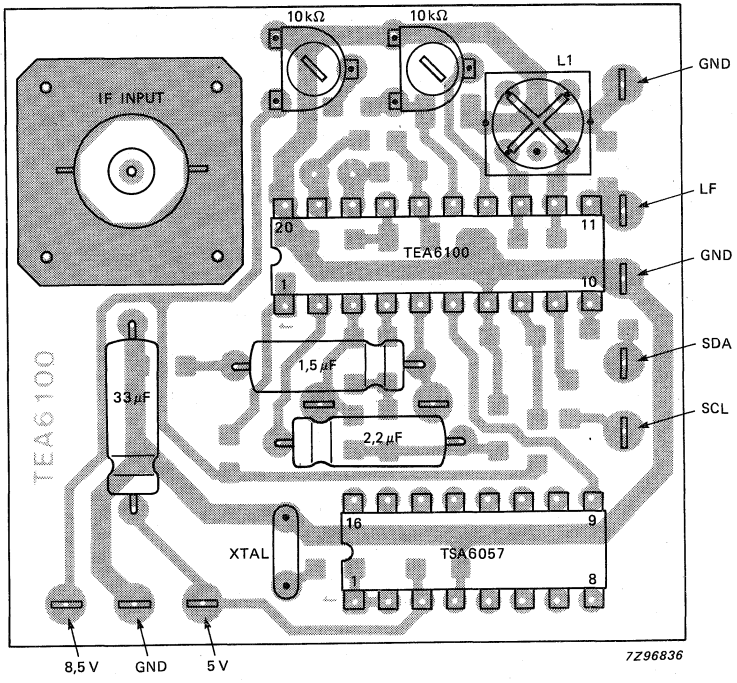
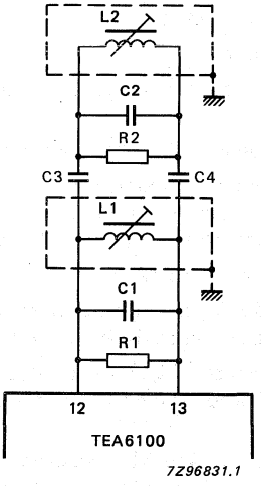


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

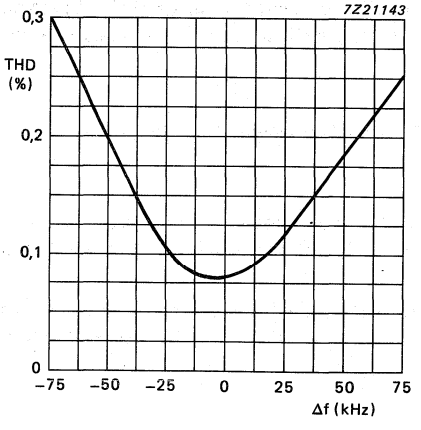


Fig. 17 Total harmonic distortion plotted against IF detuning; for Δf = ± 75 kHz, f_{mod} = 1 kHz and V_O = 500 mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and –3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x $(2^{[E \times 2 + G \times 1]})$ x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_I) = (TIFF) + R x (MHEX – THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF – $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

$N1 = (0 \times 4 + 1 \times 5) \times (0 \times 4 + 1 \times 5) \times 8 \times (2^{[1 \times 2 + 0 \times 1]}) \times (1 \times 1 + 0 \times 8) = 800$

$T = 800/40 = 20$ ms

$N2 = (1 \times 16 \times 8 + 0 \times [1 \times 1 + 0 \times 16]) \times (0 \times 2 + 1 \times 1) = 128$

$TDEC = 20 \times 10,7/128 + (1 \times 247 + 0 \times 79) = 1919$

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

$R = 128/20 = 6400$ Hz/count

Assume the readout is '6E', the measured frequency will be:

- $F_I = 10,7 + (6E - 7F) \times 6400 = 10,59$ MHz

Assume the readout is '83', the measured frequency will be:

- $F_I = 10,7 + (83 - 7F) \times 6400 = 10,726$

Antenna diversity circuit TEA6101/T

FEATURES

- Ability to switch between up to four antennae
- Switching signal derived from two signals: the audio and the level signals
- Floating switching threshold adjusts switching rate to prevailing circumstances:
  - increasing threshold due to excessive noise
  - increasing threshold due to numerous level variations
- Memory for the most favourable antenna signal to overcome unnecessary switching
- Signal-dependent "soft" muting circuit
- Mode selection to the first antenna receiving an AM signal whilst the diversity system is reset.

GENERAL DESCRIPTION

Intended for multi-antenna FM car radio reception (antenna diversity system), the TEA6101/T selects the most favourable signal from one of up to four antennae. Founded upon audible signal disturbance the criteria are derived from two signals: high frequency components (e.g. spikes due to noise and multipath reception) and variations in signal level as a result of multipath reception or fluctuations in field strength.

APPLICATIONS

- Car radio receivers
- Mobile radio communications equipment

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	–	8.5	–	V
I_P	positive supply current	–	14	–	mA
$V_{I(p-p)}$	audio input voltage (peak-to-peak value)	–	–	3	V
I_{os}	antenna switch output current (source/sink)	–	–	7	mA
V_L	–3 dB audio attenuation (soft mute)	–	1.45	–	V
T_{amb}	operating ambient temperature range	–30	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6101	18	DIL	plastic	SOT102
TEA6101T	20	SO	plastic	SOT163A

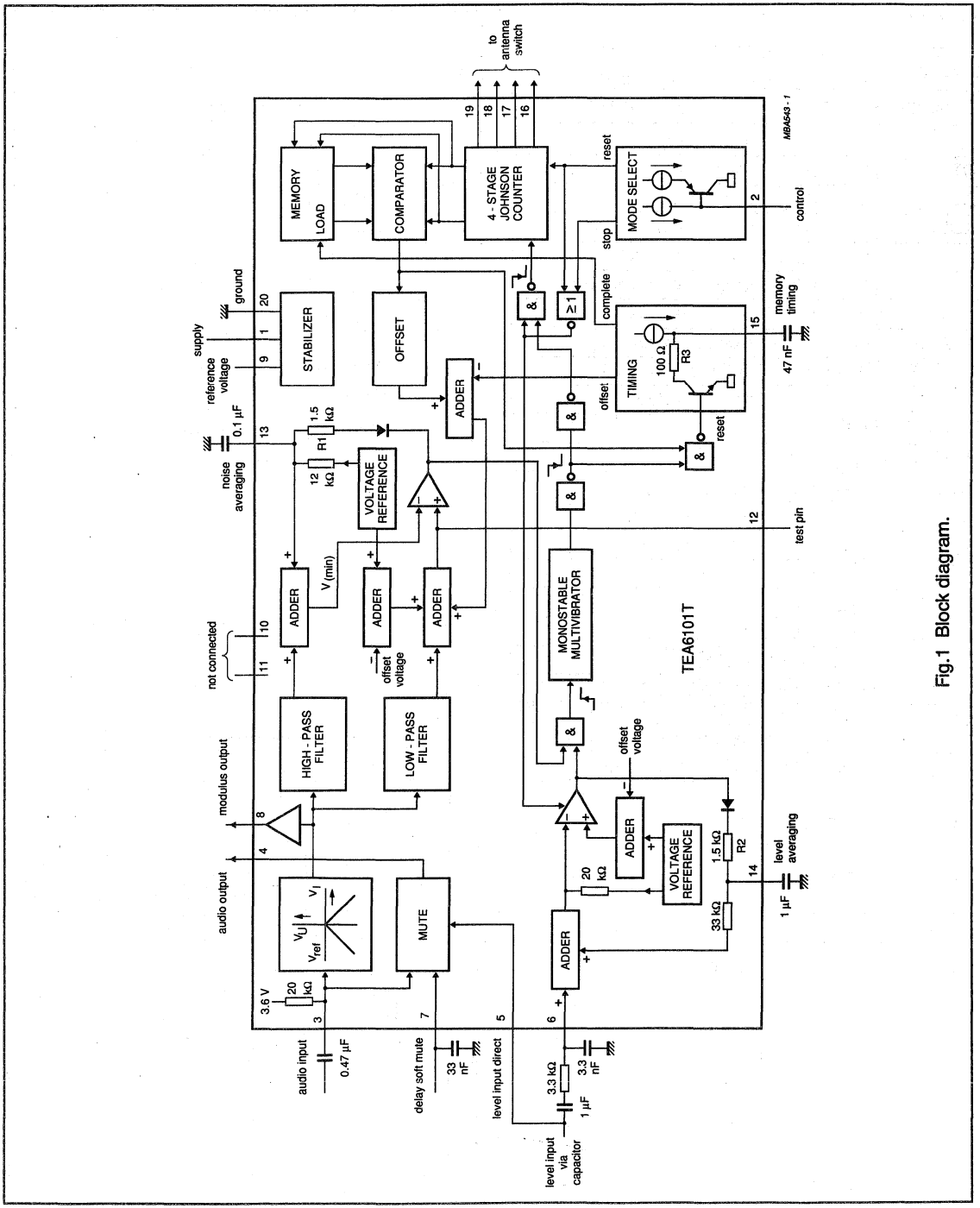


Fig.1 Block diagram.

PINNING

The pin numbers given in parenthesis refer to the TEA6101

SYMBOL	PIN		DESCRIPTION
V_P	1	(1)	positive supply
CTRL	2	(2)	control input
AUDIN	3	(3)	audio input
AUDOUT	4	(4)	audio output
LID	5	(5)	level input direct
LIC	6	(6)	level input via capacitor
DSM	7	(7)	delay soft mute
MODOUT	8	(8)	modulus output
V_{ref}	9	(9)	reference voltage
n.c.	10	–	not connected
n.c.	11	–	not connected
TEST	12	(10)	test pin
NOAV	13	(11)	noise averaging
LEAV	14	(12)	level averaging
MT	15	(13)	memory timing
OUT4	16	(14)	output 4
OUT3	17	(15)	output 3
OUT2	18	(16)	output 2
OUT1	19	(17)	output 1
GND	20	(18)	ground

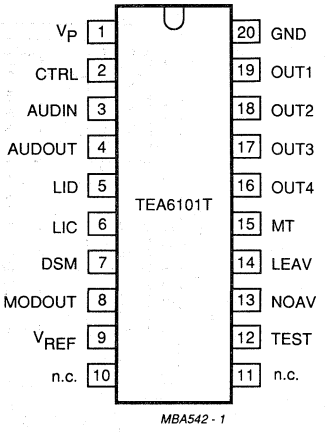


Fig.2 Pin configuration (TEA6101T).

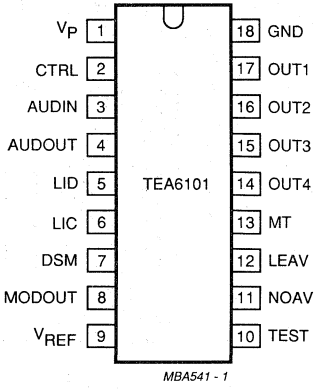


Fig.3 Pin configuration (TEA6101).

FUNCTIONAL DESCRIPTION

Various forms of disturbance can affect signal reception in car radio receivers:

- ignition interference produces spikes on the audio signal. Switching to another antenna will be ineffective. Strong ignition interference, however, will modulate the antenna field strength. In this instance another antenna possessing a directional pattern will suffer less disturbance and switching would be appropriate.
- variation of antenna field strength due to travelling through a zone of variable signal strength will result in a variation in the signal level. Greater noise will be apparent on the audio signal whilst the IF limiter is not limiting. Switching to an alternative antenna input would increase the signal strength.
- multipath reception occurs when a signal reaches the antenna from two or more directions. Often the signals will be of different phase. In certain circumstances the sum of the reflected signals results in zero and a large spike will be evident on the audio signal. It will then be necessary to switch to an alternative antenna from which the sum of the received signals will be different.

The criteria for an antenna diversity system are high frequency components (spikes and noise) on the audio signal in combination with variations in signal level.

Detection of spikes on the audio signal

A rectifier, high pass filter, low pass filter and a comparator are used to detect spikes and noise on the audio signal (see Fig.1). The negative spikes are detected by the rectifier whilst a high pass filter removes the audio signal to leave the high frequency signal components at the negative input to the comparator. The signal at the positive input to the comparator consists of an offset together with an audio signal attenuated by the low pass filter. If the amplitude of the spikes exceed that of the attenuated audio plus offset, the output of the comparator is HIGH.

When the switching rate of the comparator is HIGH, feedback increases the offset via the diode, the resistor R1, and the 100 nF capacitor. The offset is decreased by the 12 kΩ resistor and the 100 nF capacitor (pin 11 or 13). The result is an offset based upon the comparator switching rate, rapid to increase but slow to decrease, therefore permitting only the largest spikes to trigger the comparator (floating threshold).

Should high noise be apparent on the audio signal, the offset is decreased by means of the rectifier and high pass filter. This will result in more frequent switching to an alternative antenna whilst the result of the switching operation will be less audible.

Detection of voltage level variation

A 1 µF input capacitor and 20 kΩ resistor remove the absolute level voltage to leave only variations to be detected. The level comparator output is HIGH when the variations in level voltage are greater than the offset. Similarly to the audio comparator; the feedback diode, resistor R2, the 1 µF capacitor and the 33 kΩ resistor cause the threshold level to float. During periods of high activity the comparator thus switches only on the largest variations.

Switching to an alternative antenna

When both the level and the audio comparator outputs are HIGH, another output of the Johnson counter will be selected. Since switching to an alternative antenna would cause a disturbance of the audio and level signals the monostable multivibrator will prohibit the counter from selecting another antenna input for 21 µs.

Memory and timing

Approximately similar qualities of signal originating from different antennae could result in unnecessary antenna switching. This is prevented by appointing a priority antenna. The selection of an antenna without priority results in the audio offset being decreased by 1.2 V such that the audio comparator will have a HIGH output voltage. During the period of memory timing the offset increases towards the normal offset value. Should level alterations occur during this period another antenna will be selected. If, however, the memory is timed-out without the occurrence of signal variation, priority will be appointed to the selected antenna. Thus a priority antenna will be selected for the majority of the time during reception of almost all similarly weak antenna signals.

Mute

A mute function should not precede the circuit. This function is therefore assumed by the TEA6101. When used in combination with the TEA6100 the 20 kΩ input of the IF IC together with the 6 kΩ output resistor of the TEA6101 cause an attenuation of 3 dB. The mute circuit therefore has 3 dB amplification of level voltages in excess of 2.75 V.

Mode selection

The diversity system is intended for FM reception. To avoid an audible disturbance if it is used with an AM system, the circuit can be reset. In the reset mode antenna 1 (pin 17 (19)) is selected and both comparators are switched off to prevent pulses reaching the output.

For FM search tuning the diversity system may be similarly disabled. The selected antenna will again be retained with the comparators being inhibited.

Test pin

Although intended for test purposes the test pin can be used to increase the audio offset (resistor from pin 10 (12) to ground) or to change the compensation factor (resistor between pin 8 (8) and 10 (12)). These modifications permit the behaviour of the antenna switch to be adapted to alternative IF amplifier IC's.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	0	12	V
P_{tot}	total power dissipation	–	see Fig.3	
T_{amb}	operating ambient temperature range	–30	+85	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ c\text{-}a}$	from crystal to ambient (SOT102)	75 K/W
$R_{th\ c\text{-}a}$	from crystal to ambient (SOT163A)	150 K/W

DC CHARACTERISTICS

Measurements using application circuit (Fig 1) at T_{amb} = 25 °C and V_P = 8.5 V. Voltages with respect to pin 18 (20); pin numbers in parenthesis refer to TEA6101T; all currents positive into the IC unless otherwise specified.

SYMBOL	PARAMETER		CONDITION	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage			7.5	8.5	12	V
I_P	positive supply current		I_{SO} = 0 mA	–	14	–	mA
P_{tot}	total power dissipation			–	119	–	mW
V_{pins}	voltage at pin:						
	1	(1)		–	8.5	–	V
	2	(2)		–	7.8	–	V
	3	(3)		–	3.6	–	V
	4	(4)		–	5.4	–	V
	5	(5)		–	0	–	V
	6	(6)		–	5.3	–	V
	7	(7)		–	0.6	–	V
	8	(8)		–	5.2	–	V
	9	(9)		–	5.4	–	V
	–	(10)		–	n.c.	–	
	–	(11)		–	n.c.	–	
	10	(12)		–	5.1	–	V
	11	(13)		–	5.4	–	V
	12	(14)		–	5.3	–	V
	13	(15)		–	0	–	V
	14	(16)		–	0	–	V
	15	(17)		–	0	–	V
	16	(18)		–	0	–	V
	17	(19)		–	7.5	–	V
	18	(20)		–	0	–	V

AC CHARACTERISTICS

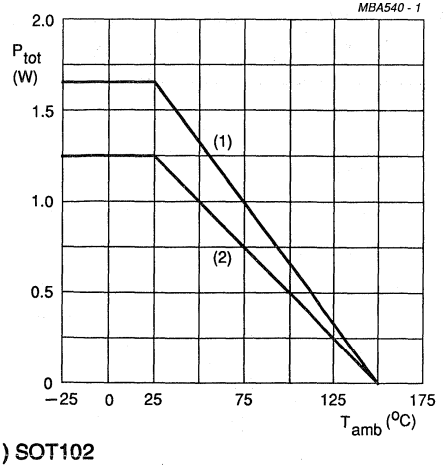
V_P = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute						
SOFT MUTE (V_L)						
Z_I	input impedance (pin 3 (3))		–	20	–	kΩ
MR	mute range	note 1	17	19.3	–	V
V_{aud}/V_I	mute gain	V_L = 2.75 V	–	2.7	–	dB
		V_L = 1.45 V	–1	0.6	2	dB
HARD MUTE (VMUTE)						
V_{mute}	–60 dB output attenuation		–	455	–	mV
$+I_m$	mute ON sink current	V_{mute} = 1 V, V_L = 0 V	–	370	–	µA
$-I_m$	mute "OFF" source current	V_{mute} = 0 V	3	–	–	µA
THD	total harmonic distortion	V_i = 200 mV; V_L = 2.5 V	–	0.09	–	%
$V_{I(p-p)}$	audio input voltage (peak-to-peak value)	THD > 10%	–	3	–	V
(S+N)/N	signal-to-noise ratio; measured with dB(A) curve	V_{aud} = 600 mV; 1 kHz; V_L = 3 V	–	95	–	dB
V_{aud}/V_p	ripple rejection	note 2; 300 Hz; 100 mV; V_L = 2.5 V	28	32	–	dB
V_{ref}	output reference voltage		–	5.3	–	V
V_{off1}	audio comparator offset voltage	$V_{off1} = V_{min} - V_{ap}$				
		with priority	–	+250	–	mV
		with no priority				
		V_t = 0 V	–	–1100	–	mV
		V_t = 3 V	–	–348	–	mV
Level comparator						
$V_{ref}-V_{il}$	voltage for high comparator output		–	56	–	mV
t	monostable multivibrator time period	started with both comparator outputs HIGH	16	21	28	µs
Timing/memory						
$-I_t$	source current		–	30	–	µA
C_t	value delay capacitor		–	–	50	nF
T_t	timing duration	C_t = 47 nF	–	6	–	ms
$+I_t$	reset current	V_t = 3 V	–	17.7	–	mA
V_t	change of priority antenna		–	3.7	–	V
Antenna switch outputs						
$-I_{os}$	output source current		–	–	7	mA
$+I_{os}$	output sink current		–	–	7	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SO}	selected output voltage					
		I_{SO} = −10 mA	V_P−2 V	–	–	V
		I_{SO} = 0.5 mA	V_P−1 V	–	–	V
V_{NSO}	not selected output voltage					
		I_{SO} = +10 mA	–	–	0.7	V
		I_{SO} = 0 mA	–	–	0.1	V
Mode selection						
ENABLE						
V_r	all functions active		–	–	1	V
$-I_r$	input current	V_r = 1 V	–	–	12	µA
RESET (ACTIVE AT OPEN INPUT)						
V_r	voltage at first antenna (pin 17 (19))		4.2	–	V_P	V
STOP						
V_r	keep selected antenna voltage		1.6	–	3.5	V

Notes to the AC characteristics

1. $\frac{V_{aud}\,(a\ V_L = 2.75\ V)}{V_{aud}\,(a\ V_L = 0.1\ V)}$
2. When V_P (pin 1 (1)) is filtered with R = 25 Ω and C = 100 µF the ripple rejection becomes 46 dB



(1) SOT102
(2) SOT163A

Fig.4 Derating curve.

INTEGRATED AM UPCONVERSION RECEIVER

GENERAL DESCRIPTION

The TEA6200 is an integrated AM upconversion receiver circuit with an IF of 10.7 MHz. Because of the high dynamic range of the RF prestage there is no tuned prestage. The whole selectivity is provided by crystal filters. The circuit is intended for use in AM radios with synthesizer tuning.
The TEA6200 can handle RF signals up to 2 V RMS.

Features

- No pre-tuned selection is required
- No LW/MW switching
- RF input is protected from static discharge from the aerial
- Electronic standby switch
- Voltage controlled oscillator for synthesizer tuning
- IF output providing level information for search tuning.
- No alignment required.

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7.6	8.5	9.4	V
Supply current range	I_P	–	50	70	mA
AF output voltage with: RF at 1 MHz and 10 mV f_m at 400 Hz and 30%	V_{af}	–	350	–	mV
AGC start	V_{rf}	30	50	80	μV
AGC range	ΔV_{rf}	–	95	–	dB

PACKAGE OUTLINE

20-lead dual in line; plastic (SOT146).

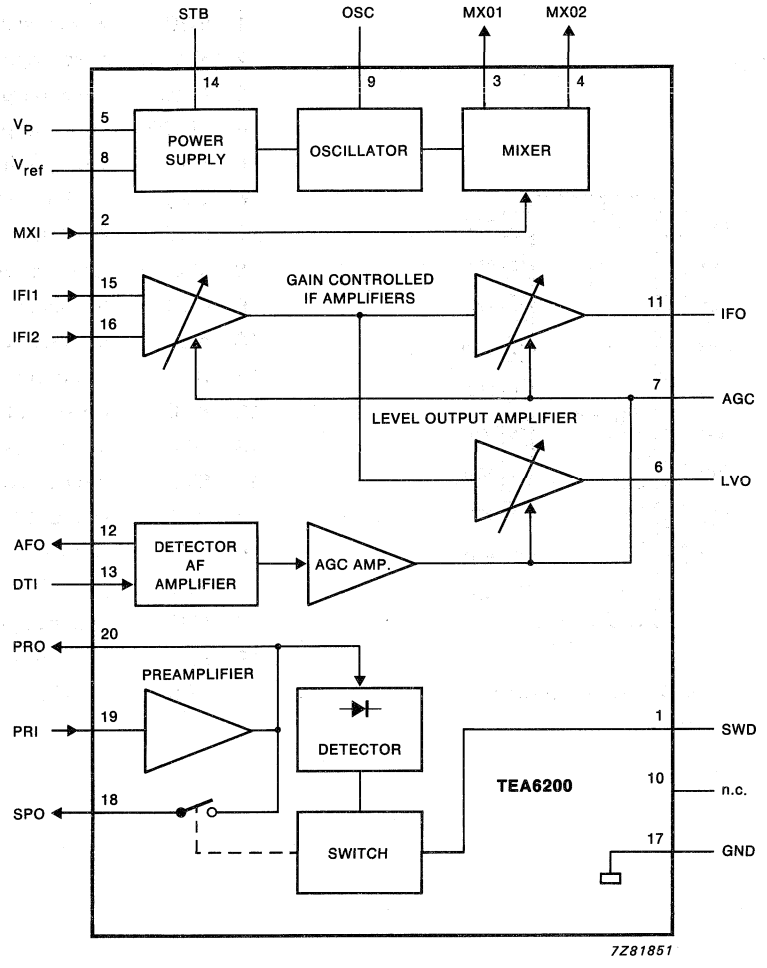


Fig. 1 Block diagram.

PINNING

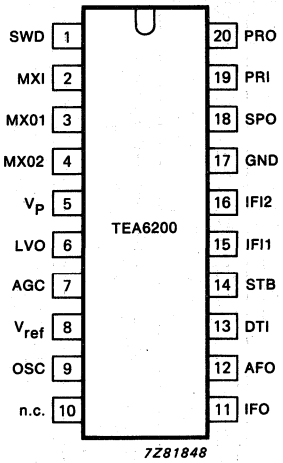


Fig. 2 Pinning diagram.

1	SWD	switching delay
2	MXI	mixer input
3	MXO1	mixer output 1
4	MXO2	mixer output 2
5	V_P	supply voltage
6	LVO	level output
7	AGC	AGC time constant
8	V_{ref}	reference voltage
9	OSC	oscillator
10	n.c.	not internally connected*
11	IFO	IF output
12	AFO	AF output
13	DTI	detector input
14	STB	standby switch
15	IFI1	IF input 1
16	IFI2	IF input 2
17	GND	ground
18	SPO	switched prestage output
19	PRI	prestage input
20	PRO	prestage output

* Pin 10 must be connected to pin 5, 8 or 17.

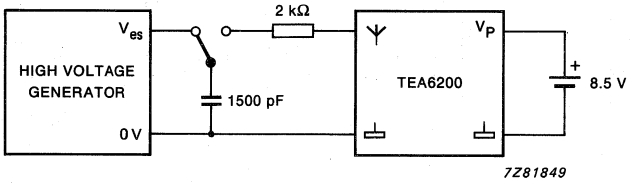
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	12	V
Supply current	I_P	–	70	mA
Total power dissipation	P_{tot}	–	850	mW
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 150	°C
Electrostatic discharge voltage	$\pm V_{es}$	–	10	kV

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 80 K/W



Will tolerate discharge between −10 kV and + 10 kV.

Fig. 3. Test circuit in accordance with IEC 315-1 clause 25.

DC CHARACTERISTICS

V_P = 8.5 V; V_{14} = V_P; Signal in OFF condition; all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Mixer input		V_I	–	4.0	–	V
Mixer output 1		V_O	–	8.5	–	V
Mixer output 2		V_O	–	8.5	–	V
Level output		V_O	–	8.5	–	V
AGC voltage		V_{AGC}	–	0.65	–	V
Reference voltage		V_{ref}	–	4.0	–	V
Oscillator DC voltage		V_{OSC}	–	4.0	–	V
Prestage input		V_I	–	1.2	–	V
Prestage output		V_O	–	3.2	–	V

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; f_{RF} = 1 MHz at 10 mV RMS; Q_{OSC} = 50; modulation = 400 Hz at 30%; insertion loss of filters: crystal filter = 1 dB; ceramic filter = 4 dB, all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	7.6	8.5	9.4	V
Supply current range		I_P	–	50	70	mA
Guaranteed operating voltage		V_P	7.0	–	10.0	V
Standby switch						
ON voltage		V_{14}	3.2	–	V_P	V
OFF voltage		V_{14}	0	–	1	V
ON current		$\|I_{14}\|$	–	–	10	μA
OFF current		$-I_{14}$	–	–	0.5	mA
Supply current	device OFF	I_P	–	–	10	mA
Prestage	note 1					
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis		V_{rf}	1.5	3.5	5.5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Frequency range		f_{osc}	10.8	–	17.8	MHz
Oscillator amplitude		V_{osc}	200	420	–	mV
Tuned circuit selectivity		Q_{OSC}	20	50	–	–
Mixer						
Input capacitance		$C_{2\text{-}8}$	–	5	10	pF
Input impedance		$Z_{2\text{-}8}$	10	40	–	kΩ
Conversion transconductance		$I_{3\text{-}4}/V_{2\text{-}8}$	–	3.8	–	S
IF amplifier						
Input impedance		$R_{16\text{-}15}$	10	–	–	kΩ
Input capacitance		$C_{16\text{-}15}$	–	–	5	pF
Output impedance		Z_{11}	230	330	430	Ω
Detector	note 2					
Input impedance		Z_{13}	265	380	500	Ω
Output impedance		Z_{12}	7	10	14	kΩ
Output level		V_{af}	250	350	500	mV
Reference voltage						
Voltage	V_P = 8.5 V	V_8	3.8	4.0	4.2	V
Output impedance		Z_8	–	20	–	Ω
Ripple rejection		$\frac{\Delta V_P}{\Delta V_8}$	40	–	–	dB
Level output pin 6	see Fig. 5					
Output impedance		Z_6	–	1	–	kΩ
Output voltage	V_{rf} = 70 μV	V_6	0.5	0.7	1.0	mV
Output voltage	V_{rf} = 2 mV	V_6	–	15	–	mV

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input	(S + N)/N = 6 dB	V_{rf}	–	11	20	μV
	(S + N)/N = 26 dB	V_{rf}	–	110	150	μV
	(S + N)/N = 46 dB	V_{rf}	–	1100	2000	μV
	RF = 150 kHz (S + N)/N = 26 dB	V_{rf}	–	200	–	μV
Output signal						
AF output voltage	V_{rf} = 10 mV	V_{af}	250	350	500	mV
	V_{rf} = 20 μV	V_{af}	–	100	–	mV
Total distortion	V_{rf} = 1 mV; modulation = 80%	d_{tot}	–	3	5	%
Signal plus noise-to-noise ratio	RF = 10 mV to 1 V	(S + N)/N	53	57	–	dB
Ripple rejection	V_P = 8.5 V + V_r 20 Hz < fR < 20 kHz V_{rms} = 40 mV	$\frac{\Delta V_P}{\Delta V_{af}}$	20	–	–	dB
Large signal handling						
Aerial input voltage	THD = 10%; modulation = 80%	V_{rf}	2	3	–	V
AGC range of preamplifier switch			–	12	–	dB
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis	modulation = 80%	V_{rf}	1.5	3.5	5.5	dB
Ripple rejection of preamplifier	20 Hz < f_R < 1.5 MHz	$\frac{\Delta V_P}{\Delta V_{20}}$	–	40	–	dB
AGC						
AGC range			–	95	–	dB
Change of V_{af}	100 μV < V_{rf} < 2 V		–	2	3	dB
AGC start		V_{rf}	30	50	80	μV
Intermodulation free dynamic range						
Long wave	350/250 kHz					
second order	input noise level = –99 dBm	IMFDR 2	72	82	–	dB
third order	input noise level = –99 dBm	IMFDR 3	–	86	–	dB
Medium wave	650/1550 kHz					
second order	input noise level = –104 dBm	IMFDR 2	74	84	–	dB
third order	1.25/1.4 MHz input noise level = –104 dBm	IMFDR 3	–	90	–	dB

Notes to the characteristics

1. The prestage is connected to the aerial by a 6 MHz low-pass filter that decouples unwanted aerial cable resonance frequencies. The large dynamic range of the prestage is achieved by use of a transimpedance amplifier with a feedback loop consisting of an equivalent aerial capacitance and a feedback capacitor. When large RF signals are received the feedback capacitance in the loop is increased and the gain subsequently reduced, (see Fig. 4).

   Voltage gain for small signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1}$

   Voltage gain for large signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1 + C_2}$

2. To protect the demodulator and the AGC circuitry, against parasitic oscillation in the IF section, a ceramic filter is connected between the IF output and detector input.

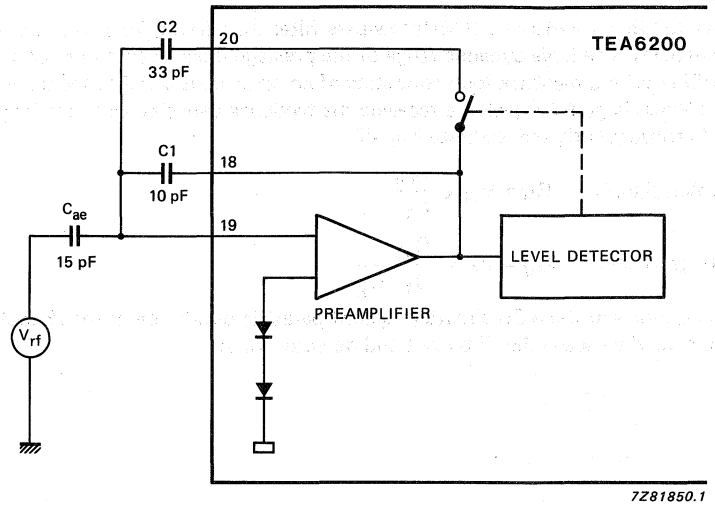


Fig. 4 Prestage circuit.

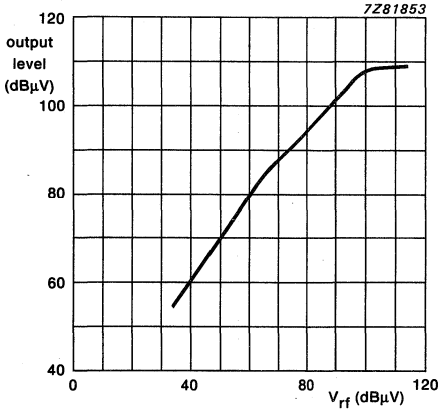


Fig. 5 IF output level.

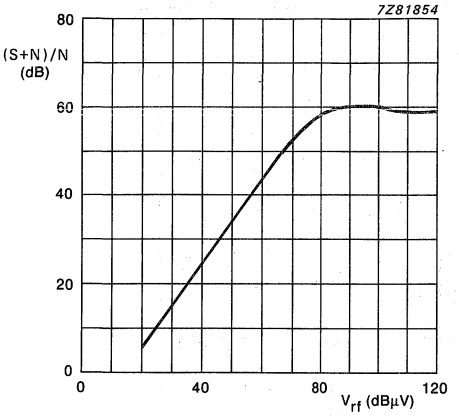


Fig. 6 Signal plus noise-to-noise ratio.

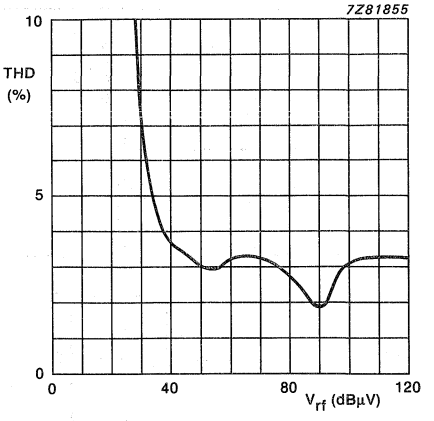


Fig. 7 Total harmonic distortion.

APPLICATION INFORMATION

Notes Fig. 8.

	Component	Circuit identity	Supplier reference
(1)	Crystal filters	XTAL	NDK 10T 7 BA
(2)	Ceramic filter	SFE	Murata E 10 7 S
(3)	Transformer	T1	Toko 7PS-1078 JK
(4)	Variable capacitance diode.	D1	BB609, BB809 or BBY40
(5)	Oscillator coil	L1	Toko 7PS-1077 X

APPLICATION INFORMATION

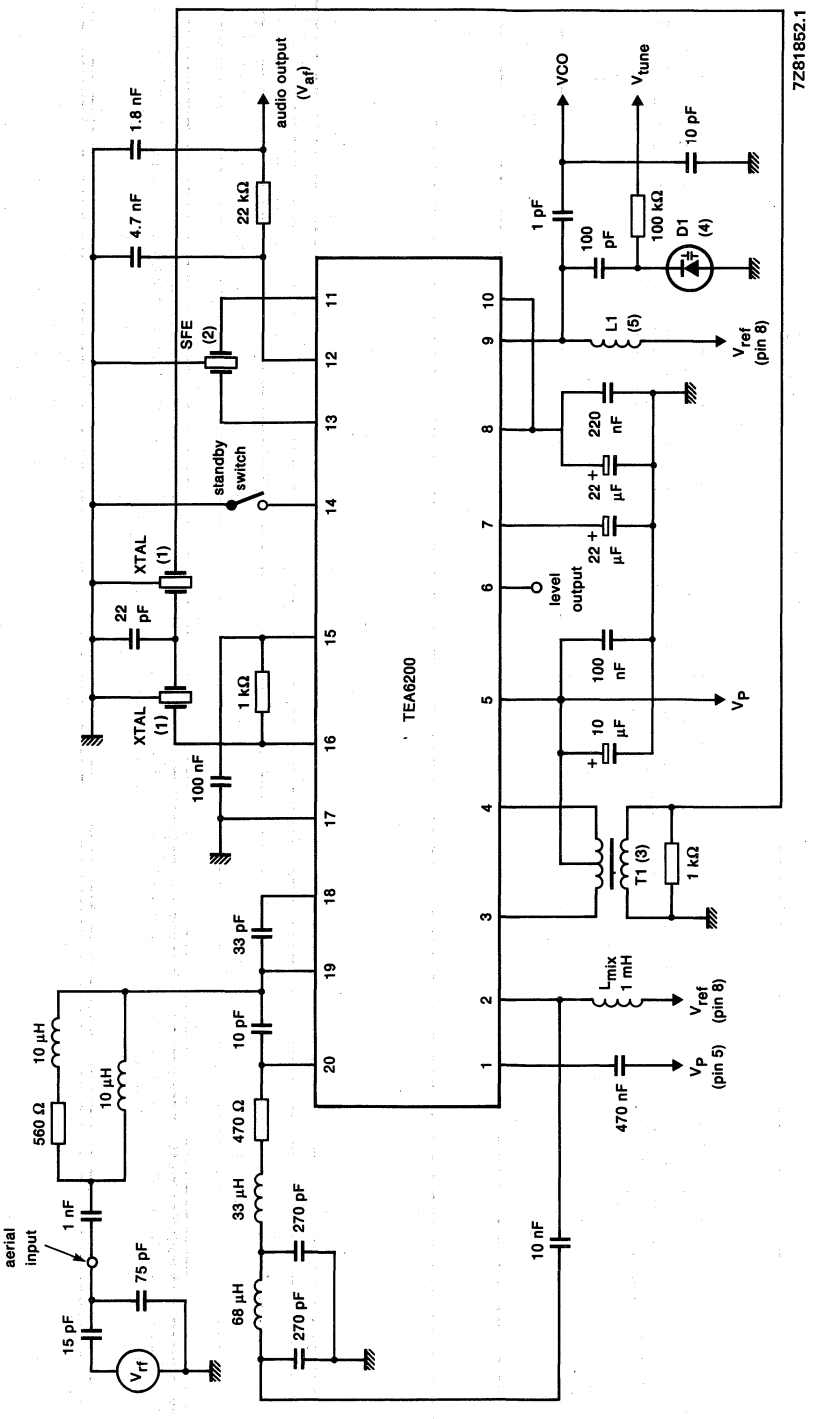


Fig. 8 Application diagram.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

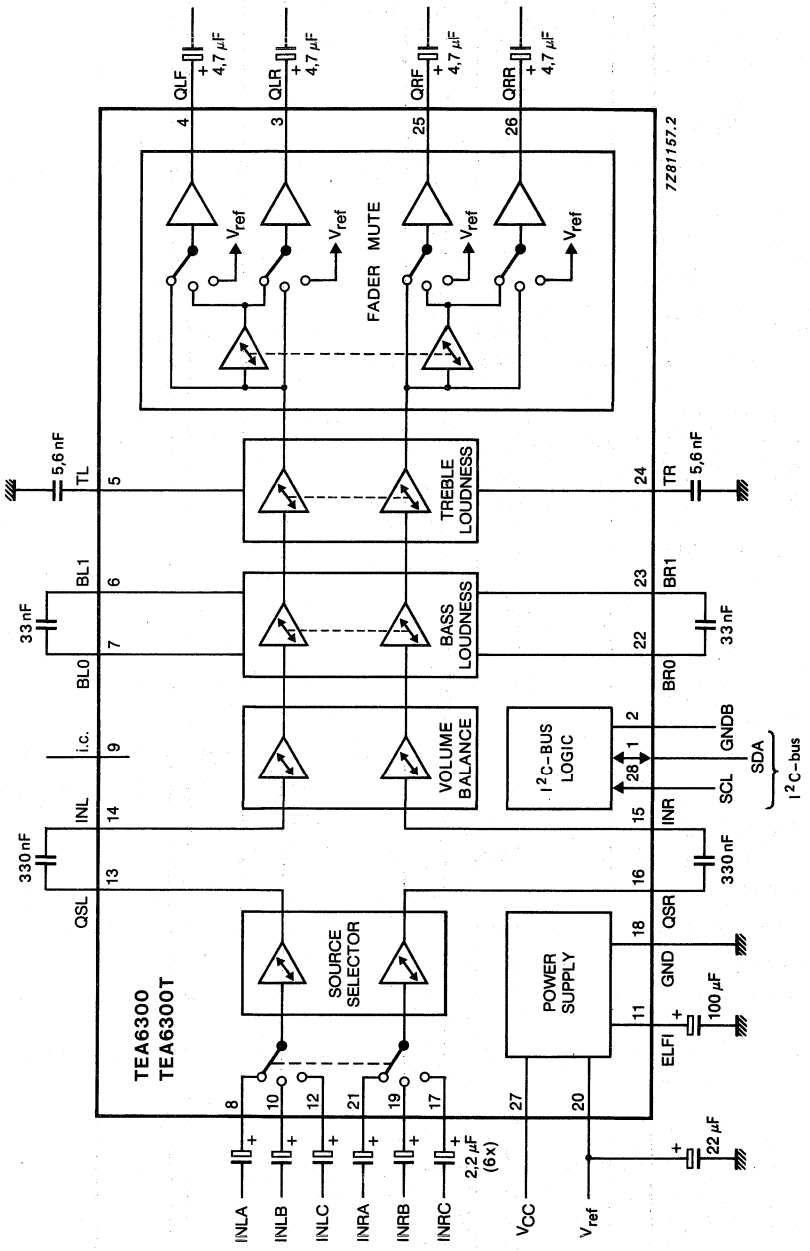


Fig. 1 Block diagram.

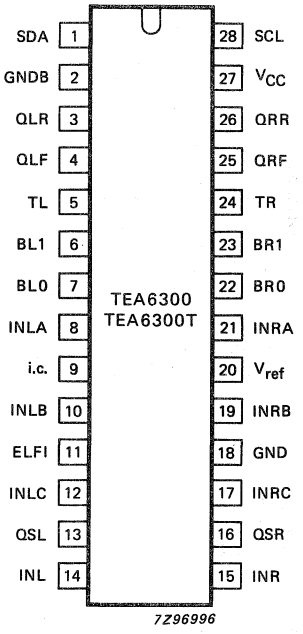
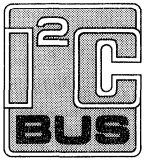


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels —RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	33	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage for start of clipping	$V_{o(rms)}$ $V_{o(rms)}$	– –	500 1000	– –	mV mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency –1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz V_i = 50 mV; G_v = 20 dB V_i = 500 mV; G_v = 0 dB V_i = 1,6 V; G_v = –10 dB	 THD THD THD	 – – –	 0,1 0,05 0,2	 0,3 0,2 0,5	 % % %
Ripple rejection $V_{r(rms)}$ < 200 mV; G_v = 0 dB; bass and treble linear; at f = 100 Hz at f = 40 Hz to 12,5 kHz	 RR_{100} RR_{range}	 – –	 70 60	 – –	 dB dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value)					
THD < 0,5%	$V_{i(rms)}$	–	1,65	–	V
THD < 0,5%; V_{CC} = 7,5 V	$V_{i(rms)}$	–	1,5	–	V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	72	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_v = 0 to −66 dB		–	–	10	mV
In any bass position G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	−10	–	+ 10	μA
LOW	I_{IL}	−10	–	+ 10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

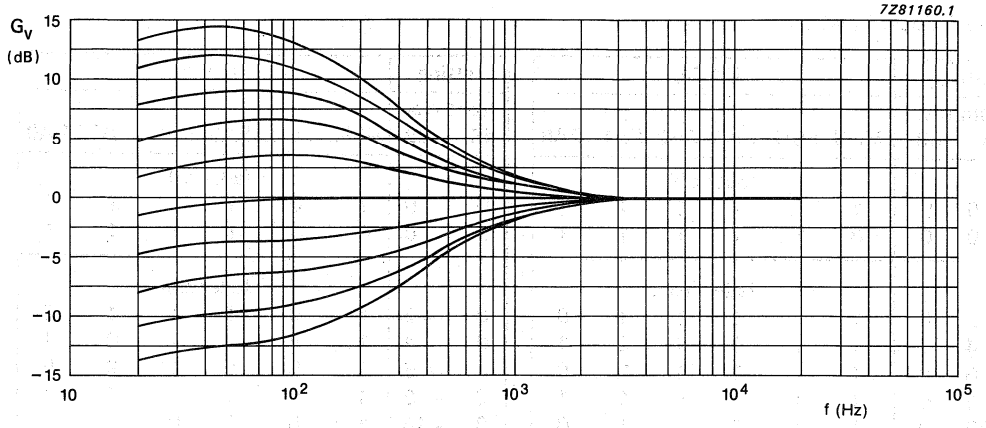


Fig. 3 Bass control without T-pass filter.

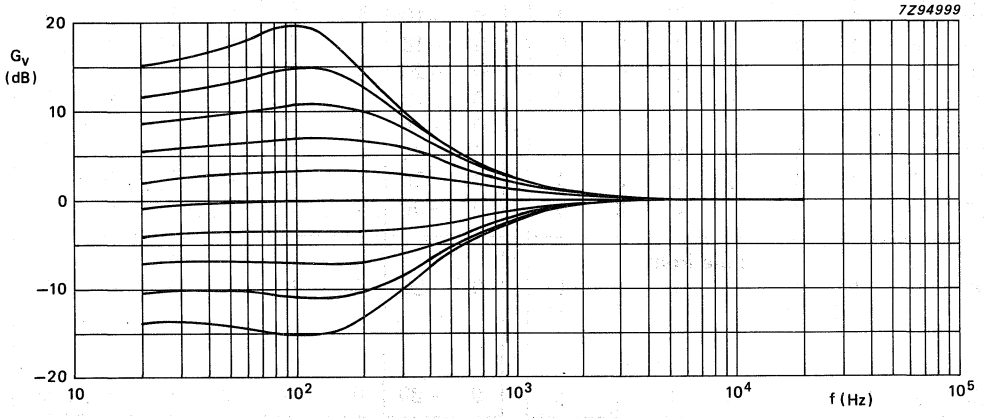
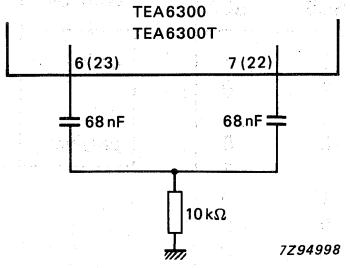


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

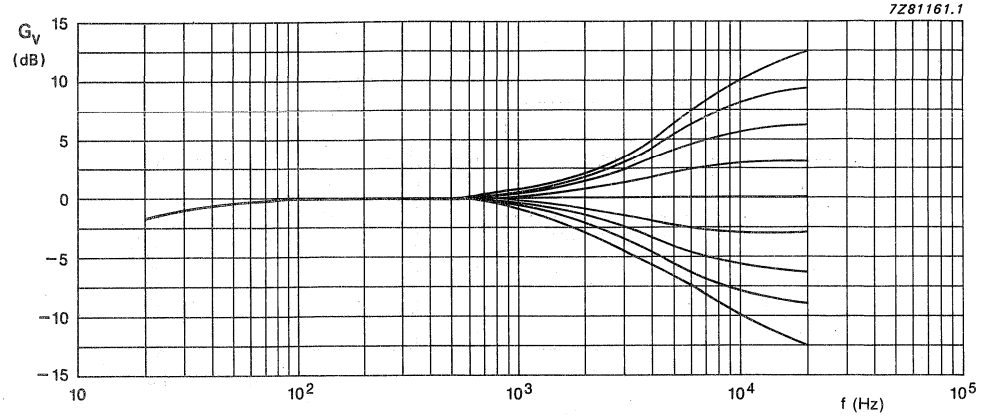


Fig. 6 Treble control.

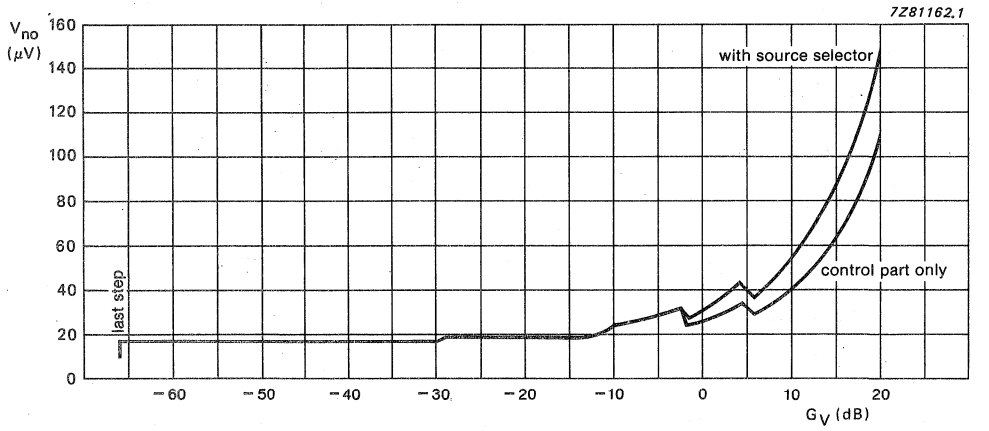


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

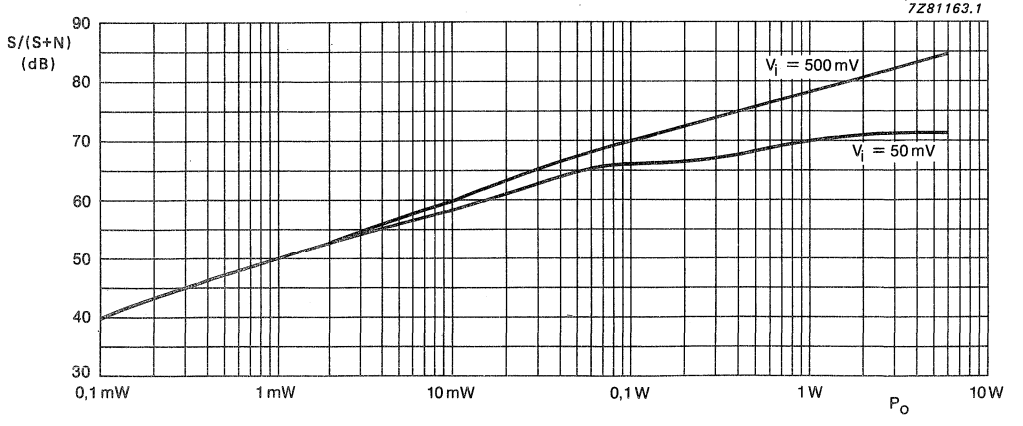


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

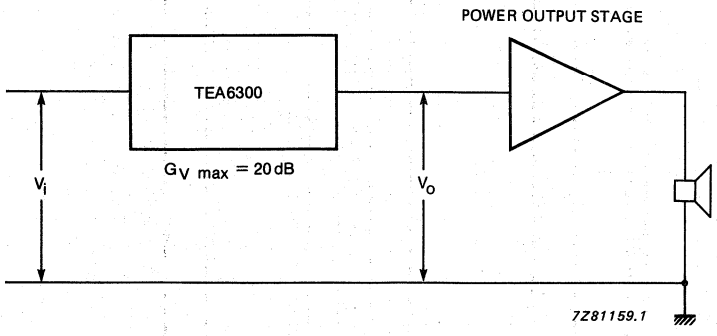


Fig. 9 Recommended level diagram; $V_{i\ min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

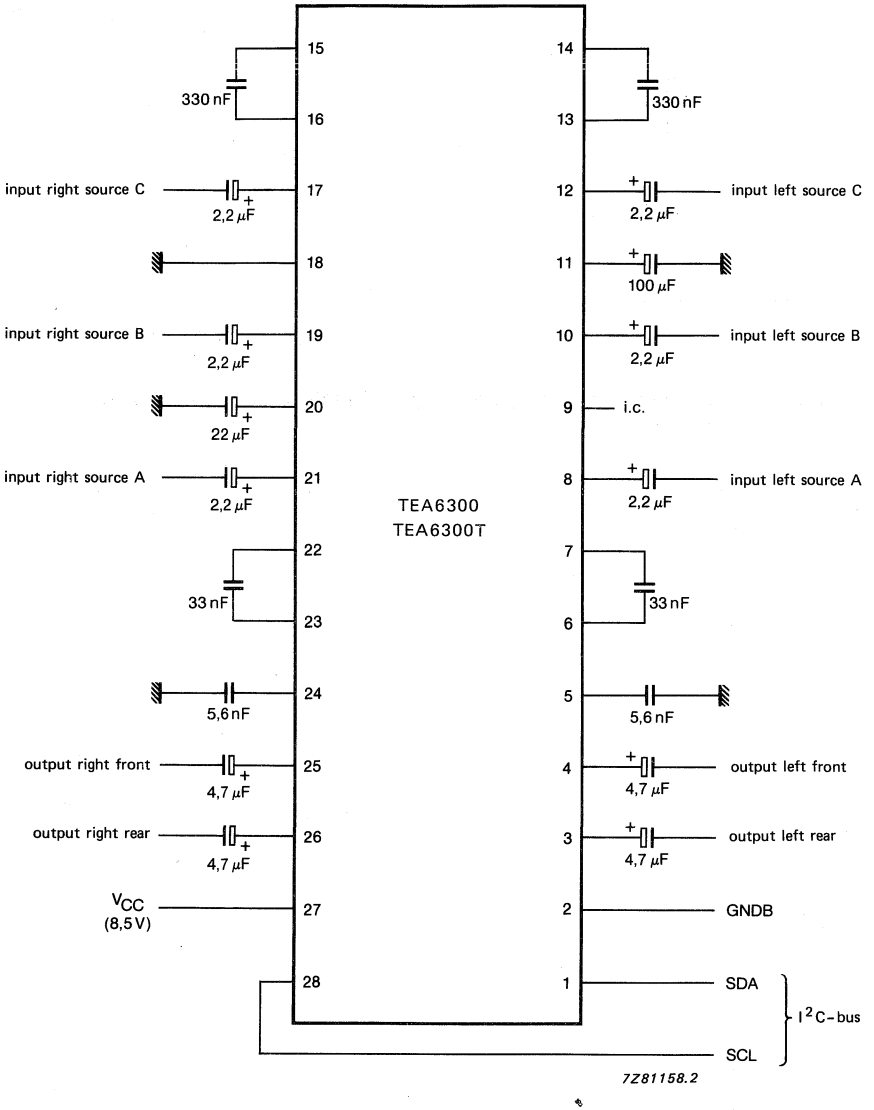


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled tone and volume control circuit for car radios.

Features

- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from +15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control form 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

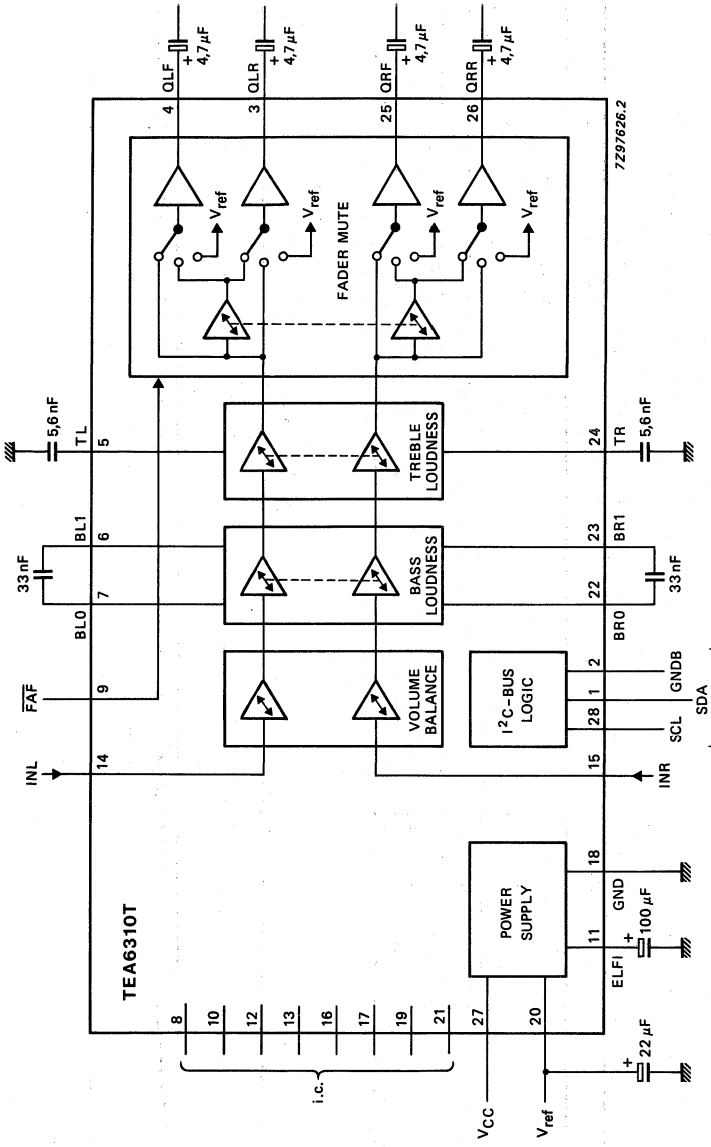


Fig. 1 Block diagram.

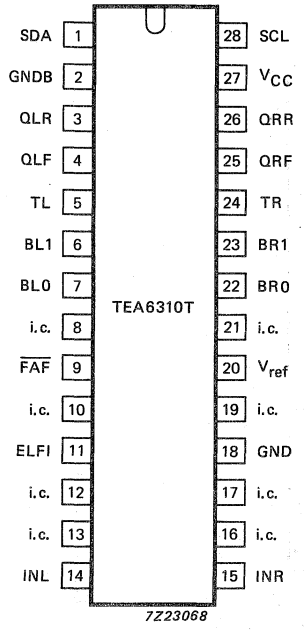


Fig. 2 Pinning diagram

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	i.c.	internally connected
9	$\overline{FAF}$	fader off control input
10	i.c.	internally connected
11	ELFI	electronic filtering for supply
12	i.c.	internally connected
13	i.c.	internally connected
14	INL	input left control part
15	INR	input right control part
16	i.c.	internally connected
17	i.c.	internally connected
18	GND	ground
19	i.c.	internally connected
20	V_{ref}	reference voltage (1/2 V_{CC})
21	i.c.	internally connected
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6310T has four outputs a low level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at $\overline{FAF}$ (pin 9).
An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6310T is required.

The on-chip power-on-reset sets the TEA6310T to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ <200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio; bass and treble linear; notes 1 and 2; CCIR 468-2 weighted; quasi peak;					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	S/(S + N)	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	S/(S + N)	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	86	–	dB
Noise output power mute position, only contribution of TEA310T, power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_v = 0 dB; bass and treble linear;	α_B	–	110	–	dB
Control part					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF
Maximum input voltage; THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage; weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off;					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error; (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error; (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error; balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB

parameter	symbol	min.	typ.	max.	unit
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position					
G_v = 0 to −66 dB		–	–	10	mV
In any bass position					
G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range;					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Fader control					
Continous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Fader enable/disable control (pin 9)					
Fader enabled					
Input voltage HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled					
Input voltage LOW	$V_{9\text{-}18}$	−0,3	–	1,5	V
Input current					
HIGH	I_9	−10	–	+10	μA
LOW	I_9	−10	–	+10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	+10	μA
LOW	I_{IL}	−10	–	+10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 10000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_v dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_v dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front rear dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front rear dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

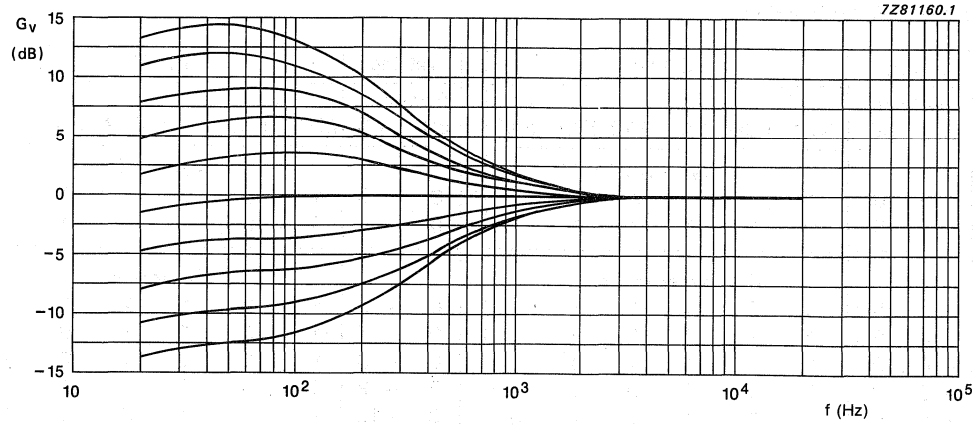


Fig. 3 Bass control without T-pass filter.

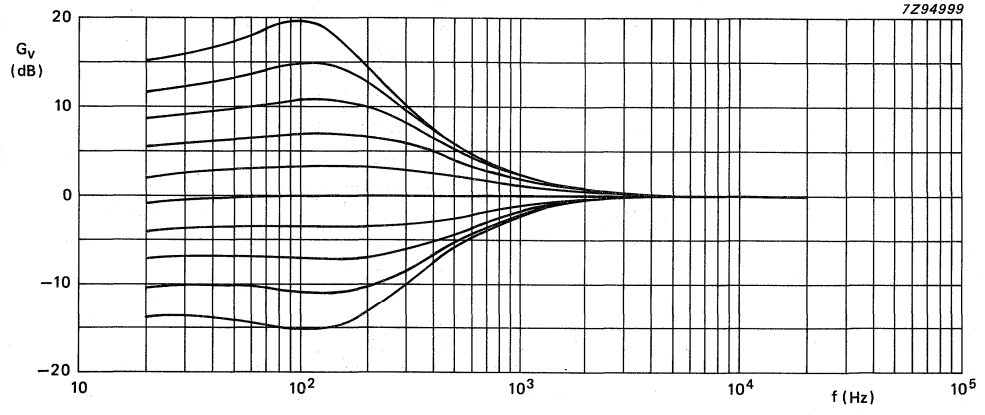
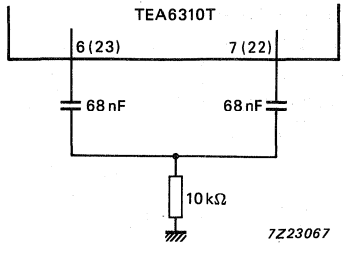


Fig. 4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig. 5 T-pass filer.

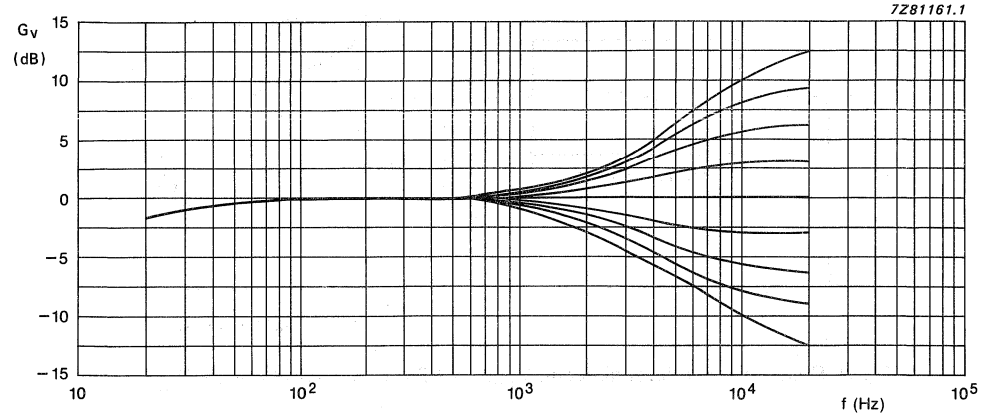


Fig. 6 Treble control.

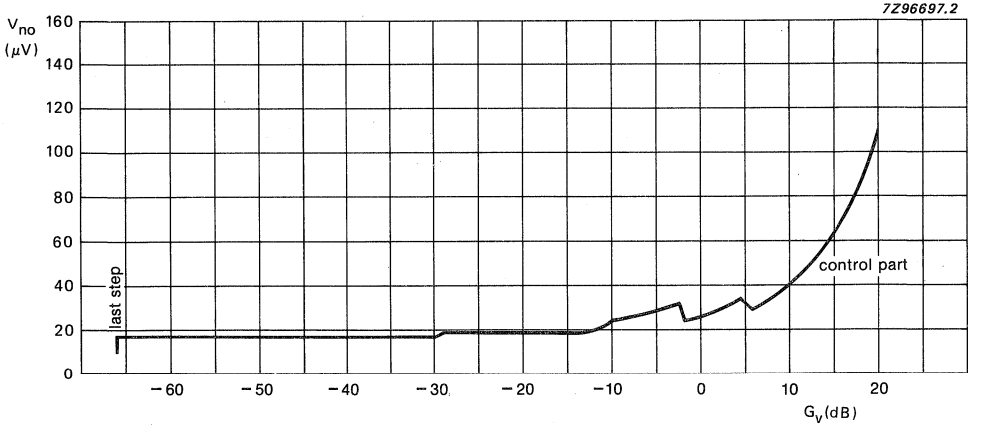


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

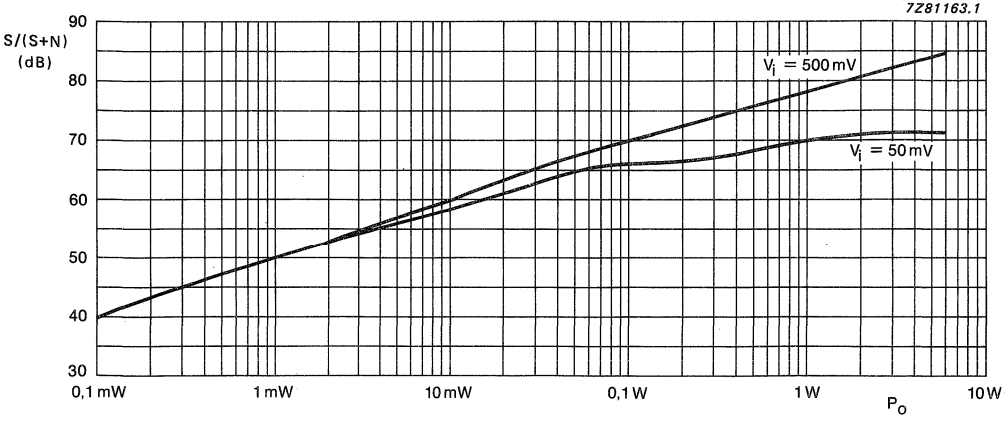


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

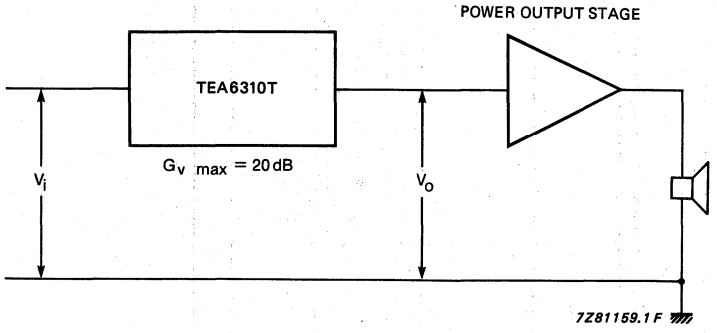


Fig. 9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

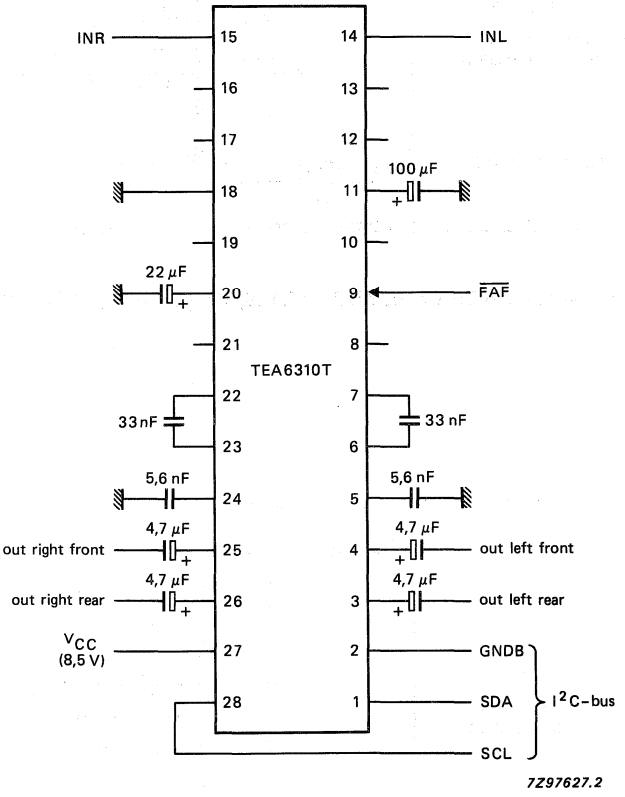


Fig. 10 Test and application circuit.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

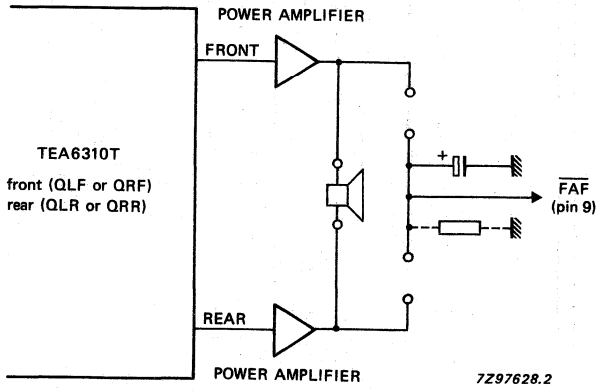


Fig. 11 Automatic FADER control; P_o = 24 W, V_{9-18} = 0 V (FADER disabled).

DEVELOPMENT DATA

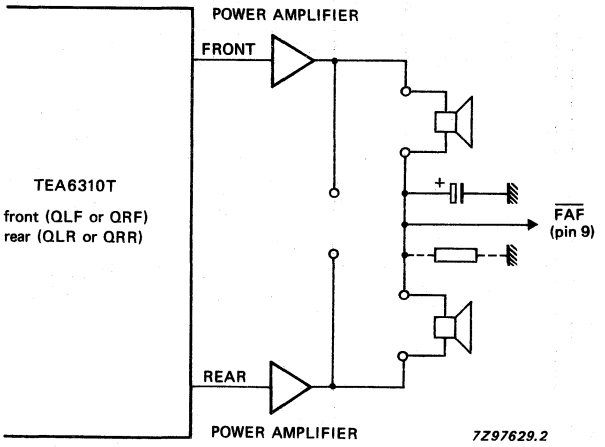


Fig. 12 Automatic FADER control; P_o = 2 x 6 W, V_{9-18} = 7 V (FADER enabled).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TEA6330T

Sound fader control circuit for car radios

FEATURES

- Stereo/hi-fi processor for car radios performed with volume, balance, bass and treble controls
- Sound fader control (front/rear) down to –30 dB in steps of 2 dB
- Fast muting via bus or via setting the muting pin
- Suitable for external audio equalizers, can be looped-in controlled by the I²C-bus
- Power-on reset on chip sets the device into general mute position
- AC and DC short-circuit protected concerning neighbouring pins
- I²C-bus control for all functions.

GENERAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for car radios, in addition with fader function and the possibility of an external equalizer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current	-	26	-	mA
V_i	maximum AF input signal (RMS value)	2	-	-	V
V_o	maximum AF output signal (RMS value)	1.1	-	-	V
ΔG_v	volume control range, separated	–66	-	+20	dB
	fader control range, separated	0	-	–30	dB
	bass control range	–12	-	+15	dB
	treble control range	–12	-	+12	dB
THD	total harmonic distortion	-	-	0.2	%
S/N(W)	weighted signal-to-noise ratio	-	67	-	dB
α_{CR}	crosstalk attenuation	-	90	-	dB
B	frequency response (–1 dB)	-	35 to 20000	-	Hz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6330T	20	SO	plastic	SOT163A

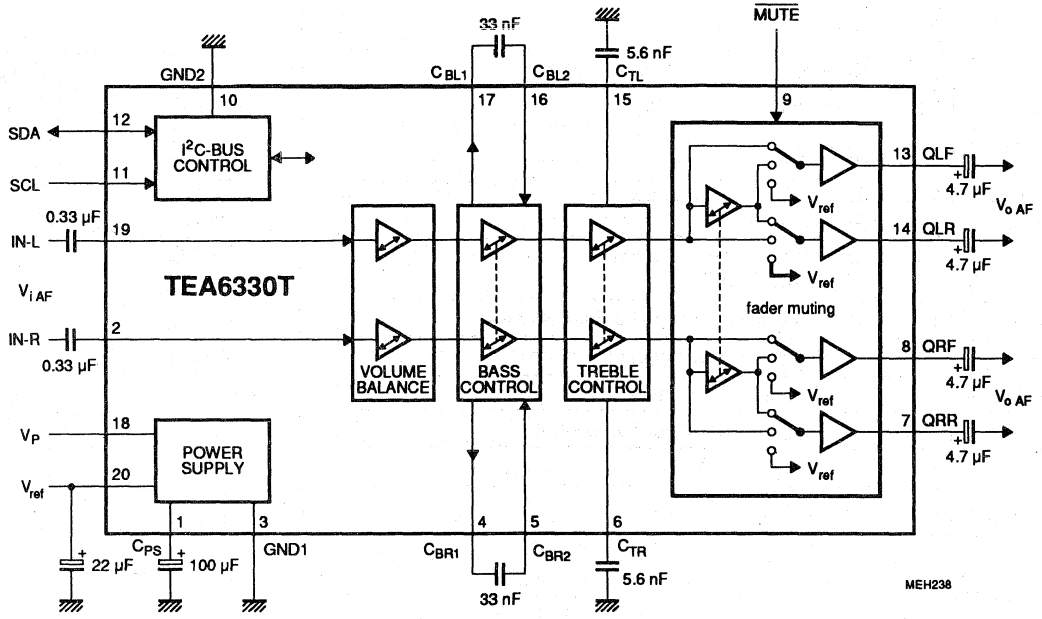


Fig.1 Block and test circuit.

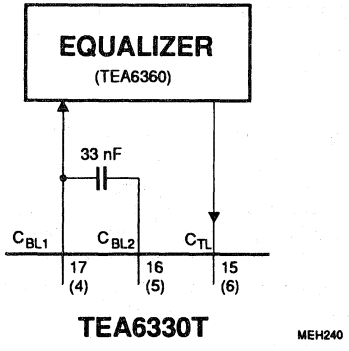


Fig.2 Connection of equalizer (Table 7). In application with equalizer circuit TEA6360 coupling capacitors are not necessary. Connectors for RIGHT in brackets.

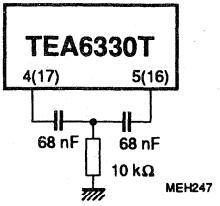


Fig.3 T-filter for enhanced bass control (Fig.5). Connectors for LEFT in brackets.

Sound fader control circuit for car radios

TEA6330T

PINNING

SYMBOL	PIN	DESCRIPTION
C_{PS}	1	filtering capacitor for power supply
IN-R	2	audio input signal RIGHT
GND1	3	analog ground (0 V)
C_{BR1}	4	capacitor for bass control RIGHT and signal to equalizer
C_{BR2}	5	capacitor for bass control RIGHT
C_{TR}	6	capacitor for treble control RIGHT, input signal for equalizer RIGHT
QRR	7	right audio output signal of rear channel
QRF	8	right audio output signal of front channel
MUTE	9	input to set mute externally
GND2	10	digital ground (0 V) for bus control
SCL	11	clock signal of I²C-bus
SDA	12	data signal of I²C-bus
QLF	13	left audio output signal of front channel
QLR	14	left audio output signal of rear channel
C_{TL}	15	capacitor for treble control LEFT, input signal for equalizer LEFT
C_{BL2}	16	capacitor for bass control LEFT
C_{BL1}	17	capacitor for bass control LEFT and signal to equalizer
V_P	18	+8.5 V supply voltage
IN-L	19	audio input signal LEFT
V_{ref}	20	reference voltage output (V_P/2)

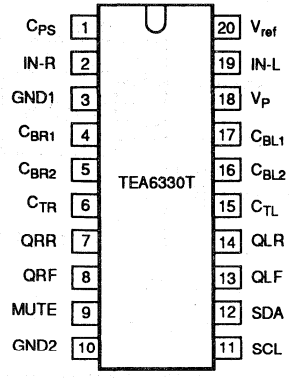


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for car radios including fader function and the possibility of an external equalizer. The sound signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantages of this principle are the combination of low noise, low distortion and a high dynamic range. The separated volume controls of the left and the right channel make the balance control possible. The value and the characteristic of the balance is controlled via the I²C-bus.

The contour function is performed by setting an extra bass control and optional treble, depending on the actual volume position. Its switching points and its range are also controllable via the I²C-bus.
An interface is assigned behind the volume control to loop-in an equalizer (Fig.2). In this case the treble control is switched off, and the bass control can be used to set the contour.

Low level control fader is included independent of the volume controls, because the TEA6330T has four driver outputs (for front and rear).

An extra mute position for the front, the rear or for all channels is built in. The last function may be used for muting during preset selection.
No external interface is required between the microcomputer and this circuit, for all switching and controlling functions are controllable via the two-wire I²C-bus.

The separate mute-pin allows to switch the fader into mute position without using the I²C-bus.
The on chip power-on reset sets the TEA6330T into the general mute mode.

Sound fader control circuit for car radios

TEA6330T

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	0	10	V
P_{tot}	total power dissipation	0	700	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V
	electrostatic handling** for all pins	-	±4000	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V; load resistors at audio outputs 10 kΩ, f_i = 1 kHz (R_S = 600 Ω), bass and treble in linear position, fader in off position and T_{amb} = 25 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		7	8.5	10	V
I_P	supply current		-	26	-	mA
V_{ref}	reference voltage (pin 20)		0.45 V_P	0.5 V_P	0.55 V_P	V
V_O	DC voltage at output (pins 7, 8, 13, 14)		-	0.5 V_P	-	V
Measurements over all						
V_i	maximum AF input level for THD = 2 % at pins 2 and 19 (RMS value)	G_v = –66 to –6 dB and V_P = 8.1 V	2	-	-	V
V_o	maximum AF output level for THD = 2 % at pins 7, 8, 13, 14 (RMS value)	G_v = –4 to +20 dB and V_P = 8.1 V	1.1	-	-	V
G_v	maximum gain by volume setting		19	20	21	dB
B	frequency response	–1 dB roll-off frequency	-	35 to 20000	-	Hz
α_{CR}	crosstalk attenuation	f = 250 to 10000 Hz G_v = 0 dB	70	90	-	dB
THD	total harmonic distortion	f = 20 to 12500 Hz				
	$V_{i\,(RMS)}$ = 50 mV	G_v = +20 dB	-	0.1	0.3	%
	$V_{i\,(RMS)}$ = 500 mV	G_v = 0 dB	-	0.05	0.2	%
	$V_{i\,(RMS)}$ = 1.6 V	G_v = –10 dB	-	0.2	0.5	%
RR	ripple rejection for V_R < 200 mV RMS	G_v = 0 dB				
		f = 100 Hz	-	70	-	dB
		f = 40 Hz to 3 kHz	-	60	-	dB
		f = 3 to 12.5 kHz	-	50	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_N	noise power at output of a 25 W power stage with 26 dB gain (only contribution of TEA6330T)	mute position (V_9 = 0)	-	-	10	nW
α_{BUS}	crosstalk attenuation between SDA, SCL and signal output (20 log V_{BUS} (p-p)/ V_o RMS)	G_v = 0 dB	-	110	-	dB
S/N(W)	weighted signal-to-noise ratio for	CCIR 468-2 quasi peak for 6 W power amplifier				
	V_i = 50 mV RMS	P_o = 50 mW	-	65	-	dB
	V_i = 500 mV RMS	P_o = 50 mW	-	67	-	dB
	V_i = 50 mV RMS	P_o = 1 W	65	72	-	dB
	V_i = 500 mV RMS	P_o = 1 W	71	78	-	dB
	V_i = 50 mV RMS	P_o = 6 W; Fig.9	-	72	-	dB
	V_i = 500 mV RMS	P_o = 6 W; Fig.9	-	86	-	dB
Audio frequency outputs QLF, QRF, QLR and QRR						
V_o	maximum output signal (RMS value)		1.1	-	-	V
R_o	output resistance (pins 7, 8, 13 and 14)		-	100	150	Ω
R_L	admissible output load resistor	to ground or V_{CC}	7.5	-	-	kΩ
C_L	admissible output load capacitor		-	-	2.5	nF
$V_{N(W)}$	weighted noise voltage at output	CCIR 468-2 ; Fig.8 quasi peak				
	for maximim gain	G_v = +20 dB	-	110	220	μV
	for 0 dB gain	G_v = 0 dB	-	25	50	μV
	for minimum gain	G_v = –66 dB	-	19	38	μV
	for mute position	(V_9 = 0)	-	11	22	μV
Volume control		R_G = 600 Ω				
R_I	input resistance (pins 2 and 19)		35	50	65	kΩ
G_v	volume control range	Table 2	–66	-	+20	dB
ΔG_v	step width		-	2	-	dB
	gain set error	G_v = –50 to +20 dB	-	-	2	dB
		G_v = –66 to –50 dB	-	-	3	dB
	gain tracking error	balance in mid position	-	-	2	dB
α_{mute}	mute attenuation at volume mute	set mute-bits	76	90	-	dB
Bass control						
G_v	controllable bass range	Table 3; Fig.6				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum boost	f = 100 Hz	12	13	14	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
	maximum attenuation	f = 100 Hz	10	11	12	dB
ΔG_v	step width	f = 40 Hz	2.5	3	3.5	dB

Sound fader control circuit for car radios

TEA6330T

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble control						
G_v	controllable treble range	Table 4; Fig.7				
	maximum boost	f = 10 kHz	9	10	11	dB
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	-	-	15	dB
	maximum attenuation	f = 10 kHz	9	10	11	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_v	step width	f = 15 kHz	2.5	3	3.5	dB
Fader control						
G_v	fader control range	Table 5	-	0 to −30	-	dB
	step width		1.5	2	2.5	dB
α_{MUTE}	mute attenuation	GMB-bit = 1; Table 6	74	84	-	dB
ΔV_o	DC offset output voltage (pins 7, 8, 13, 14)					
	between any adjoining volume step and any step to mute	G_v = −66 to 0 dB	-	0.2	10	mV
		G_v = 0 to +20 dB	-	2	15	mV
	in any treble and fader position	G_v = −66 to 0 dB	-	-	10	mV
	in any bass position	G_v = −66 to 0 dB	-	-	10	mV
External mute (pin 9)						
V_9	input voltage for MUTE-ON (LOW)	fader is switched into general mute position	0	-	1.5	V
	input voltage for MUTE-OFF (HIGH)	Tables 2 and 5	3	-	V_P	V
	input voltage for MUTE-OFF	pin 9 open-circuit	-	5	-	V
I_9	input current		-	-	±10	μA
I^2C-bus, SCL and SDA (pins 11 and 12)						
$V_{11, 12}$	input voltage HIGH-level		3	-	V_P	V
	input voltage LOW-level		0	-	1.5	V
$I_{11, 12}$	input current		-	-	±10	μA
V_{ACK}	output voltage at acknowledge (pin 12)	I_{12} = −3 mA	-	-	0.4	V
Power-on reset, when reset is active the GMU-bit (general mute) is set and the bus receiver is in reset position						
V_P	supply voltage for start of reset	increasing voltage	-	-	2.5	V
	supply voltage for end of reset	increasing voltage	5.2	6.0	6.8	V
	supply voltage for start of reset	decreasing voltage	4.2	5.0	5.8	V

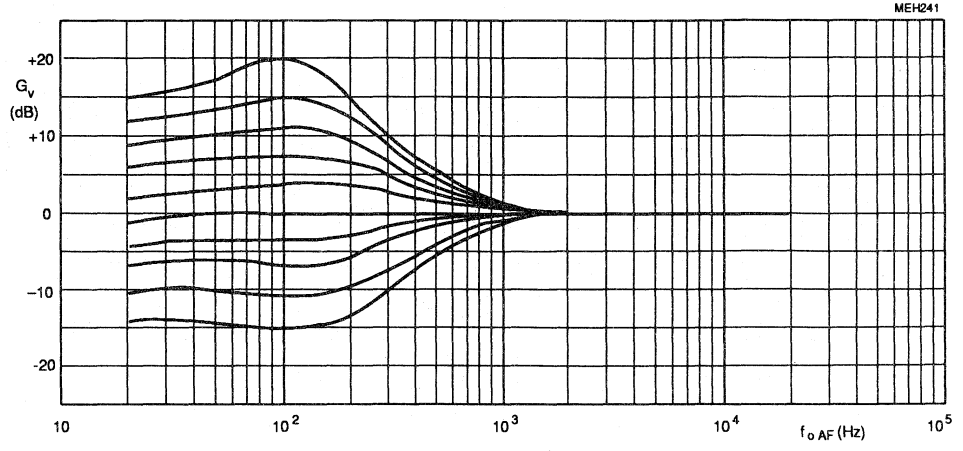


Fig.5 Bass control with enhanced control range (T-filter coupling, Fig.1).

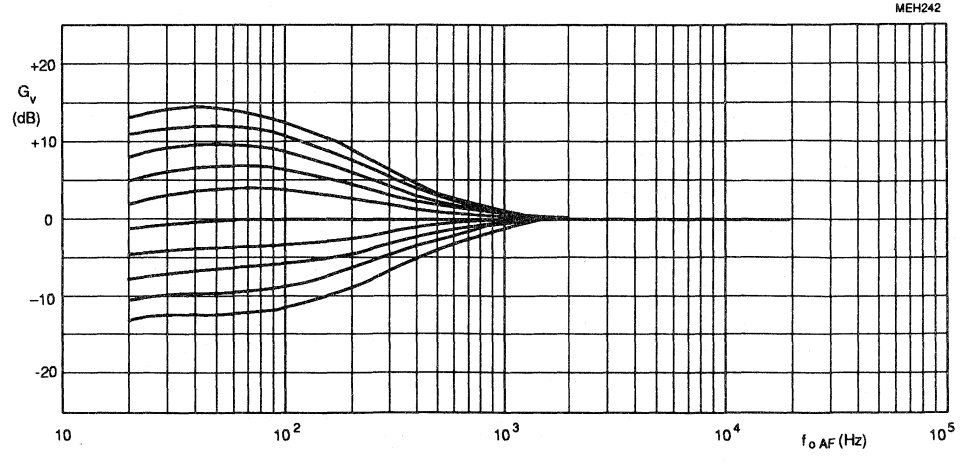


Fig.6 Bass control with normal control range (Fig.1).

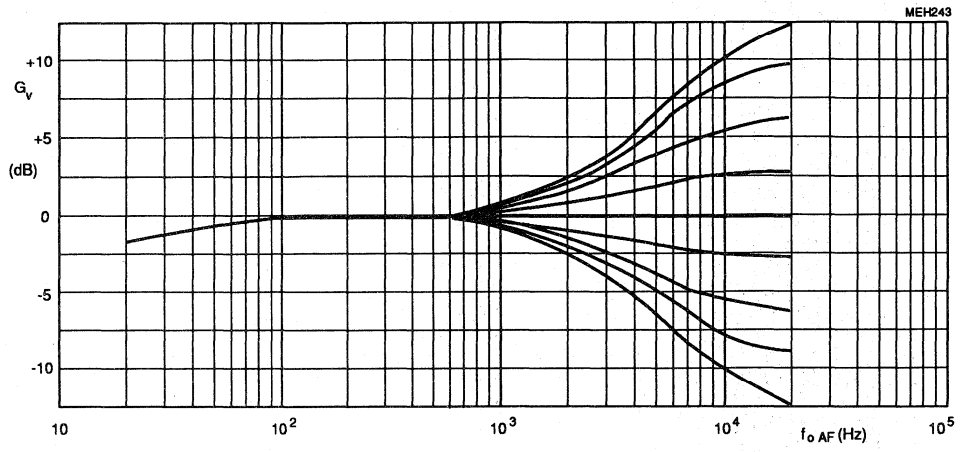


Fig.7 Treble control.

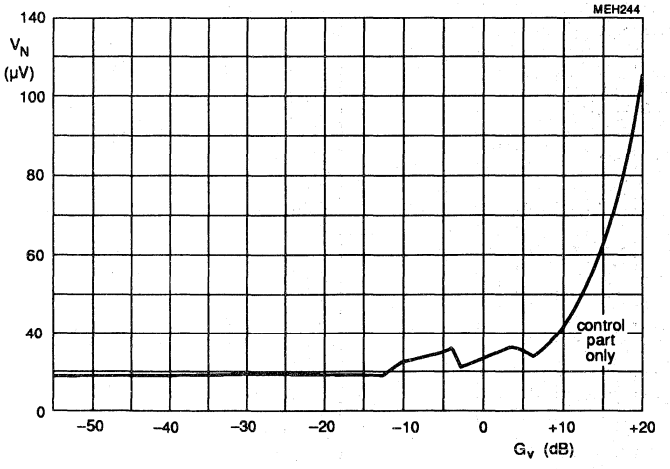


Fig.8 Noise voltage on outputs (CCIR 468-2 weighted, quasi-peak).

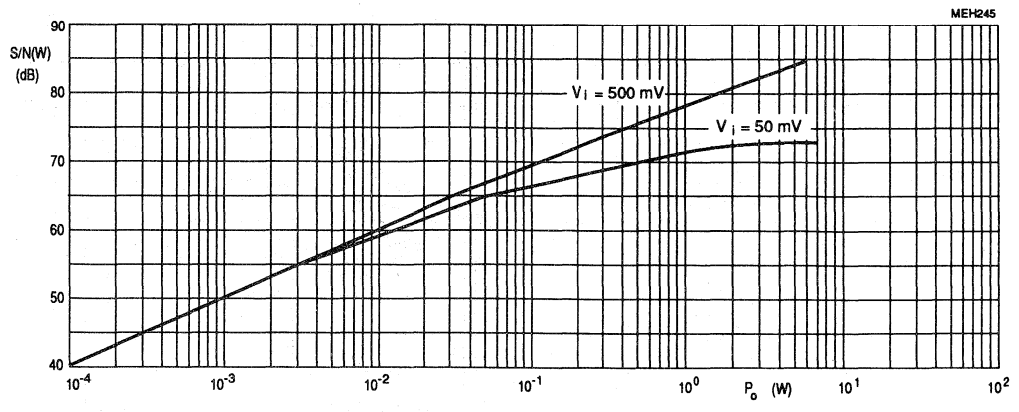


Fig.9 Signal-to-noise ratio (CCIR 468-2 weighted, quasi-peak) for TEA6330T with a 6 W power amplifier (20 dB gain, Fig.10). Measurements without noise contribution of the power amplifier.

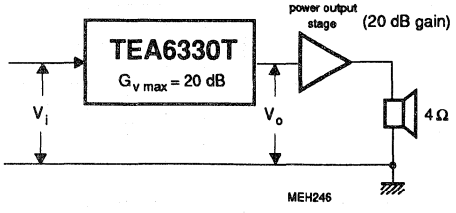


Fig.10 Signal-to-noise ratio measurement (Fig.9) with V_i = 50 mV RMS, V_o = 500 mV RMS for P_{max} = 6 W.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 000X**
A = acknowledge, generated by the slave
SUBADDRESS = subaddress byte, Table 1
DATA = data byte, Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission

function	subaddress byte								data byte D7	D6	D5	D4	D3	D2	D1	D0
volume left	0	0	0	0	0	0	0	0	0	0	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0	0	0	0	0	0	0	1	0	0	VR5	VR4	VR3	VR2	VR1	VR0
bass	0	0	0	0	0	0	1	0	0	0	0	0	BA3	BA2	BA1	BA0
treble	0	0	0	0	0	0	1	1	0	0	0	0	TR3	TR2	TR1	TR0
fader	0	0	0	0	0	1	0	0	0	0	MFN	FCH	FA3	FA2	FA1	FA0
audio switch	0	0	0	0	0	1	0	1	GMU	EQN	0	0	0	0	0	0

Function of the bits:

VL0 to VL5 volume control of left channel (balance control)
VR0 to VR5 volume control of right channel (balance control)
BA0 to BA3 bass control of both channels
TR0 to TR3 treble control of both channels
FA0 to FA3 fader control front to rear

FCH select fader channels front or rear
MFN mute control of the selected channels front or rear
GMU mute control, general mute
EQN equalizer switchover (0 = equalizer-on)

Table 2(a) Volume setting LEFT

G_v	DATA					
dB	VL5	VL4	VL3	VL2	VL1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
−2	1	1	0	1	0	0
−4	1	1	0	0	1	1
−6	1	1	0	0	1	0
−8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
---			---			---
---			---			---
---			---			---
mute left	0	0	0	0	0	0

Table 2(b) Volume setting RIGHT

G_v	DATA					
dB	VR5	VR4	VR3	VR2	VR1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
−2	1	1	0	1	0	0
−4	1	1	0	0	1	1
−6	1	1	0	0	1	0
−8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
---			---			---
---			---			---
---			---			---
mute right	0	0	0	0	0	0

Table 3(a) Bass setting with equalizer passive (EQN = 1)

G_v	DATA			
dB	D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 3(b) Bass setting with equalizer active (EQN = 0)

G_v	DATA			
dB	D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 4(a) Treble setting with equalizer passive (EQN = 1)

G_v	DATA			
dB	D3	D2	D1	D0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 4(b) Treble setting with equalizer active (EQN = 0)

G_v	DATA			
dB	D3	D2	D1	D0
0	1	1	1	1
0	1	1	1	0
0	1	1	0	1
0	1	1	0	0
0	1	0	1	1
0	1	0	1	0
0	1	0	0	1
0	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 5(a) Fader function front

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
–2	0	1	1	1	1	1	0
–4	0	1	1	1	1	0	1
–6	0	1	1	1	1	0	0
–8	0	1	1	1	0	1	1
–10	0	1	1	1	0	1	0
–12	0	1	1	1	0	0	1
–14	0	1	1	1	0	0	0
–16	0	1	1	0	1	1	1
–18	0	1	1	0	1	1	0
–20	0	1	1	0	1	0	1
–22	0	1	1	0	1	0	0
–24	0	1	1	0	0	1	1
–26	0	1	1	0	0	1	0
–28	0	1	1	0	0	0	1
–30	0	1	1	0	0	0	0
		mute front					
–84	0	0	1	1	1	1	0
---				---			---
---				---			---
---				---			---
–84	0	0	1	0	0	0	0

Table 5(b) Fader function rear

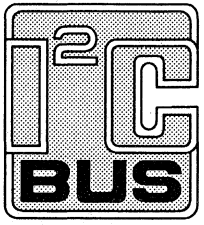
setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	–2	1	0	1	1	1	0
0	–4	1	0	1	1	0	1
0	–6	1	0	1	1	0	0
0	–8	1	0	1	0	1	1
0	–10	1	0	1	0	1	0
0	–12	1	0	1	0	0	1
0	–14	1	0	1	0	0	0
0	–16	1	0	0	1	1	1
0	–18	1	0	0	1	1	0
0	–20	1	0	0	1	0	1
0	–22	1	0	0	1	0	0
0	–24	1	0	0	0	1	1
0	–26	1	0	0	0	1	0
0	–28	1	0	0	0	0	1
0	–30	1	0	0	0	0	0
		mute rear					
0	–84	0	0	1	1	1	0
	---			---			---
	---			---			---
	---			---			---
0	–84	0	0	0	0	0	0

Table 6 Mute control

MUTE control	DATA GMU-bit	remarks
active	1	outputs QLF, QLR, QRF and QRR are muted
passive	0	no general mute

Table 7 Equalizer

equalizer control	DATA EQN-bit	remarks
active	0	signal outputs for equalizer are pins 4 and 17, inputs are pins 6 and 15; Tables 3(b) and 4(b)
passive	1	no general mute; Tables 3(a) and 4(a)



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991

TEA6360
5-band stereo equalizer circuit

FEATURES

- Monolithic integrated 5-band stereo equalizer circuit
- Five filters for each channel
- Centre frequency, bandwidth and maximum boost/cut defined by external components
- Choise for variable or constant Q-factor via I²C software
- Defeat mode
- All stages are DC-coupled
- I²C-bus control for all functions
- Two different modul addresses programmable

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 14)	7	8.5	13.2	V
I_P	supply current	-	24.5	-	mA
$V_{1,32}$	input voltage range	-	2.1 to V_{P-1}	-	V
V_o	maximum output signal level (RMS value, pins 13 and 20)	- 1.1		-	V
G_v	total signal gain, all filters linear	–0.5	-	0	dB
B	-1 dB frequency response (linear)	0 to 20	-	-	kHz
T_{amb}	operating ambient temperature	–40	-	85	°C

GENERAL DESCRIPTION

The 5-band stereo equalizer is an I²C-bus controlled tone processor for application in car radio sets, TV sets and music centres. It offers the possibility of sound control as well as equalization of sound pressure behaviour of different rooms or loudspeakers, especially in cars.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6360	32	shrink DIL	plastic	SOT232
TEA6360/T	32	mini-pack	plastic	SOT287

5-band stereo equalizer circuit TEA6360

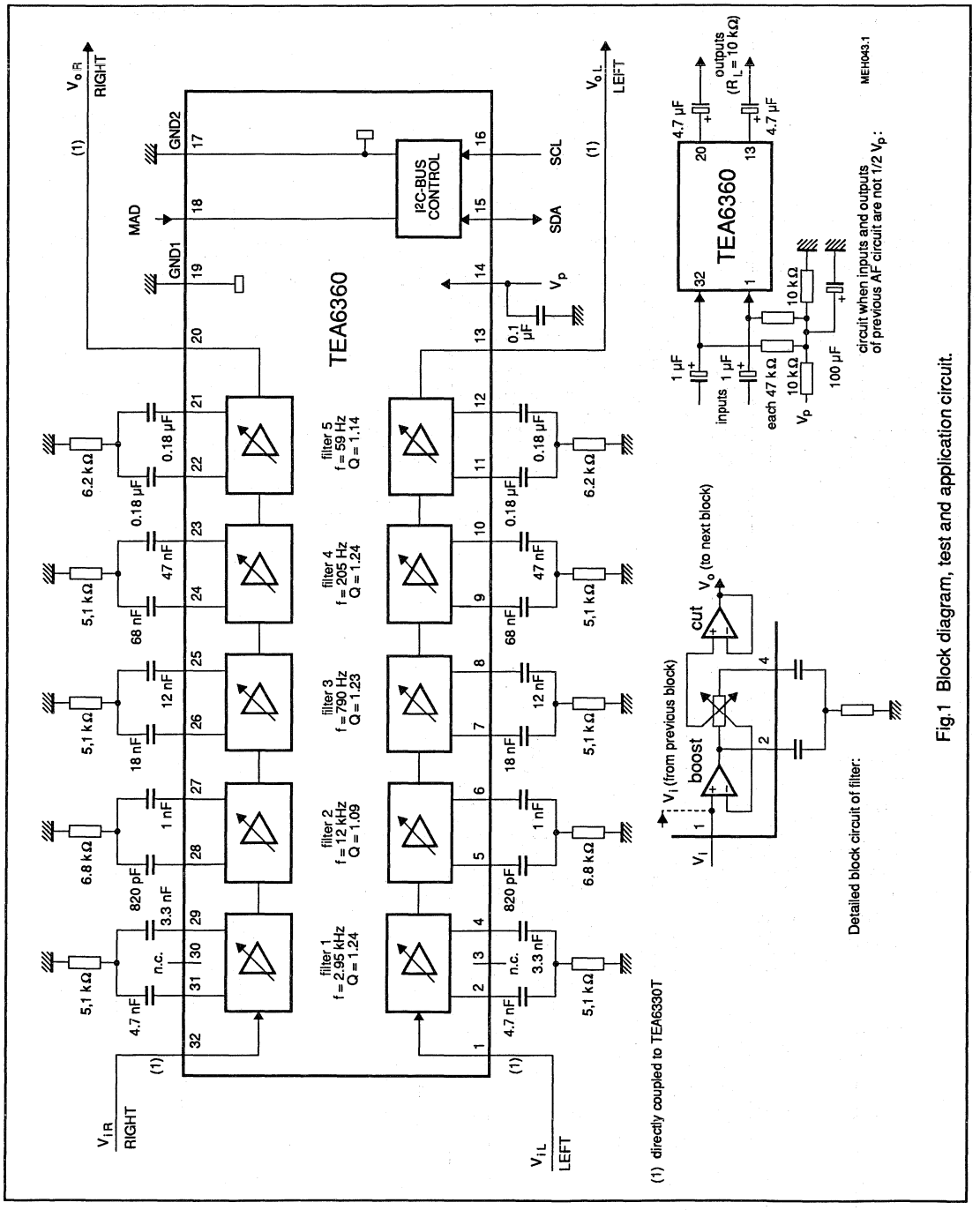


Fig.1 Block diagram, test and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{iL}	1	audio frequency input LEFT
F1LA	2	connection A for filter 1 LEFT (f = 2.95 kHz)
n.c.	3	not connected
F1LB	4	connection B for filter 1 LEFT(f = 2.95 kHz)
F2LA	5	connection A for filter 2 LEFT (f = 12 kHz)
F2LB	6	connection B for filter 2 LEFT (f = 12 kHz)
F3LA	7	connection A for filter 3 LEFT (f = 790 Hz)
F3LB	8	connection B for filter 3 LEFT (f = 790 Hz)
F4LA	9	connection A for filter 4 LEFT (f = 205 Hz)
F4LB	10	connection B for filter 4 LEFT (f = 205 Hz)
F5LA	11	connection A for filter 5 LEFT (f = 59 Hz)
F5LB	12	connection B for filter 5 LEFT (f = 59 Hz)
V_{oL}	13	audio frequency output LEFT
V_P	14	supply voltage (+8.5 V)
SDA	15	I^2C-bus data line
SCL	16	I^2C-bus clock line
GND2	17	ground 2 (I^2C-bus ground)
MAD	18	modul address
GND1	19	ground 1 (analog ground)
V_{oR}	20	audio frequency output RIGHT
F5RB	21	connection B for filter 5 RIGHT (f = 59 Hz)
F5RA	22	connection A for filter 5 RIGHT (f = 59 Hz)
F4RB	23	connection B for filter 4 RIGHT (f = 205 Hz)
F4RA	24	connection A for filter 4 RIGHT (f = 205 Hz)
F3RB	25	connection B for filter 3 RIGHT (f = 790 Hz)
F3RA	26	connection A for filter 3 RIGHT (f = 790 Hz)
F2RB	27	connection B for filter 2 RIGHT (f = 12 kHz)
F2RA	28	connection A for filter 2 RIGHT (f = 12 kHz)
F1RB	29	connection B for filter 1 RIGHT (f = 2.95 kHz)
n.c.	30	not connected
F1RA	31	connection A for filter 1 RIGHT (f = 2.95 kHz)
V_{iR}	32	audio frequency input RIGHT

PIN CONFIGURATION

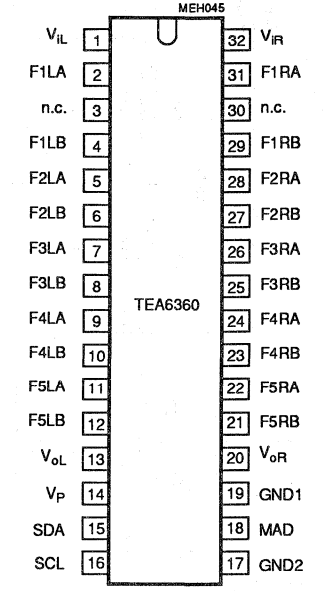


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TEA6360 is performed with two stereo channels (RIGHT and LEFT), each one consists of five equal filter amplifiers (Fig.1).

The centre frequencies for the different filters as well as the bandwidth and the control ranges for boost and cut depend on the external components. Each filter can have different external components but for one definite pair of filters the centre frequency as well as the control range for boost and cut are the same. That means, they have symmetrical curves for boost and cut.

The control range (maximum value in dB) is divided into five steps and one extra step for the linear position.

At maximum gain of 12 dB the typical step resolution is 2.4 dB. The internal resistor chain of each filter amplifier is optimized for 12 dB maximum gain. Therefore the typical gain factors for 15 dB application are as follows:

step 1 = 2.7 dB
step 2 = 5.5 dB
step 3 = 8.4 dB
step 4 = 11.6 dB
step 5 = 15.0 dB

The control of the different filters is obtained by selecting the appropriate subaddress byte (Tab.1). The position of the filter in the left channel and that in the right channel is always the same (stereo). The position of the boost part and the cut part is independently controllable (Tables 2 and 3).

The quality factor of the filter has its maximum in the maximum position (steps 5), if boost (cut on step 0) or cut (boost on step 0) is used. The quality factor decreases also with the step number (variable quality factor). In this mode the control pattern are according to Table 4.

A different control is necessary to achieve a constant quality factor over the whole control range. For boost with a constant quality factor over the boost range position +5 is selected and boost control is then performed using cut. This control technique is applied to the cut range with position –5 selected and the boost is varied (Table 5).

The cut part has to follow the boost part in each filter for economic reasons. So the signal is first amplified and then attenuated. This has to be taken into account for the internal level diagram in case of constant quality factor. This may result in a mode between constant Q and non-constant Q mode; for example for the position +2 it is not necessary to amplify by step +5 and then attenuate by –3 step. The combination of step +4 and step –2 to reach position +2 is a good result (quasi constant quality factor, Table 6).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 19, 28 and 43 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)	0	13.2	V
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–40	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins		±500	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 8.5 V; f_i = 1 kHz (R_S = 600 Ω), R_L = 10 kΩ, T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 14)		7	8.5	13.2	V
I_P	supply current (pin 14)	V_P = 8.5 V	-	25.5	-	mA
		V_P = 12 V	-	26.0	-	mA
Analog part						
R_i	input resistor (pins 1 and 32)		1	-	-	MΩ
$V_{1,32}$	input voltage range at any stage		2.1 to V_P–1	-	-	V
$V_{13,20}$	output voltage range at any stage		1.0 to V_P–1	-	-	V
V_o	output signal level (RMS value, pins 13 and 20)	control range 0 to +5, variable Q-factor or quasi constant Q-factor	1.1	-	-	V
R_o	output resistor (pins 13 and 20)		-	100	-	Ω
R_L	admissable load resistance at outputs (pins 13 and 20)		2	-	-	kΩ
C_L	admissable load capacitance at outputs (pins 13 and 20)		-	-	2.5	nF
G_v	total signal gain ($G = V_o / V_i$)	all filters linear	–0.5	-	0	dB
B	frequency response	all filters linear, roll off frequency for –1 dB				
	minimum value	(DC-coupled)	0	-	-	Hz
	maximum value		20	-	-	kHz
α_{Cr}	crosstalk attenuation between channels	f = 250 to 10000 Hz				
	all filters linear		60	75	-	dB
	all filters maximum boost		55	-	-	dB
	all filters maximum cut		55	-	-	dB
THD	distortion (pins 13 and 20)	f = 20 to 12500 Hz V_P = 8.5 to 12 V				
	$V_{o\ (rms)}$ = 1.1 V	all filters linear	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 0.1 V	all filters linear	-	0.05	0.2	%
	$V_{o\ (rms)}$ = 1.1 V	all filters max. boost	-	0.5	1.0	%
	$V_{o\ (rms)}$ = 0.1 V	all filters max. boost	-	0.1	0.3	%
	$V_{o\ (rms)}$ = 0.1 V	all filters maximum cut	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 1 V	all filters max. boost f = 1 kHz	-	-	0.35	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_N	weighted output noise voltage (RMS value)	CCIR 468-3, maximum gain/filter of 12 dB				
	defeat mode		-	8	16	µV
	all filters linear		-	23	46	µV
	all filters maximum boost		-	70	140	µV
	all filters maximum cut		-	23	46	µV
α_{Cr}	crosstalk between bus inputs and signal outputs, 20 log (V_{bus} (p-p) / V_o rms)	all filters linear	-	120	-	dB
RR	ripple rejection at V_{ripple} rms < 200 mV	all filters linear				
	for f = 100 Hz		-	70	-	dB
	for f = 40 to 12500 Hz		-	60	-	dB
Internal filters of analog part						
Q	Q-factor dependent on maximum gain					
	maximum gain 10 dB		0.1	-	1.2	
	maximum gain 12 dB		0.1	-	1.4	
	maximum gain 15 dB		0.1	-	1.8	
R_{tot}	total resistor of different filter sections		29.6	37.0	44.4	kΩ
ΔR_{tot}	tolerance between any filter section		-	-	±4	%
Internal controls of analog part via I²C-bus						
Step	number of steps for boost or for cut		-	5	-	
	position for linear		-	1	-	
	step resolution	maximum gain 12 dB	-	2.4	-	dB
	step set error		-	0.5	-	dB
ΔV_o	DC offset between any step or neighbouring step or defeat		-	-	±10	mV
I²C-bus control SDA and SCL (pins 15 and 16)						
V_{IH}	input level HIGH		3	-	V_P	V
V_{IL}	input level LOW		0	-	1.5	V
I_I	input current		-	-	±10	µA
V_{ACK}	acknowledge voltage on SDA	I_{15} = 3 mA at LOW	-	-	0.4	V
Module address bit (pin 18)						
V_{IH}	input level HIGH for address 1000 0110		3	-	V_P	V
V_{IL}	input level LOW for address 1000 0100		0	-	1.5	V
I_I	input current		-	-	±10	µA
Power on reset: When reset is active the DEF-bit (defeat) is set and the I²C-bus receiver is in reset position.						
RESET	start of reset	increasing V_P	-	-	2.5	V
		decreasing V_P	4.2	5.0	5.8	V
	end of reset	increasing V_P	5.2	6.0	6.8	V

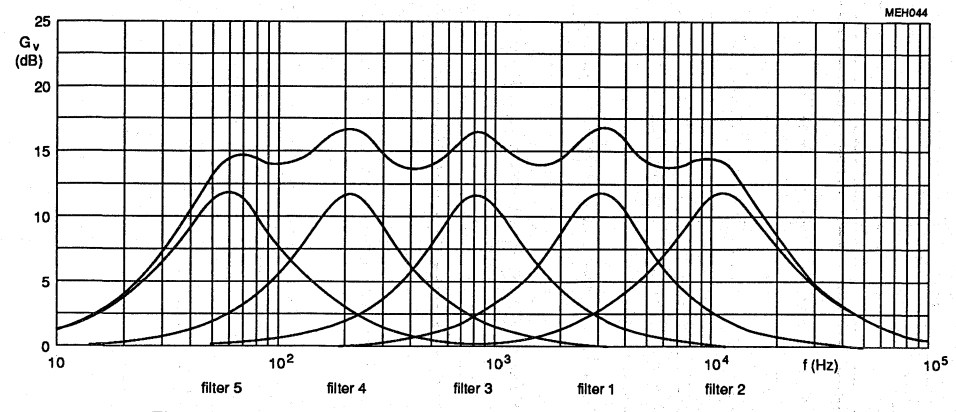


Fig.3 Frequency response for maximum boost of +12 dB according to Fig.1. For maximum cut the curves are symmetrical to negative gain values.

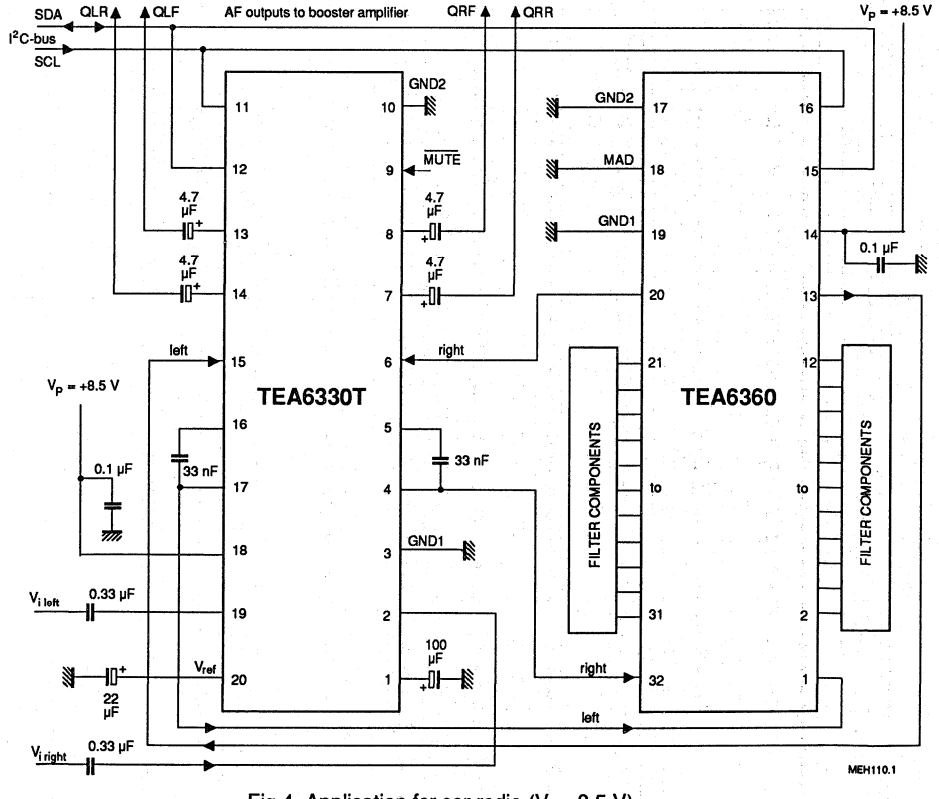


Fig.4 Application for car radio (V_P <8.5 V).

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 0100** when pin 18 is set LOW
or **1000 0110** when pin 18 is set HIGH or open-circuit
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission.

function	subaddress byte								data byte D7	D6	D5	D4	D3	D2	D1	D0
filter 1 /defeat	0	0	0	0	0	0	0	0	DEF	1B2	1B1	1B0	0	1C2	1C1	1C0
filter 2	0	0	0	0	0	0	0	1	0	2B2	2B1	2B0	0	2C2	2C1	2C0
filter 3	0	0	0	0	0	0	1	0	0	3B2	3B1	3B0	0	3C2	3C1	3C0
filter 4	0	0	0	0	0	0	1	1	0	4B2	4B1	4B0	0	4C2	4C1	4C0
filter 5	0	0	0	0	0	1	0	0	0	5B2	5B1	5B0	0	5C2	5C1	5C0

Function of the bits of Table 1:

1B0 to 1B2 boost control for filter 1
1B0 to 1B2 cut control for filter 1
2B0 to 2B2 boost control for filter 2
2B0 to 2B2 cut control for filter 2
3B0 to 3B2 boost control for filter 3
3B0 to 3B2 cut control for filter 3
4B0 to 4B2 boost control for filter 4
4B0 to 4B2 cut control for filter 4
5B0 to 5B2 boost control for filter 5
5B0 to 5B2 cut control for filter 5

DEF
DEF = 0 (defeat bit): All filters operating.
DEF = 1 : Linear frequency response, input is directly connected to the output of the output amplifier. The filter settings are stored but the internal amplification is controlled to 0 dB, independent on bits nB2 to nB0.

Table 2 Boost control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no boost)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum boost)	1	0	1
step 5	(maximum boost)	1	1	0
step 5	(maximum boost)	1	1	1

Table 3 Cut control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no cut)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum cut)	1	0	1
step 5	(maximum cut)	1	1	0
step 5	(maximum cut)	1	1	1

Table 4 Filter control with variable quality factor

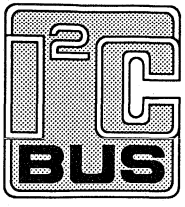
position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	0	0	0	0	0	(+4) + (−0) = +4
+3	0	0	1	1	0	0	0	0	(+3) + (−0) = +3
+2	0	0	1	0	0	0	0	0	(+2) + (−0) = +2
+1	0	0	0	1	0	0	0	0	(+1) + (−0) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	0	0	0	0	0	1	(+0) + (−1) = −1
−2	0	0	0	0	0	0	1	0	(+0) + (−2) = −2
−3	0	0	0	0	0	0	1	1	(+0) + (−3) = −3
−4	0	0	0	0	0	1	0	0	(+0) + (−4) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 5 Filter control with constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	1	0	0	1	1	(+5) + (−3) = +2
+1	0	1	0	1	0	1	0	0	(+5) + (−4) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	1	0	0	0	1	0	1	(+4) + (−5) = −1
−2	0	0	1	1	0	1	0	1	(+3) + (−5) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 6 Filter control with quasi-constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	0	0	0	1	0	(+4) + (−2) = +2
+1	0	0	1	1	0	0	1	0	(+3) + (−2) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	1	0	0	0	1	1	(+2) + (−3) = −1
−2	0	0	1	0	0	1	0	0	(+2) + (−4) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5



RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I^2C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

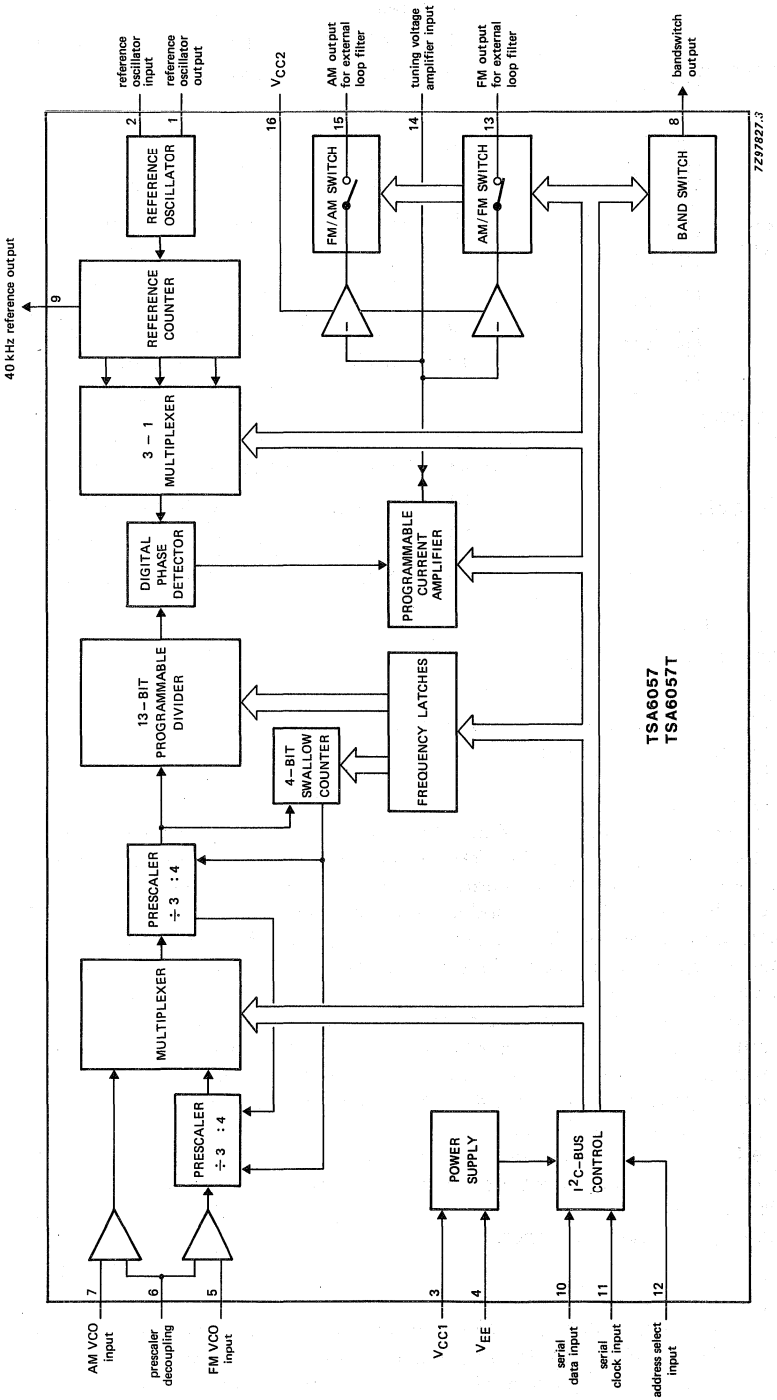


Fig.1 Block diagram.

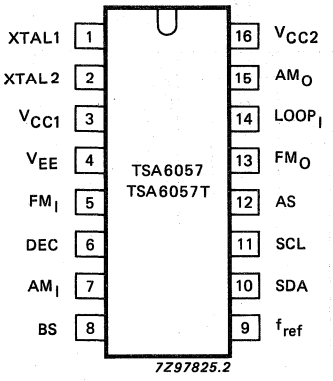


Fig.2 Pinning diagram.

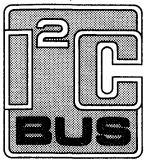
PINNING

1	XTAL1	reference oscillator output	
2	XTAL2	reference oscillator input	
3	V_{CC1}	positive supply voltage	
4	V_{EE}	ground	
5	FM_I	FM VCO input	
6	DEC	prescaler decoupling	
7	AM_I	AM VCO input	
8	BS	bandswitch output	
9	f_{ref}	40 kHz reference output	
10	SDA	serial data input	I^2C-bus
11	SCL	serial clock input	I^2C-bus
12	AS	address select input	I^2C-bus
13	FM_O	FM output for external loop filter	
14	$LOOP_I$	tuning voltage amplifier input	
15	AM_O	AM output for external loop filter	
16	V_{CC2}	positive supply voltage	

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I^2C-bus interface with data latches and control logic. The I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C-bus specification is available on request.
- A software-controlled bandswitch output.



FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I²C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I²C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

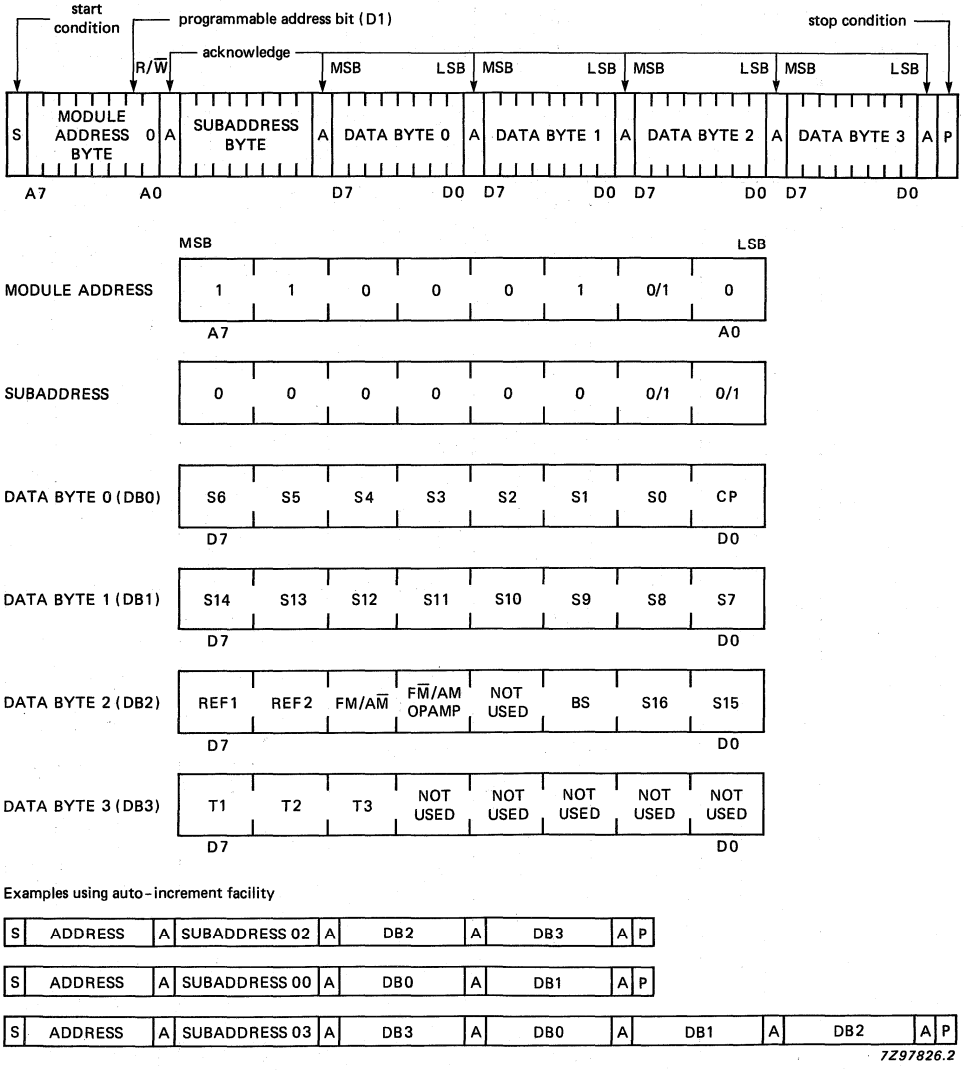


Fig.3 Bit organization.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I²C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

SENSITIVITY MEASUREMENT

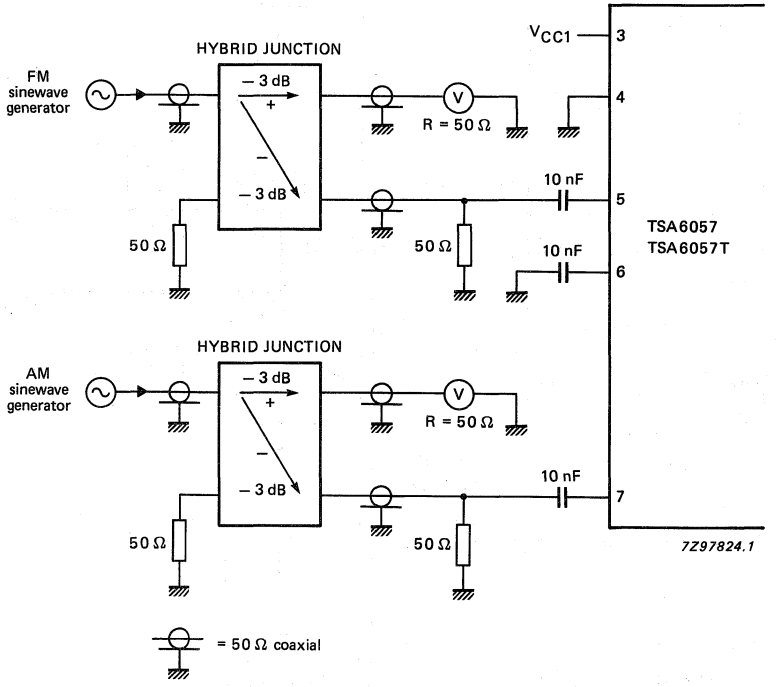


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

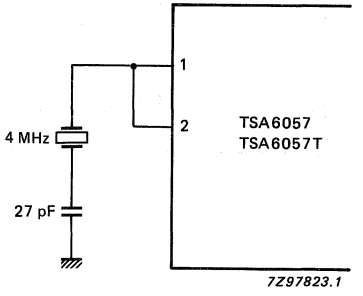


Fig.5 Crystal connection (4 MHz).

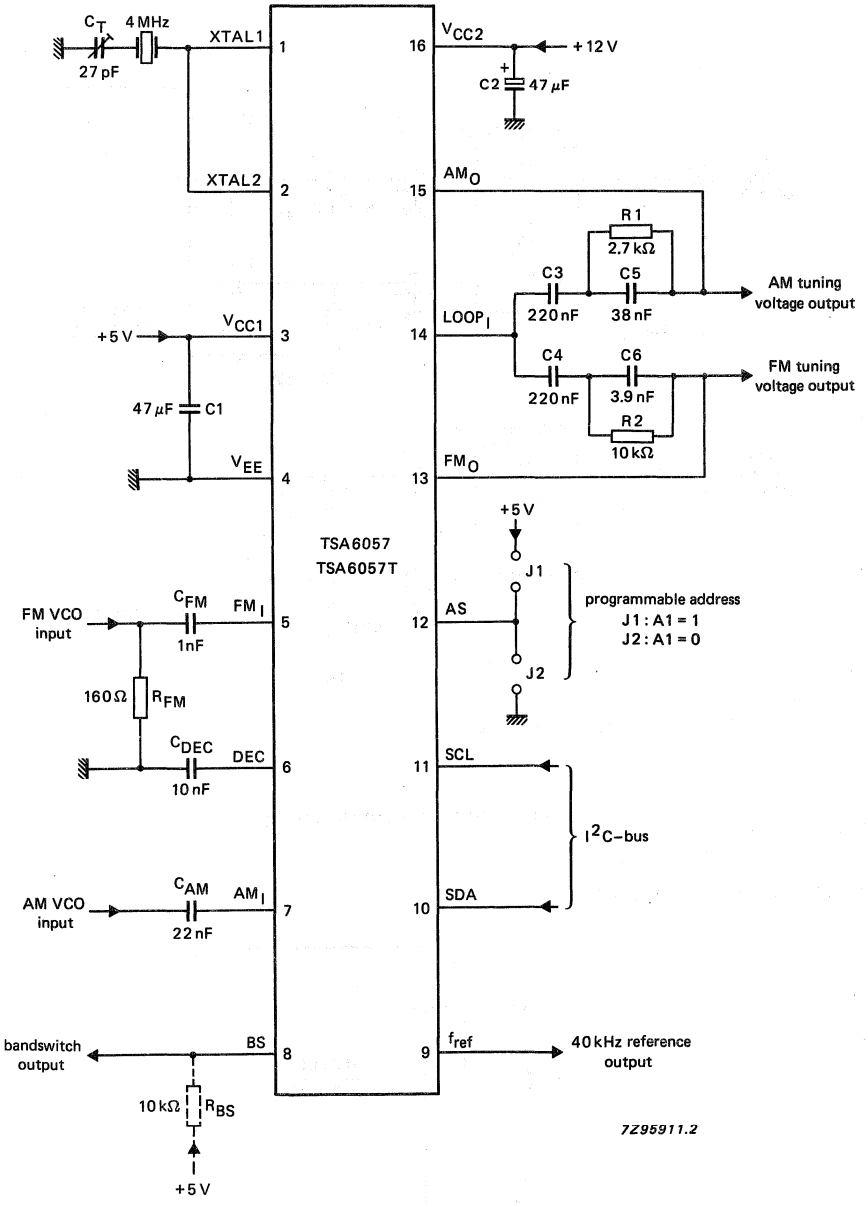


Fig.6 Application diagram

Receiver IC for infrared remote control (including photo-diode)

TSA9036/TSA9037

GENERAL DESCRIPTION

The TSA9036 and TSA9037 are remote control receivers containing, in the same package SOT294, a pin photo-diode and a bipolar integrated circuit. The photo-diode has 5 mm² sensitive area. The bipolar IC is designed to perform all filter, amplifier and pulse shaping functions required for a fully integrated IR-receiver. The typical signals sent from a IR-transmitter may be biphase coded (e.g. RC5) or pulse distance coded (RECS 80), based on a infrared wavelength of 950 ± 70 nm.

FEATURES

- Coded optical signal reception.
- On board voltage reference and ripple rejection.
- Automatic bias level control input stage providing rejection of sunlight and incandescent lamp interferences.
- Limiter.
- Band-pass filter with internal capacitors.
- Amplifiers with controlled gain (AGC) by means of an external capacitor.
- Pulse shaper.
- Active LOW output (TSA9036).
- Active HIGH output (TSA9037).

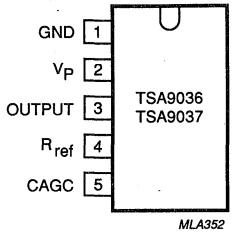


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	4.5	5.0	5.5	V
I_P	supply current (see note 1)	-	-	2.2	mA
f_o	carrier frequency	-	36	-	kHz
T_{amb}	operating ambient temperature range	0	-	+85	°C

Note

1. In complete darkness without load on output.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_P	2	supply voltage
OUTPUT	3	output signal
R_{ref}	4	reference voltage and current input
CAGC	5	AGC control

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA9036, TSA9037	5	SIL	plastic	SOT294

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–0.3	6.5	V
V_O	output voltage		–0.3	6.5	V
I_O	output current DC		-	note 1	mA
P_d	total power dissipation		-	note 1	mW
T_{stg}	storage temperature range		–40	+85	°C
T_{amb}	operating ambient temperature range		0	+85	°C
T_j	operating junction temperature		-	150	°C

Note

1. Value to be fixed.

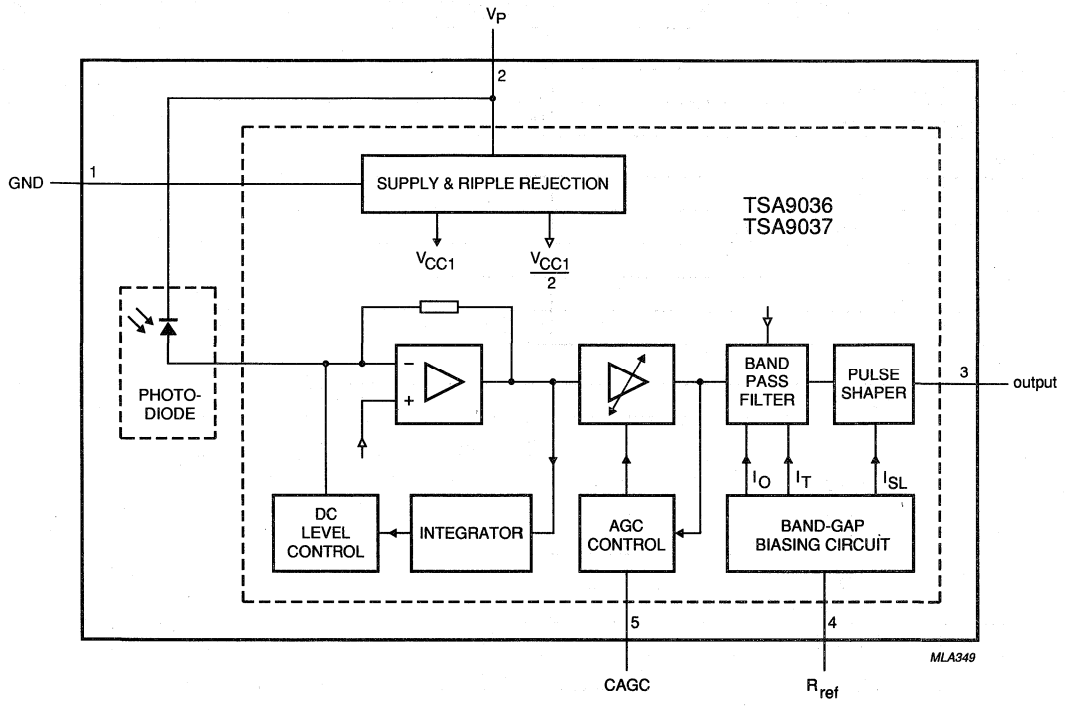


Fig.2 Block diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	note 1	-	-	note 4	mA
Input stage						
-	DC voltage		-	1.4	-	V
-	compensated DC signal		-	-	3	mA
-	AC signal		-	note 4	-	
Z_i	imput impedance		-	note 4	-	
-	sensitivity	note 2	-	note 4	-	nA
Band-pass filter						
f_0	centre frequency		-	36	-	kHz
$\left\|\frac{\Delta\phi_0}{f_0}\right\|$	tolerance on f_0	R_{ref} = note 4	-	15	-	%
BW	bandwidth (–3 dB)		-	note 4	-	MHz
AGC detector						
V_{AGC}	control voltage		note 4	-	note 4	V
A_{AGC}	AGC control range		55	60	65	dB
t_{attack}	attack time, see Fig.3	CAGC = note 4	-	150	-	µs
t_{hold}	hold time see, Fig.3	CAGC = note 4	-	10	-	ms
Optical sensitivity						
E_e	irradiance	note 3	-	0.25	0.5	mW/m²
Output						
V_{OH}	signal output voltage, HIGH		3.5	-	-	V
I_{OH}	signal output current, HIGH		–200	-	-	µA
V_{OL}	output voltage , LOW		0	-	0.8	V
I_{OL}	signal output current, LOW		-	-	1	mA
Switching time (see Fig.4)						
t_r	rise time	C_L = 15 pF	-	note 4	-	ns
t_f	fall time	C_L = 15 pF	-	note 4	-	ns

Notes

1. In complete darkness without load on output.
2. Peak value of current pulses at f_0 necessary to create correct data at the output. Duty factor = 50%; I_{DC} = 0.
3. The receiver sensitivity is the irradiance E_e (radiometric) necessary to create a correct data output (according to UAW 0422 par.4 at 0 deg off-axis).
4. Value to be fixed.

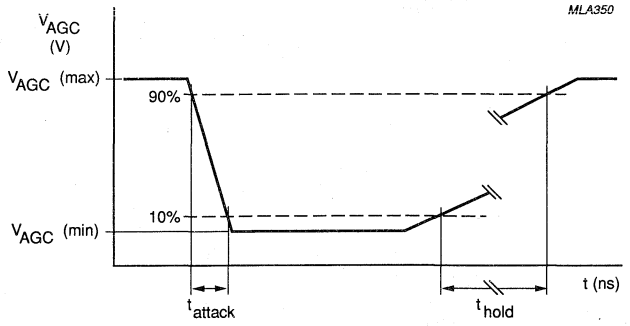


Fig.3 AGC attack and hold times.

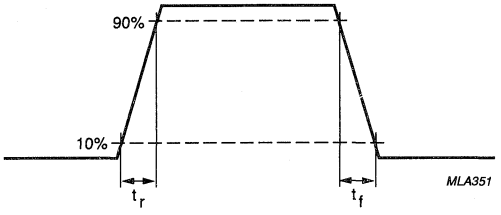


Fig.4 Switching times with a C_L = 15 pF at the output.

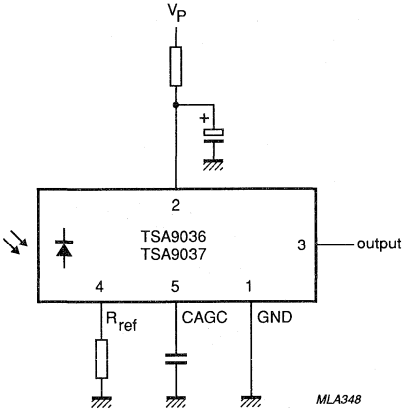


Fig.5 Typical application diagram.

Receiver IC for infrared remote control

TSA9455/TSA9456

GENERAL DESCRIPTION

The TSA9455 and TSA9456 are bipolar IC's designed to perform all filter, amplifier and pulse shaping functions required for a fully integrated IR-receiver. The typical signal sent from a IR-transmitter may be biphase coded or pulse distance coded.

FEATURES

- On board voltage reference and ripple rejection.
- Automatic bias level control input stage providing rejection of sunlight and incandescent lamp interferences.
- Limiter.
- Band-pass filter with internal capacitors.
- Amplifiers with controlled gain (AGC) by means of an external capacitor.
- Pulse shaper.
- LS-TTL compatible output buffer.
- Active HIGH output (TSA9455).
- Active LOW output (TSA9456).

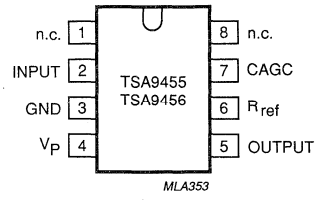


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	4	4.5	5	V
I_P	supply current (see note 1)	-	-	2.2	mA
f_o	carrier frequency	-	455	-	kHz
T_{amb}	operating ambient temperature range	–40	-	+85	°C

Note

1. When the output is not loaded.

PINNING

SYMBOL	PIN	DESCRIPTION
-	1	n.c.
INPUT	2	input signal
GND	3	ground
V_P	4	supply voltage
OUTPUT	5	output signal
R_{ref}	6	reference voltage and current input
CAGC	7	AGC control
-	8	n.c.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA9455, TSA9456	8	DIL	plastic	SOT96A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–0.3	6.5	V
V_O	output voltage		–0.3	6.5	V
I_O	output current DC		-	note 1	mA
P_d	total power dissipation		-	note 1	mW
T_{stg}	storage temperature range		–40	+85	°C
T_{amb}	operating ambient temperature range		–40	+85	°C
T_j	operating junction temperature		-	150	°C

Note

1. Value to be fixed.

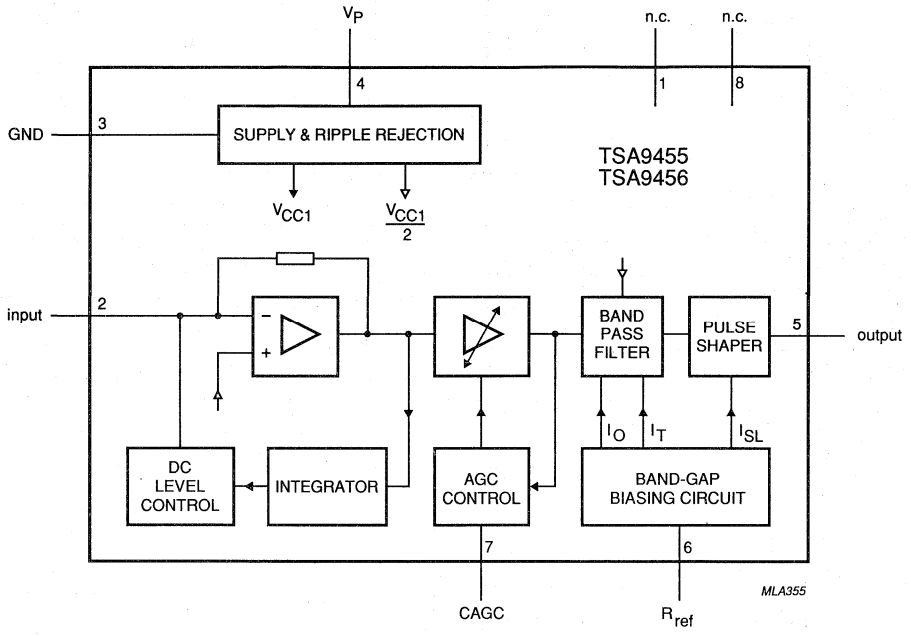


Fig.2 Block diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4	4.5	5	V
I_P	supply current		-	-	note 2	mA
Input stage						
-	DC voltage		-	1.4	-	V
-	compensated DC signal		-	-	3	mA
-	AC signal		-	note 2	-	
Z_i	imput impedance		-	note 2	-	
-	sensitivity	note 1	-	note 2	-	nA
Band-pass filter						
f_0	centre frequency		-	455	-	kHz
$\left\lvert\frac{\Delta\phi_0}{f_0}\right\rvert$	tolerance on f_0	R_{ref} = note 2	-	15	-	%
BW	bandwidth (–3 dB)		-	note 2	-	MHz
AGC detector						
V_{AGC}	control voltage		note 2	-	note 2	V
A_{AGC}	AGC control range		55	60	65	dB
t_{attack}	attack time, see Fig.3	CAGC = note 2	-	10	-	µs
t_{hold}	hold time see, Fig.3	CAGC = note 2	-	1	-	ms
Output						
V_{OH}	signal output voltage, HIGH		3	-	-	V
I_{OH}	signal output current, HIGH		–200	-	-	µA
V_{OL}	output voltage , LOW		0	-	0.4	V
I_{OL}	signal output current, LOW		-	-	1	mA
Switching time (see Fig.4)						
t_r	rise time	C_L = 15 pF	-	note 2	-	ns
t_f	fall time	C_L = 15 pF	-	note 2	-	ns

Notes

1. Peak value of current pulses at f_0 necessary to create correct data at the output. Duty factor = 50%; I_{DC} = 0.
2. Value to be fixed.

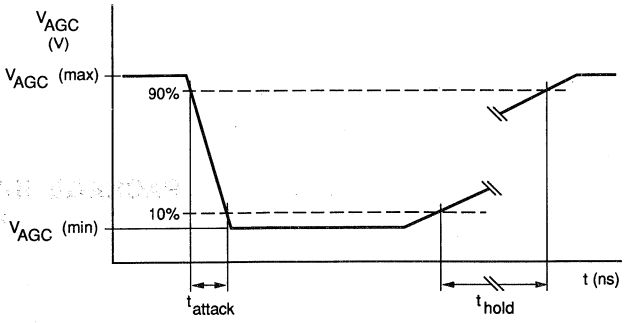


Fig.3 AGC attack and hold times.

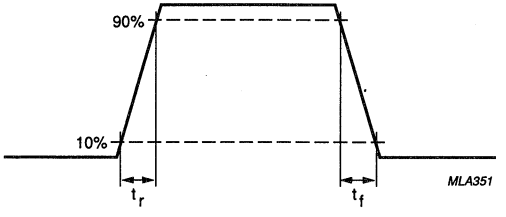


Fig.4 Switching times with a C_L = 15 pF at the output.

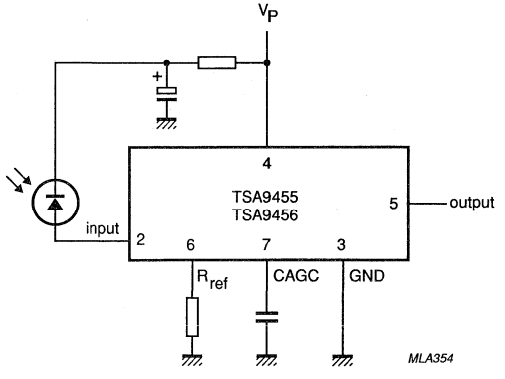


Fig.5 Typical application diagram.

PACKAGE INFORMATION

Package outlines
Soldering

Package outlines

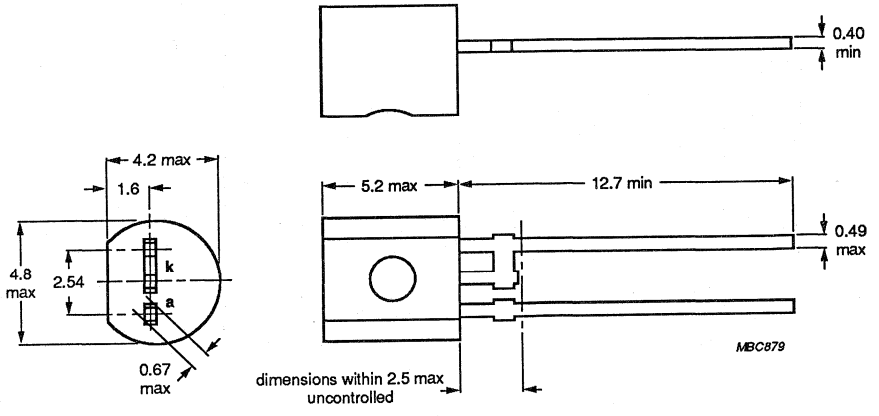
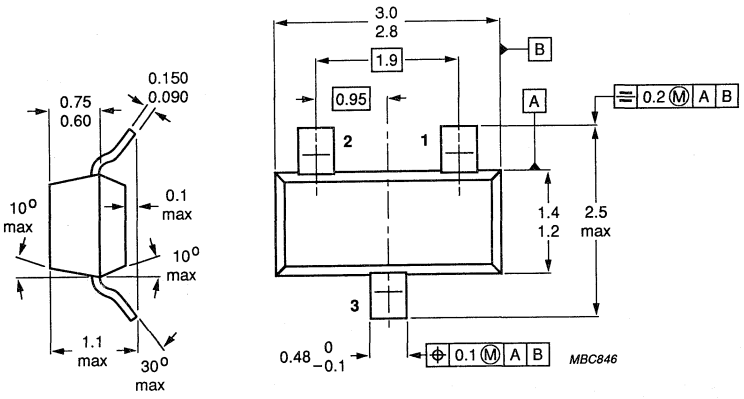


Fig.1 SOD69.

Package outlines



TOP VIEW

Fig.2 SOT23.

Package outlines

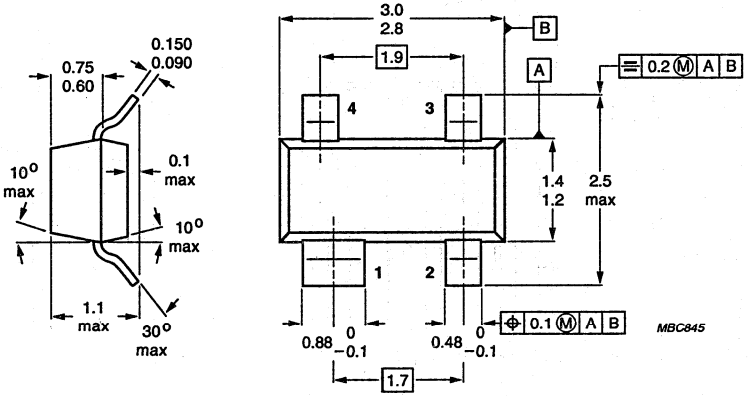
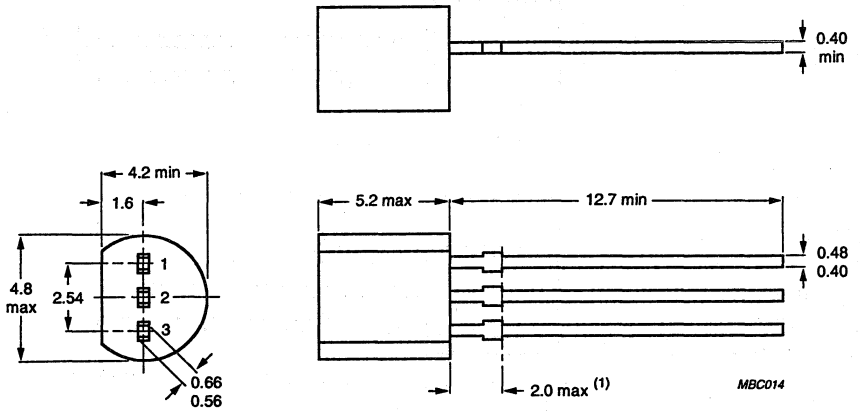


Fig.3 SOT143B.

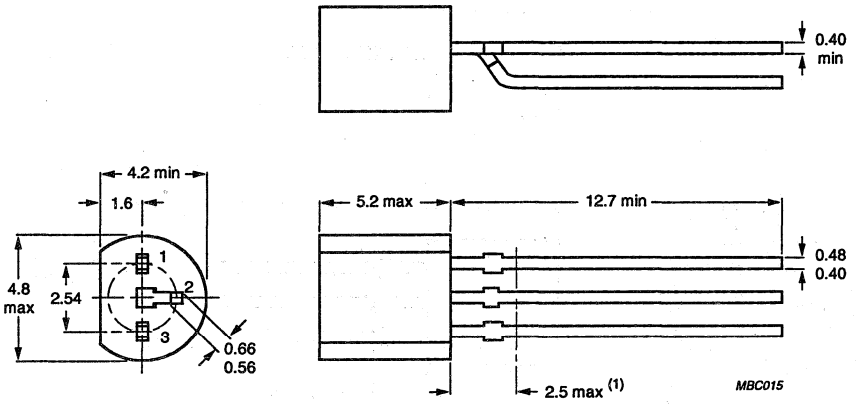
Package outlines



1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.4 TO92.

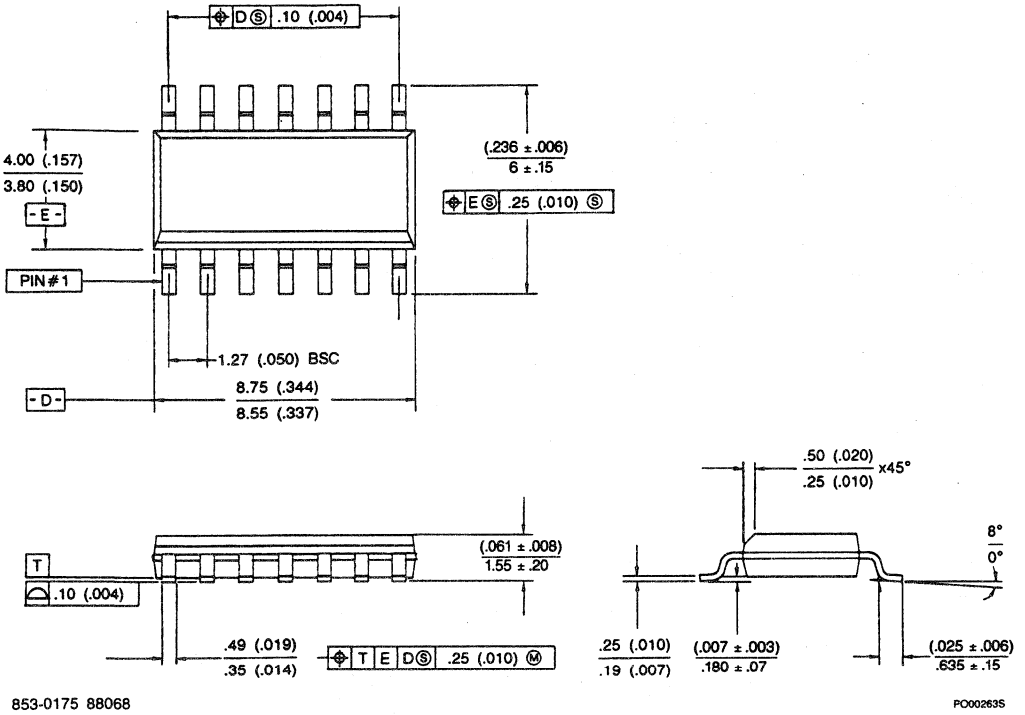
Package outlines



1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.5 TO92 (variant).

Package outlines

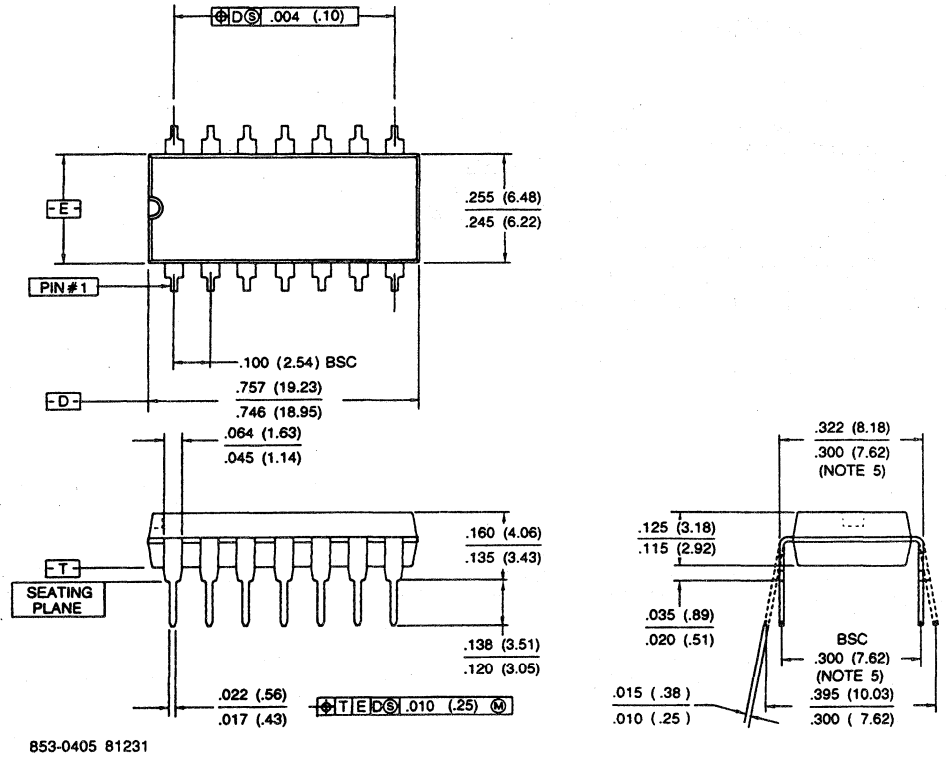


NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Fig.6 14-pin plastic SO (D package).

Package outlines

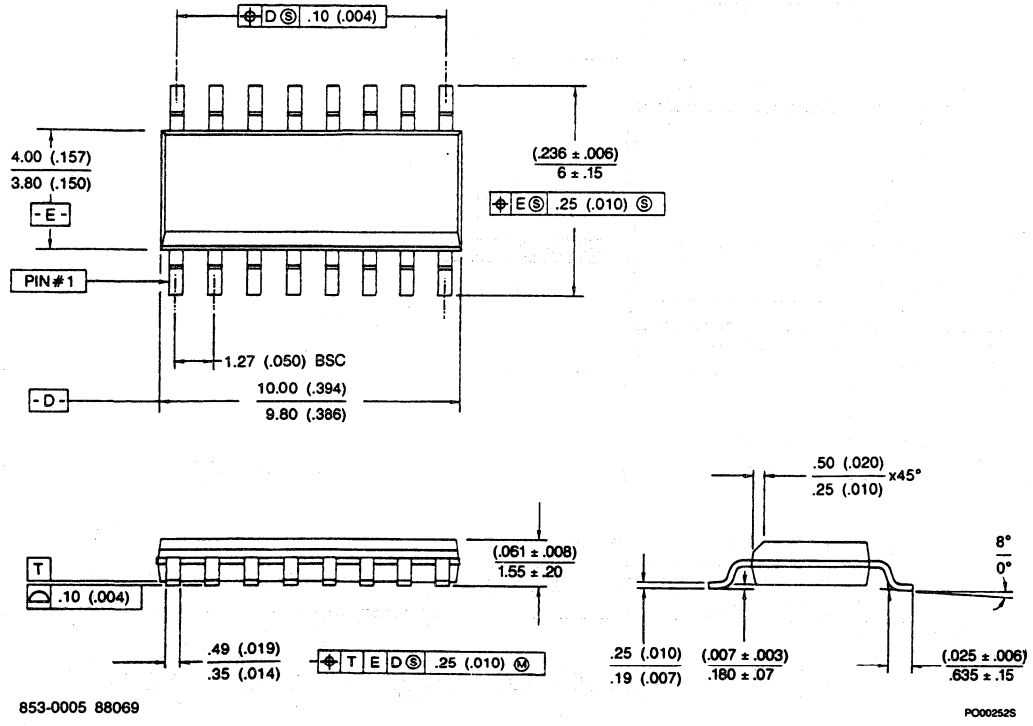


NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

Fig.7 14-pin plastic DIP (N package).

Package outlines

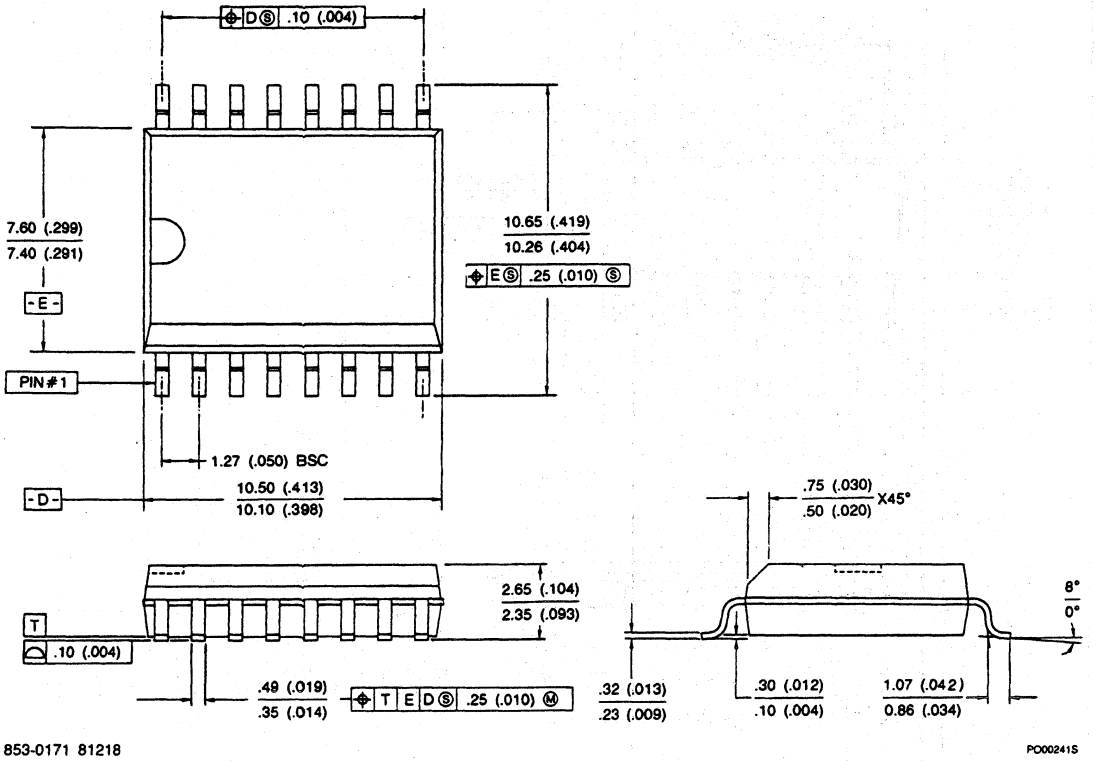


NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Fig.8 16-pin plastic SO (D package).

Package outlines

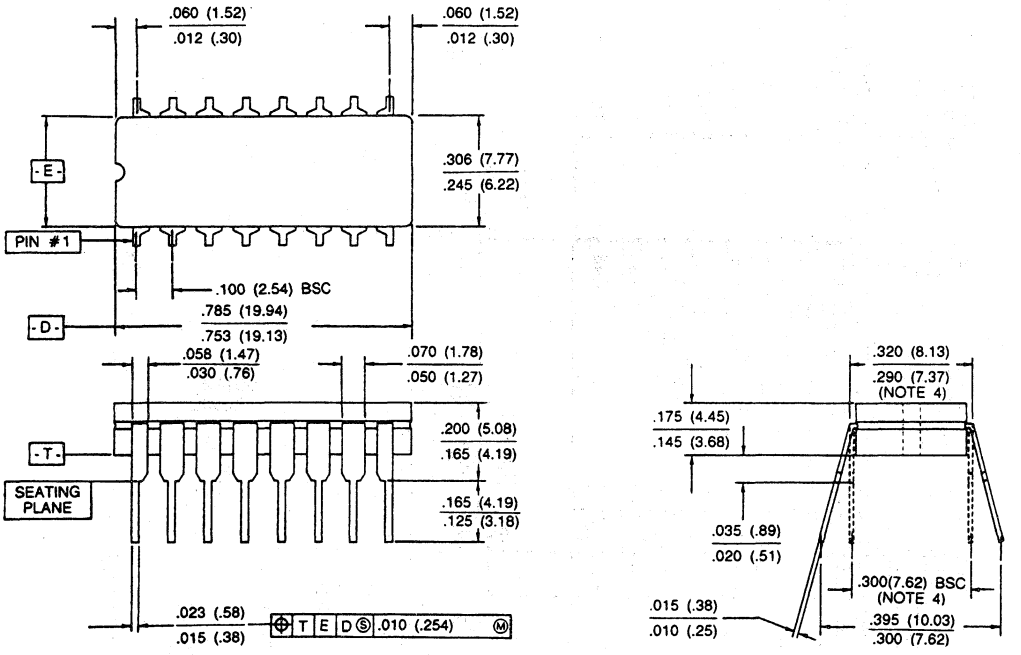


NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Fig.9 16-pin plastic SOL (D package).

Package outlines



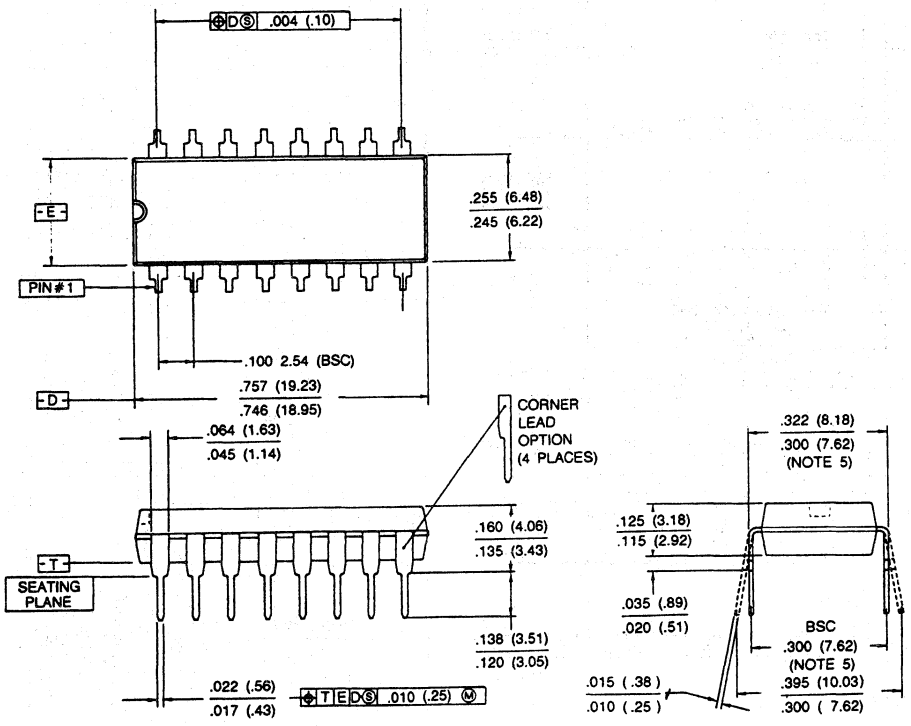
853-0582 81594

NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Fig.10 16-pin cerdip (F package).

Package outlines



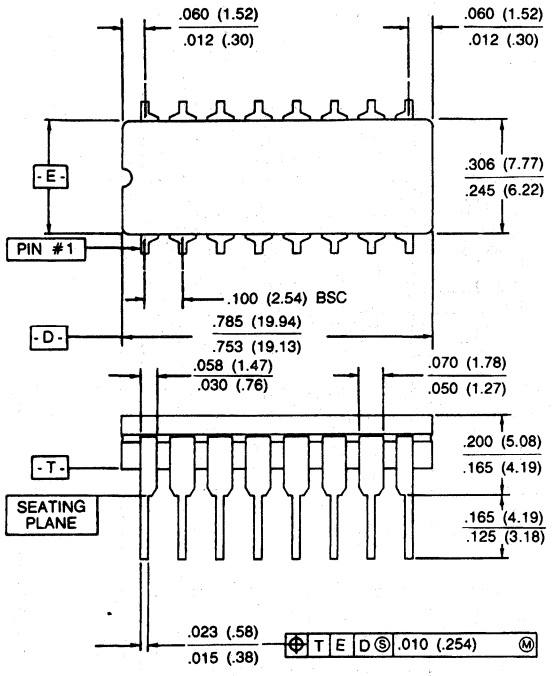
853-0406 81232

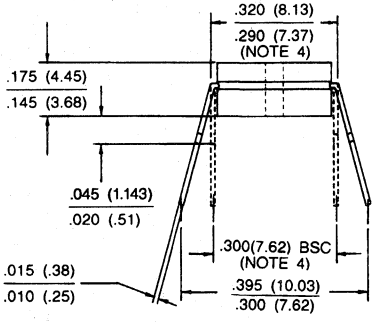
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Fig.11 16-pin plastic DIP (N package).

Package outlines





FJ1 853-0582 88375

PO00491S

NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Fig.12 16-pin plastic cerdip (F package).

Package outlines

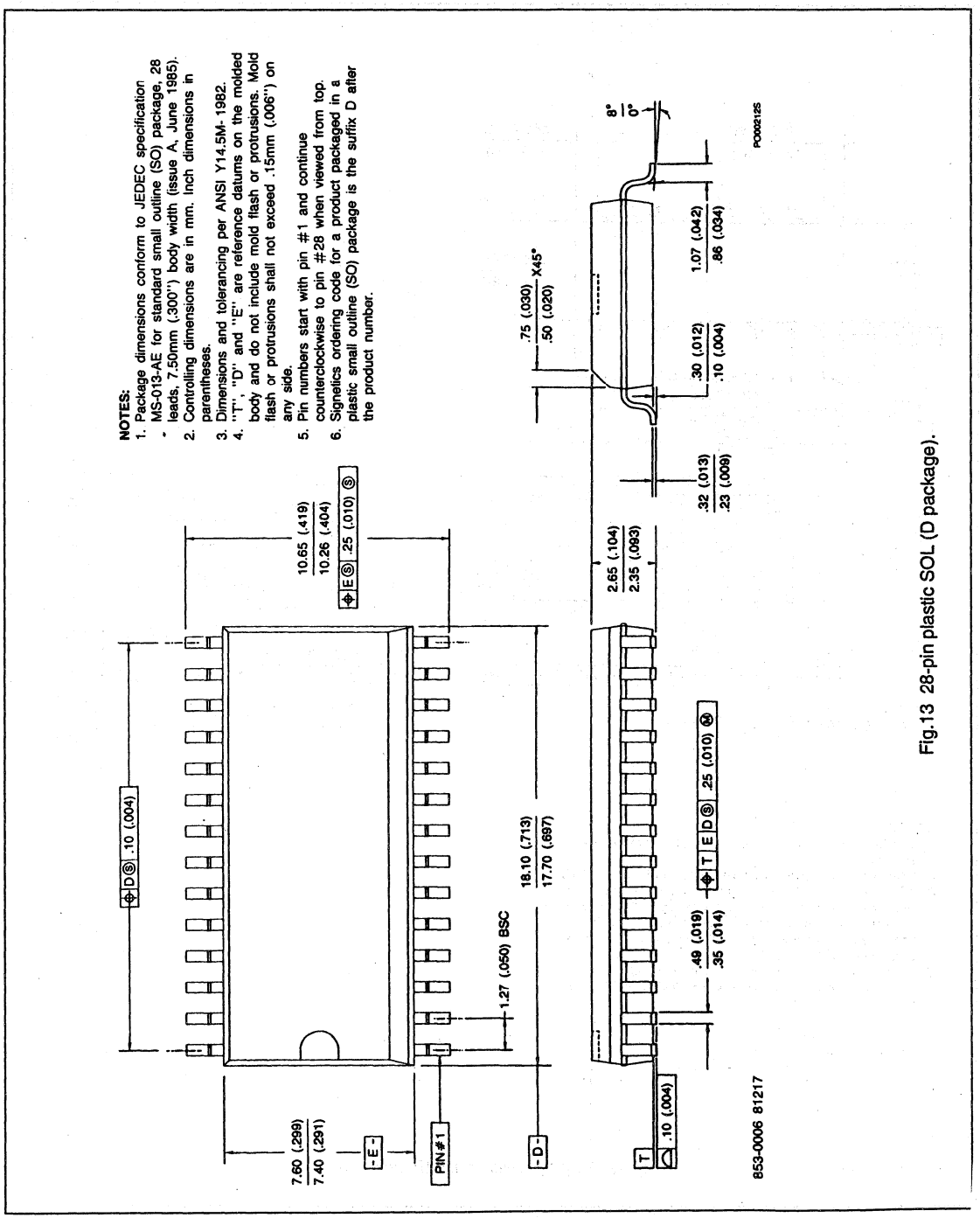
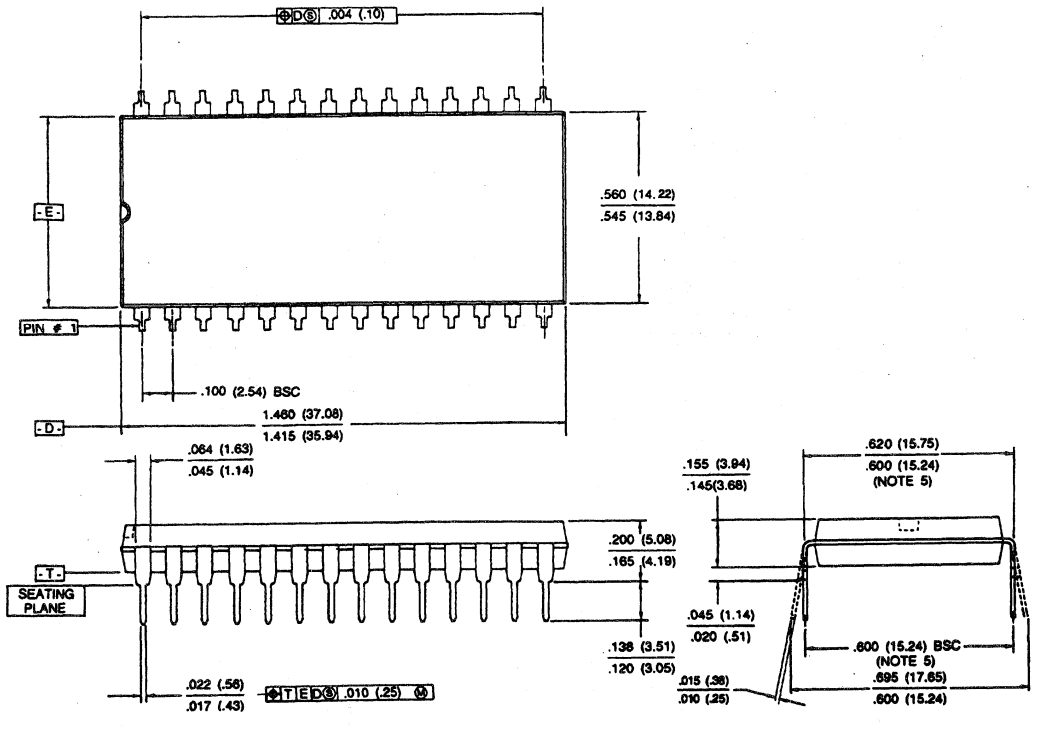


Fig.13 28-pin plastic SOL (D package).

Package outlines

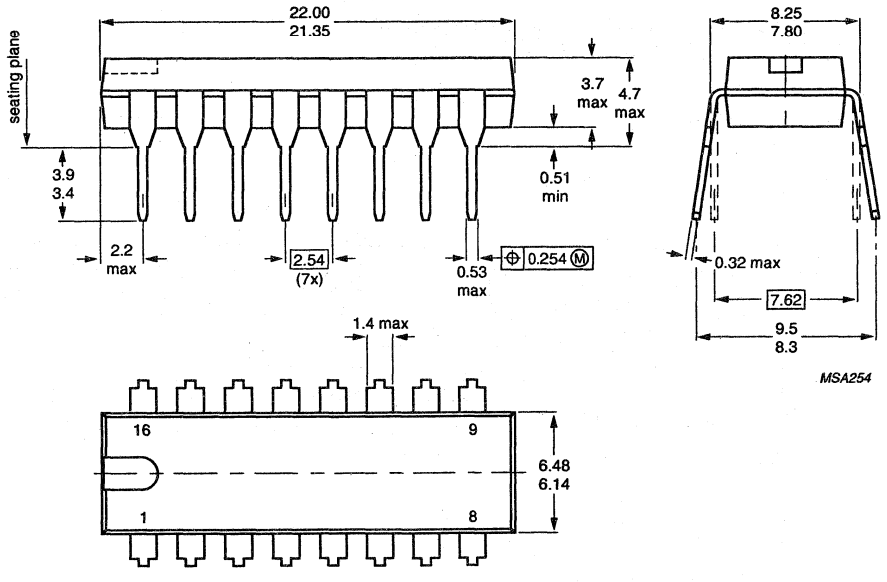


NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

Fig.14 28-pin plastic DIP (N package).

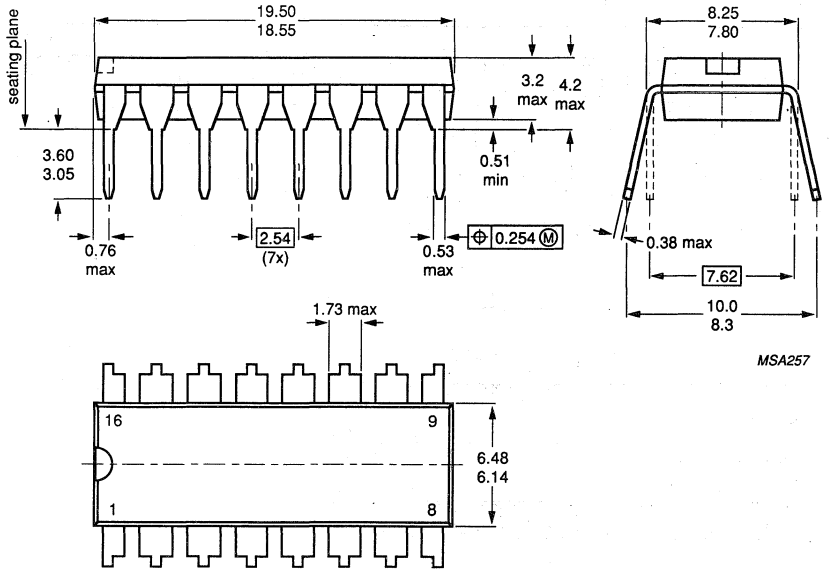
Package outlines



Dimensions in mm.

Fig.15 Dual in-line, 16-pin (DIL-1) (SOT38GE, GG).

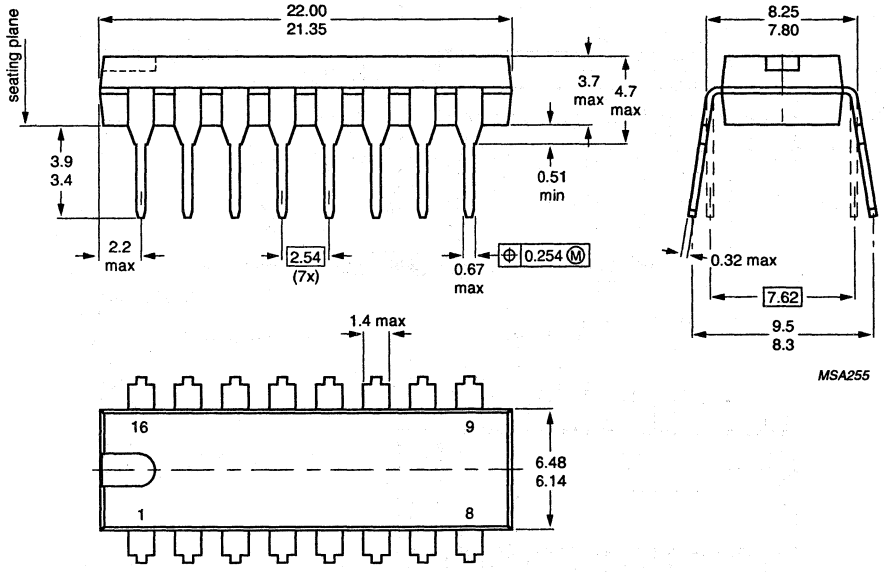
Package outlines



Dimensions in mm.

Fig.16 Dual in-line, 16-pin (DIL) (SOT38DF).

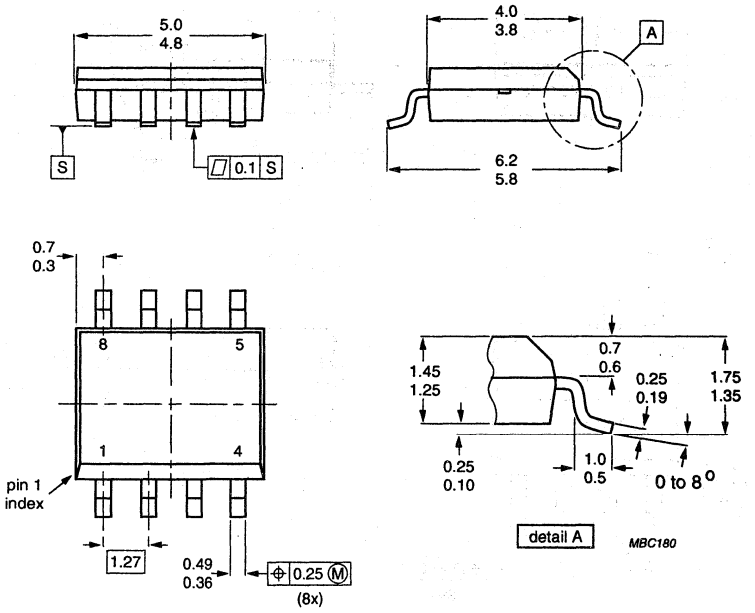
Package outlines



Dimensions in mm.

Fig.17 Dual in-line, 16-pin (DIL-3) (SOT38AG).

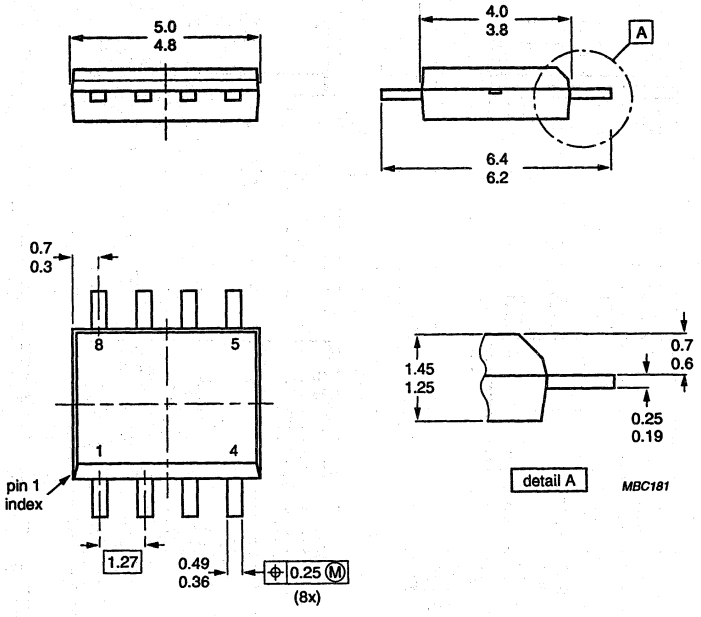
Package outlines



Dimensions in mm.

Fig.18 SO, plastic, 8-pin (SO8) (SOT96A).

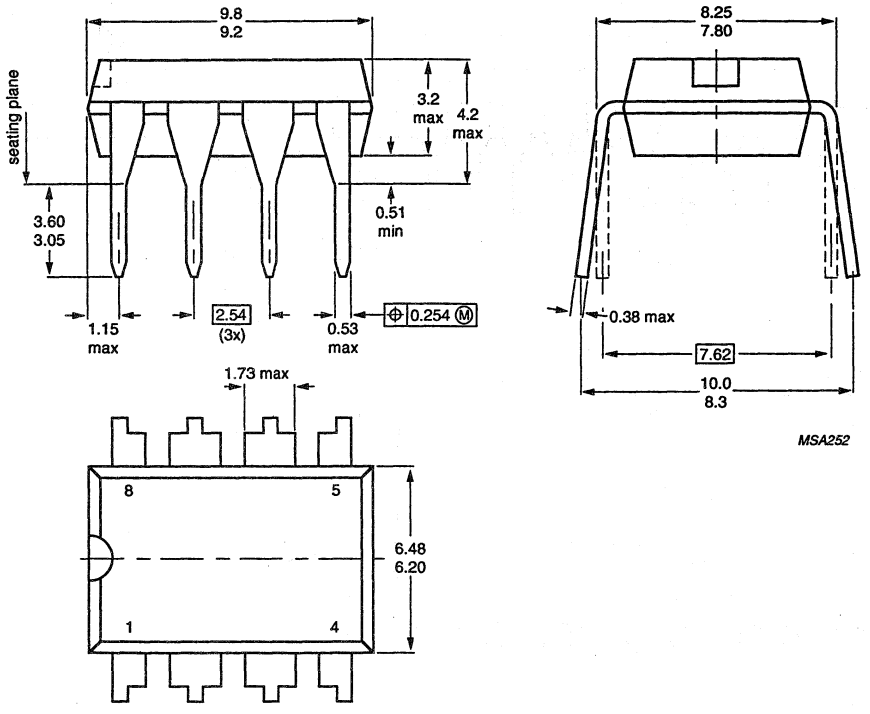
Package outlines



Dimensions in mm.

Fig.19 SO, plastic, 8-pin (straight) (SO8S) (SOT96C).

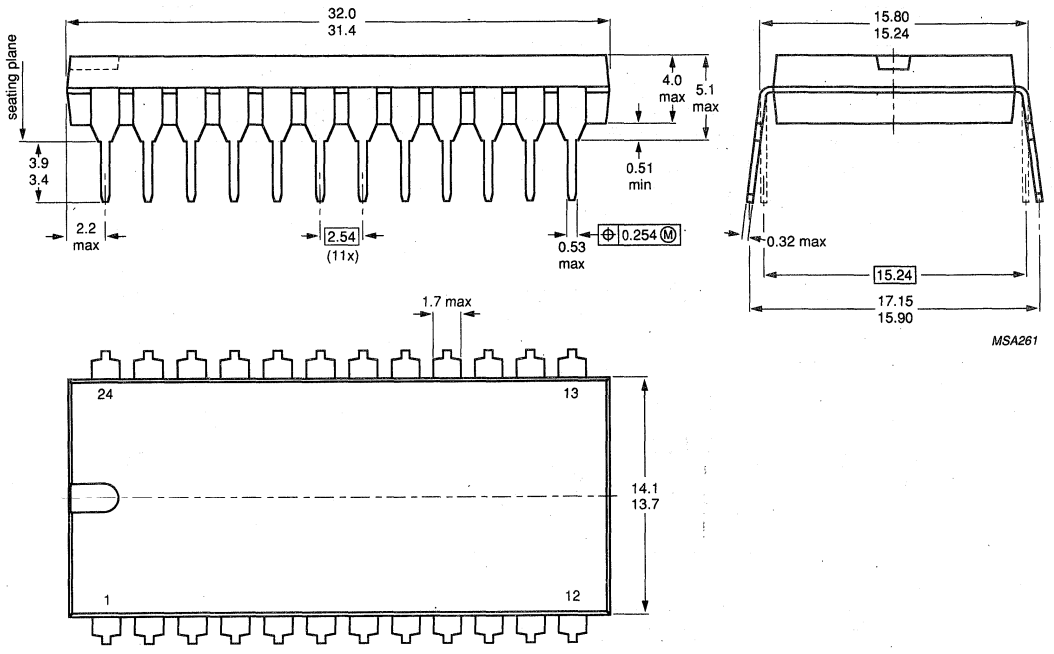
Package outlines



Dimensions in mm.

Fig.20 DIL-bent-SIL, plastic, 8-pin (DIL8) (SOT97DE, DJ, GG).

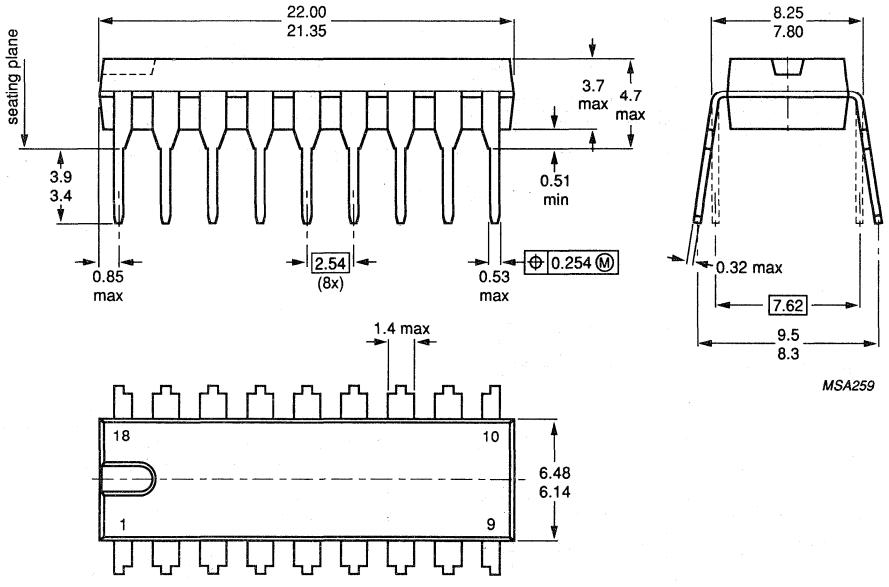
Package outlines



Dimensions in mm.

Fig.21 Dual in-line, plastic, 24-pin (DIL24) (SOT101AG, FE, LE, LG).

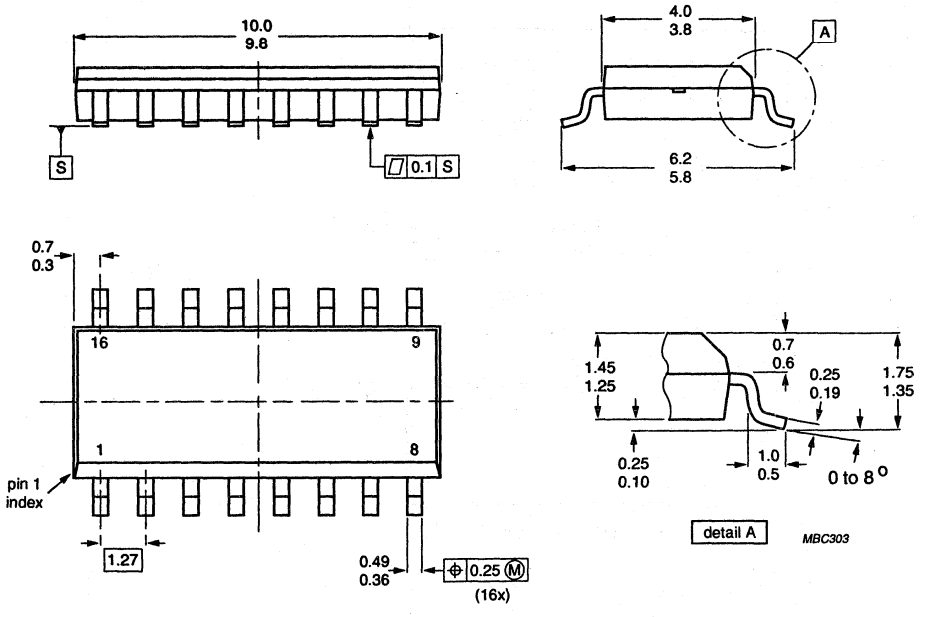
Package outlines



Dimensions in mm.

Fig.22 Dual in-line, plastic, 18-pin (DIL18) (SOT102RG, RE, MG).

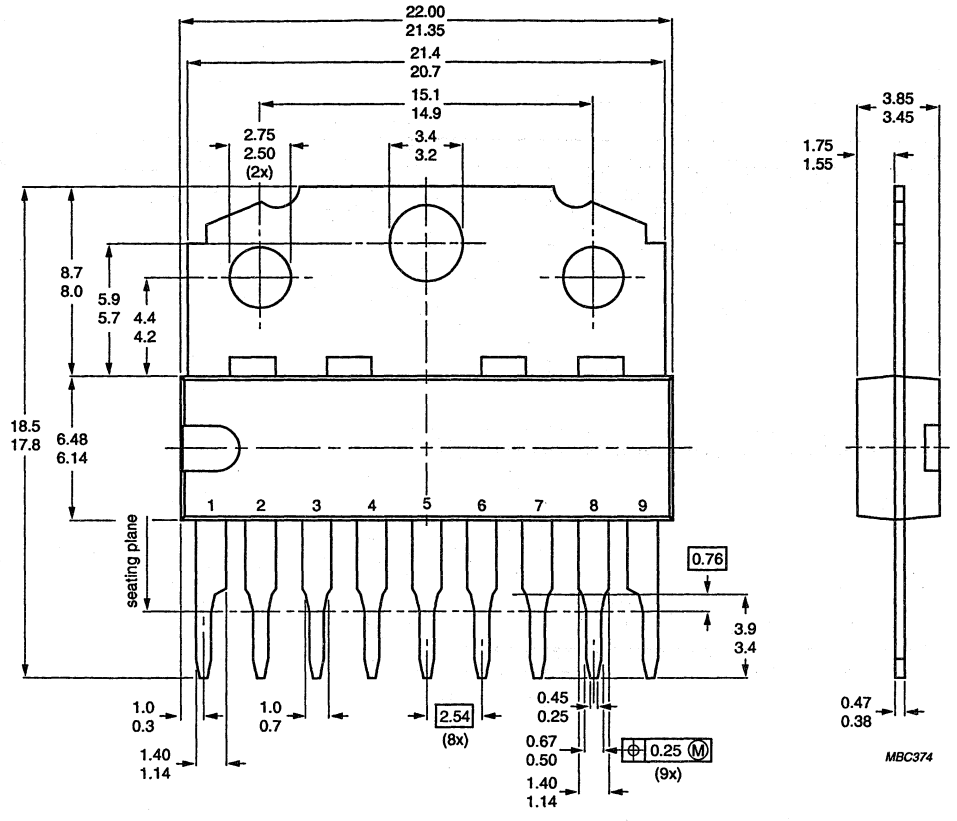
Package outlines



Dimensions in mm.

Fig.23 SO, plastic, 16-pin (SO16) (SOT109AG).

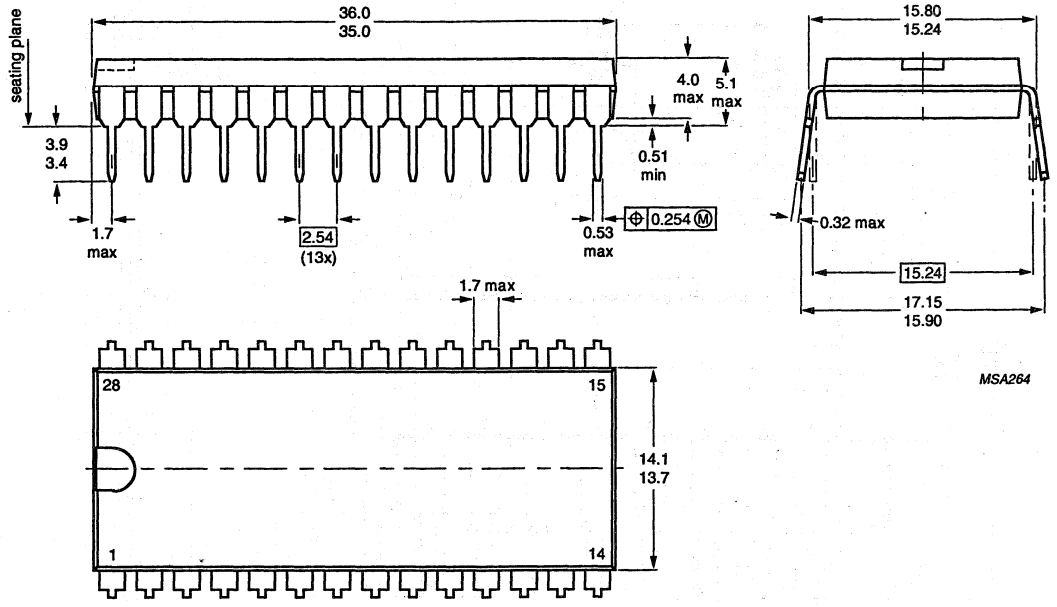
Package outlines



Dimensions in mm.

Fig.24 Single in-line, plastic, medium power with fin, 9-pin (SIL9MPF) (SOT110BE).

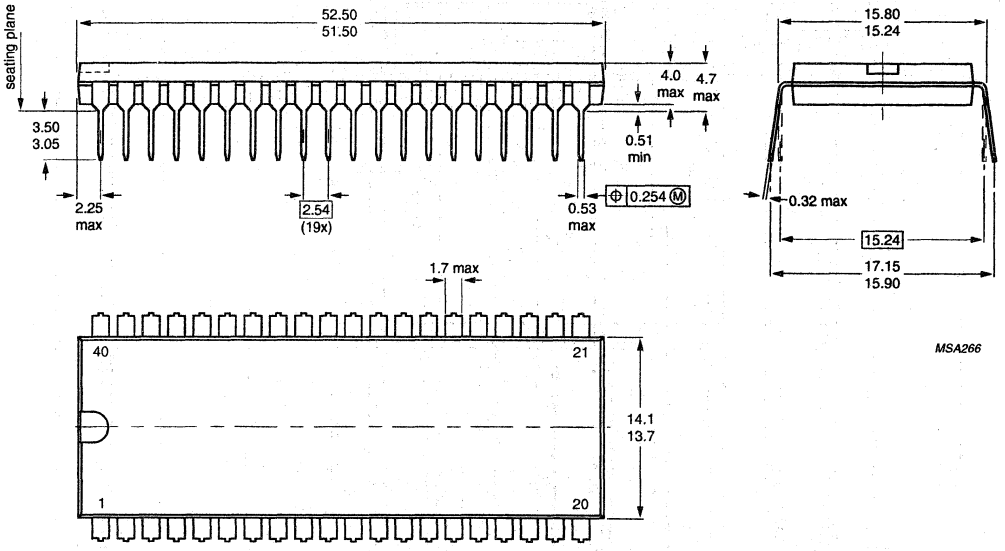
Package outlines



Dimensions in mm.

Fig.25 Dual in-line, plastic, 28-pin (DIL28) (SOT117BE, NE, NG).

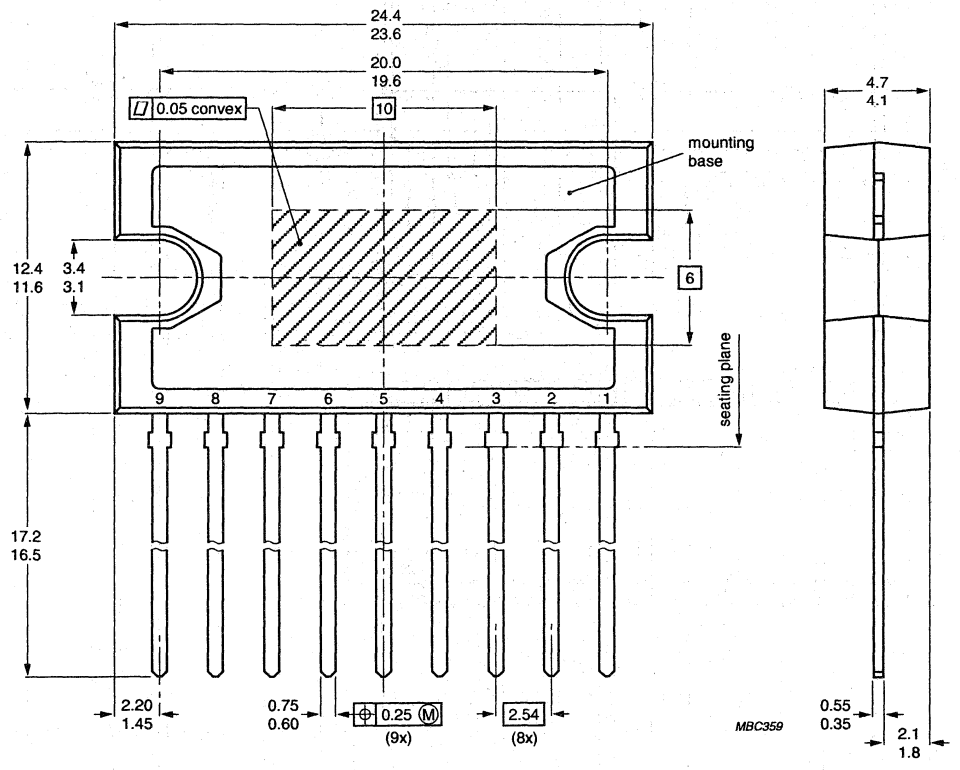
Package outlines



Dimensions in mm.

Fig.26 Dual in-line, plastic, 40-pin (DIL40) (SOT129AE, AG, DE, DG, DH, FE, FG, FH).

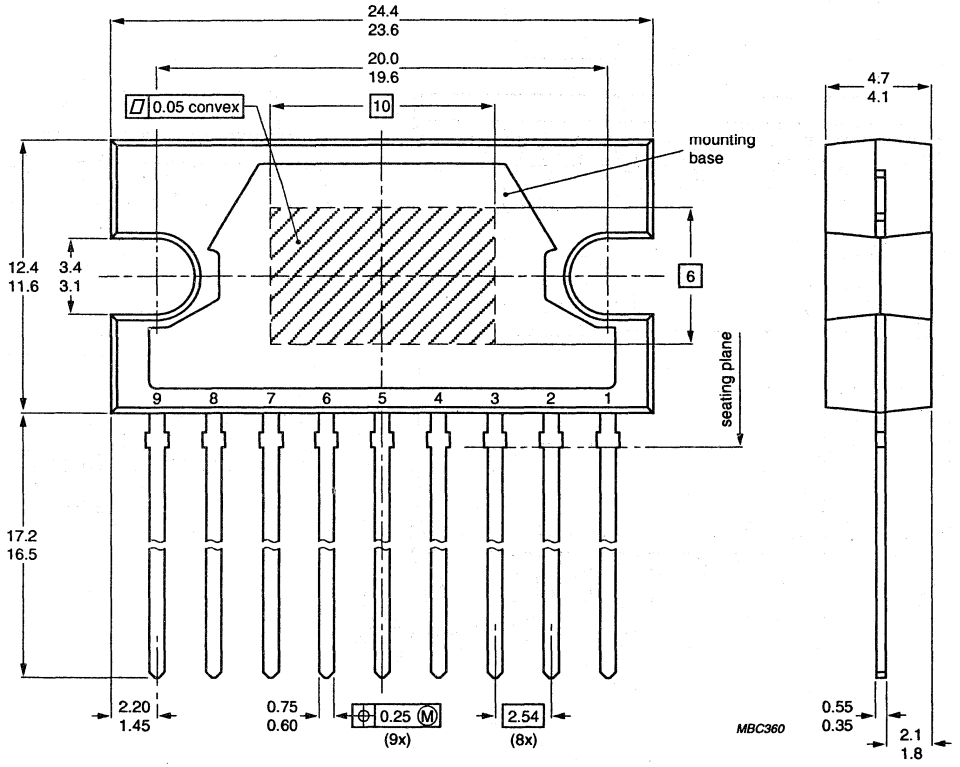
Package outlines



Dimensions in mm.

Fig.27 Single in-line, plastic, power, 9-pin (SIL9P) (SOT131A, BE, CE).

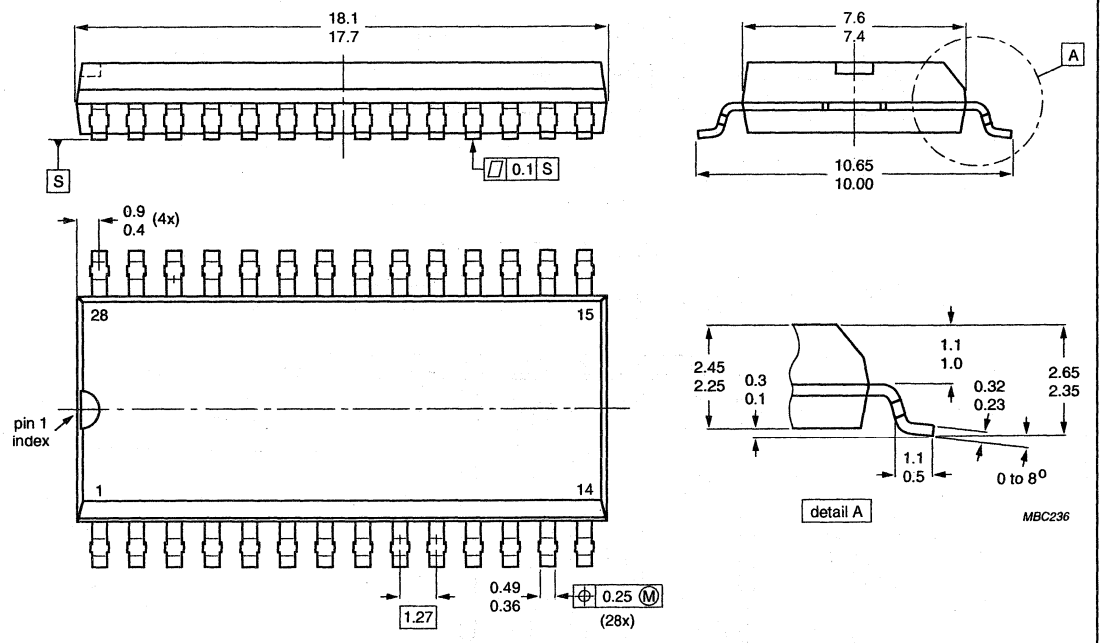
Package outlines



Dimensions in mm.

Fig.28 Single in-line, plastic, power, 9-pin (SIL9P) (SOT131RA, RBE, RDG, RFG, RG).

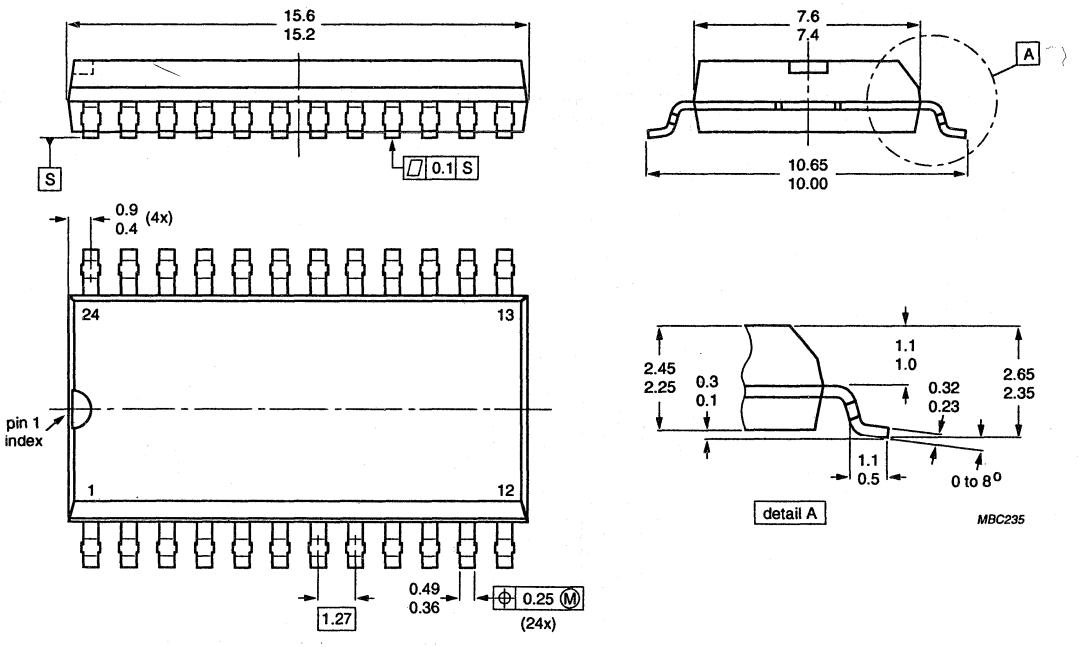
Package outlines



Dimensions in mm.

Fig.29 SOL, plastic, 28-pin (SO28L) (SOT136AG, AH).

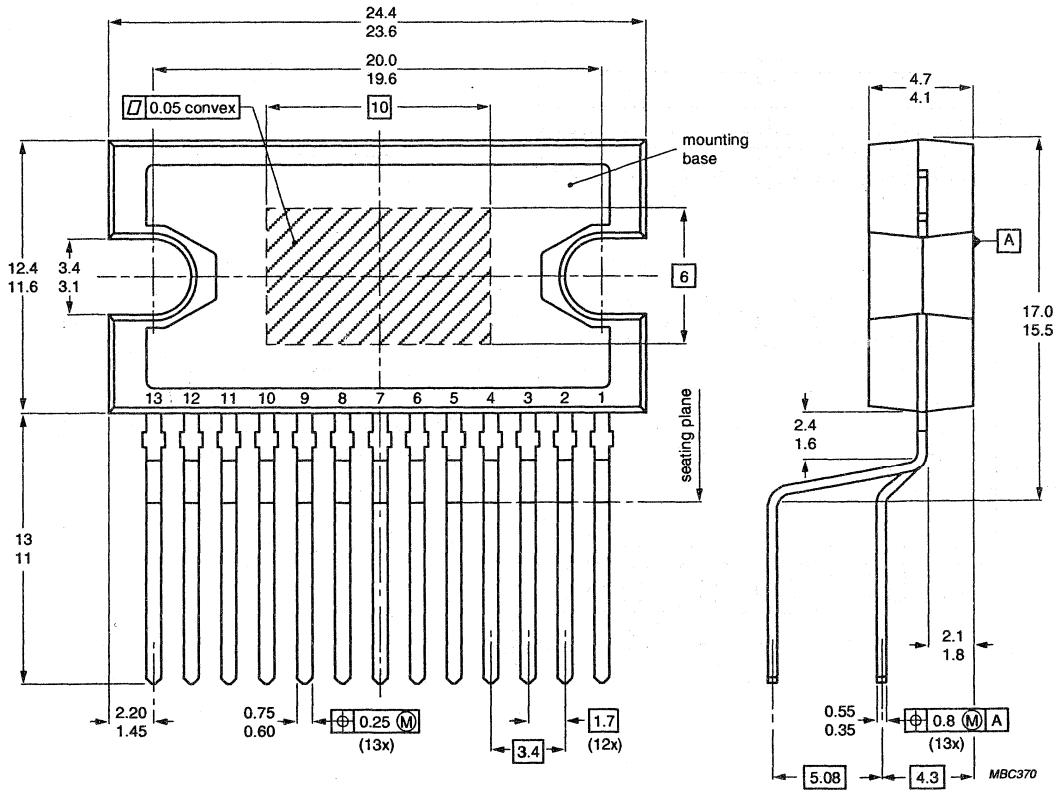
Package outlines



Dimensions in mm.

Fig.30 SOL, plastic, 24-pin (SO24L) (SOT137AG, AH).

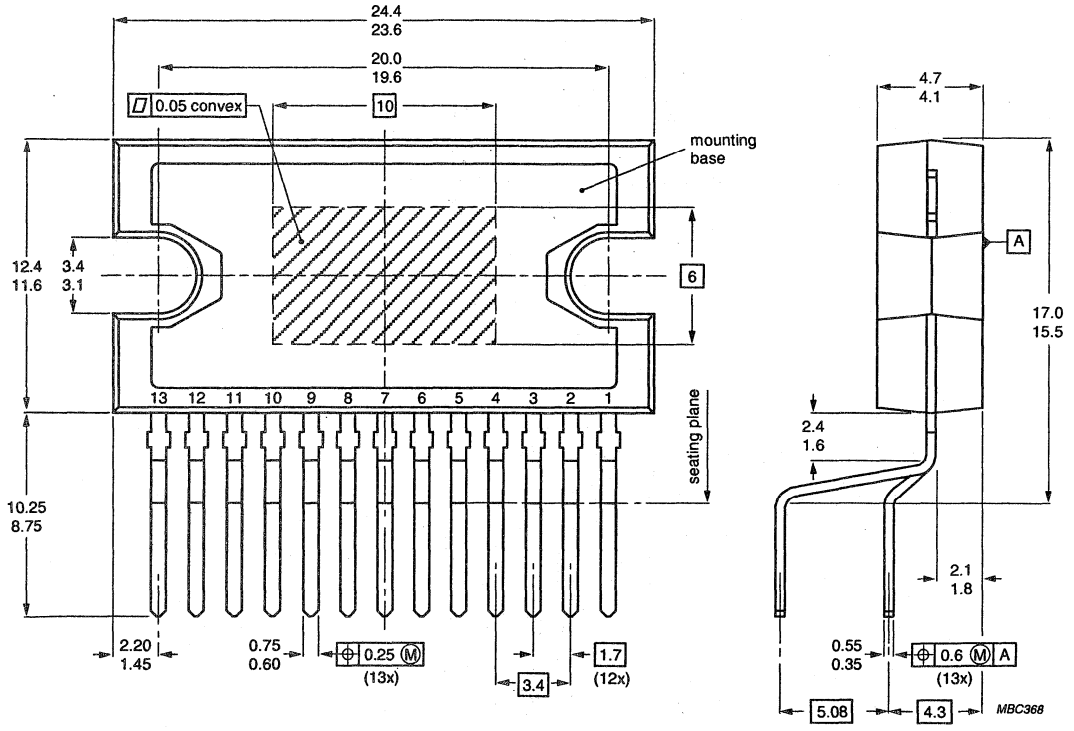
Package outlines



Dimensions in mm.

Fig.31 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEA, CEA).

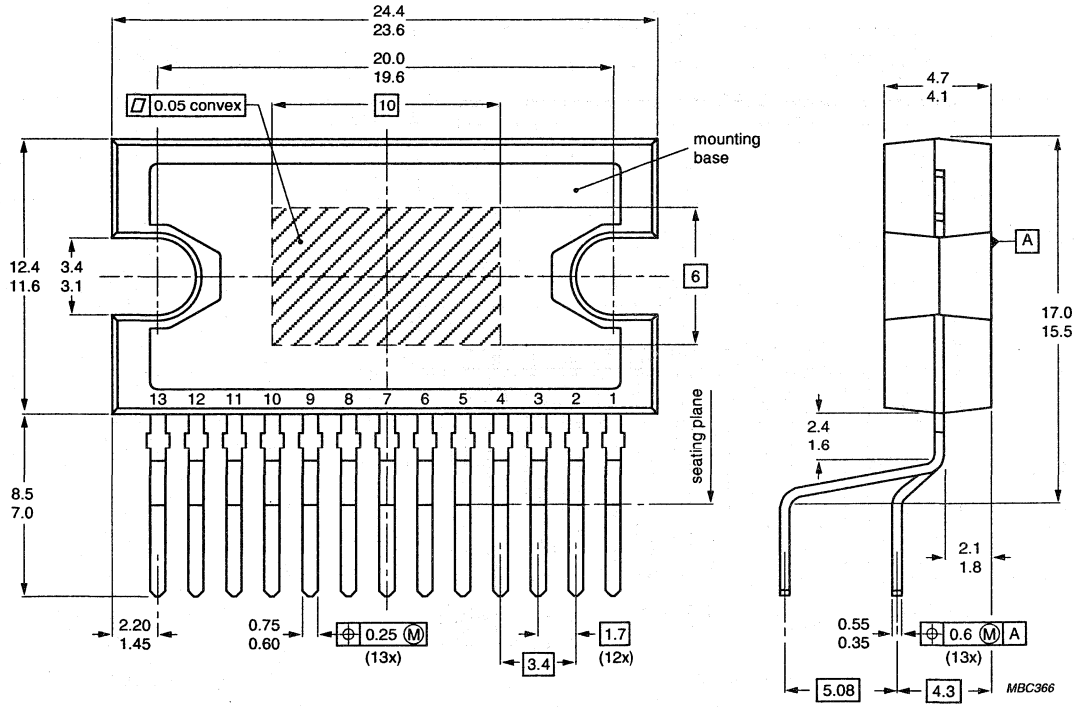
Package outlines



Dimensions in mm.

Fig.32 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEB, CEB).

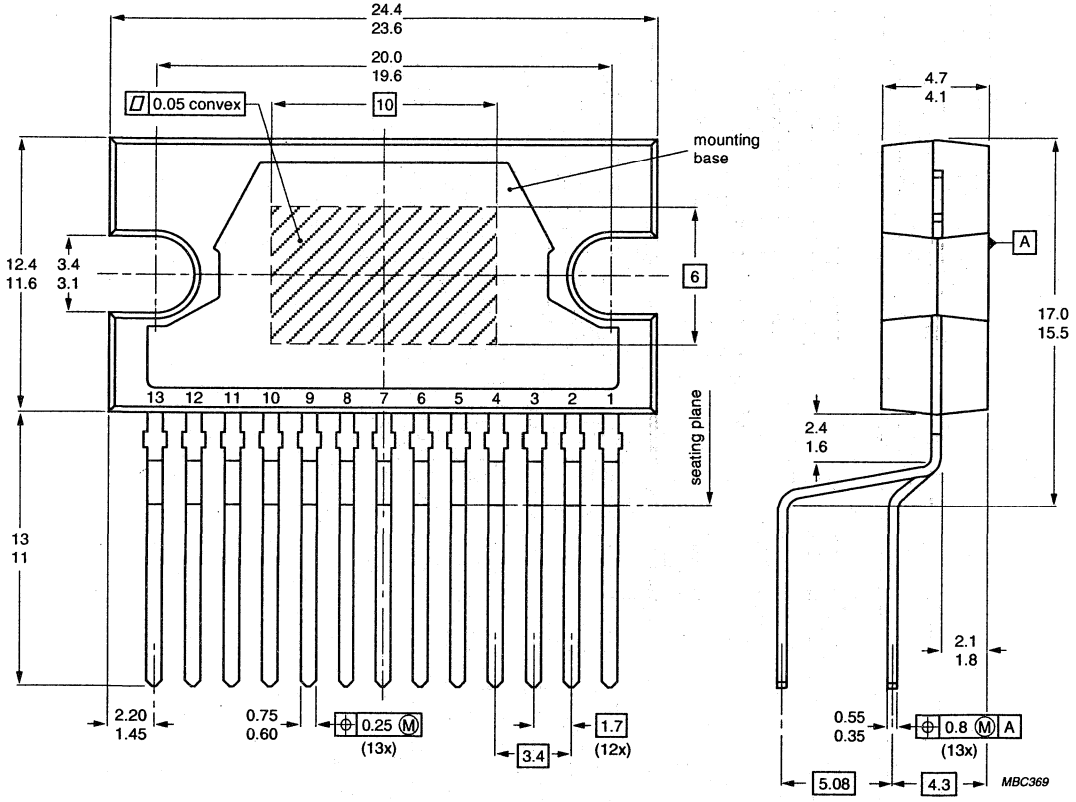
Package outlines



Dimensions in mm.

Fig.33 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEC, CEC).

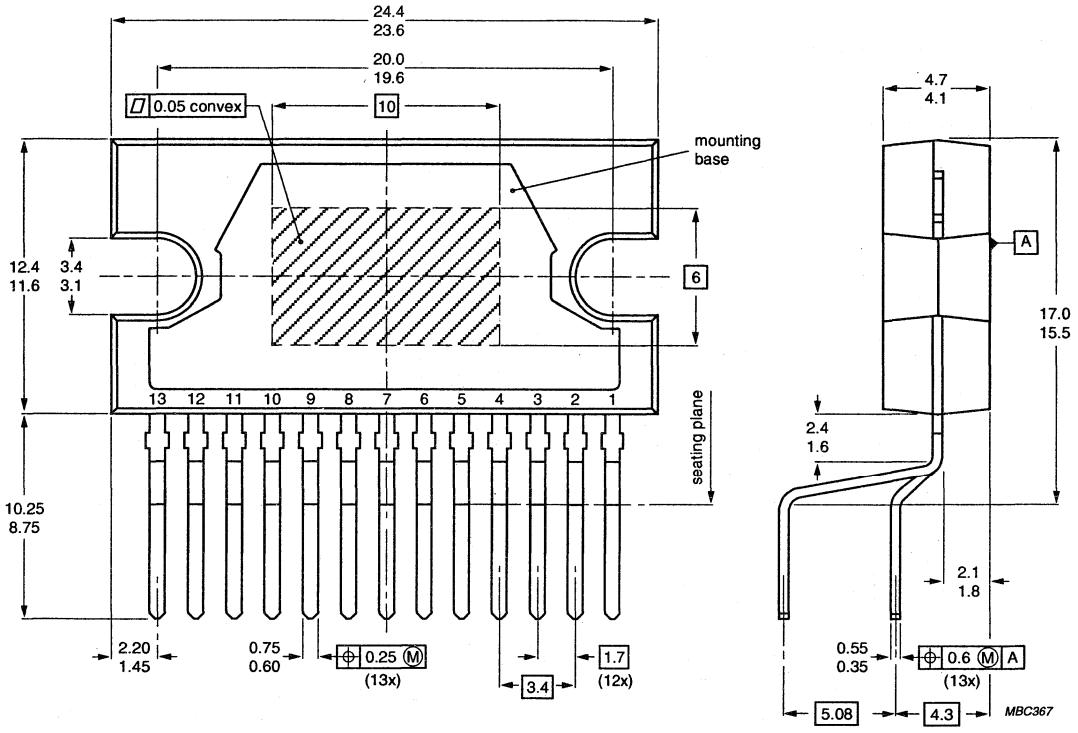
Package outlines



Dimensions in mm.

Fig.34 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAA, RBEA, RDGA, RFGA, RGA).

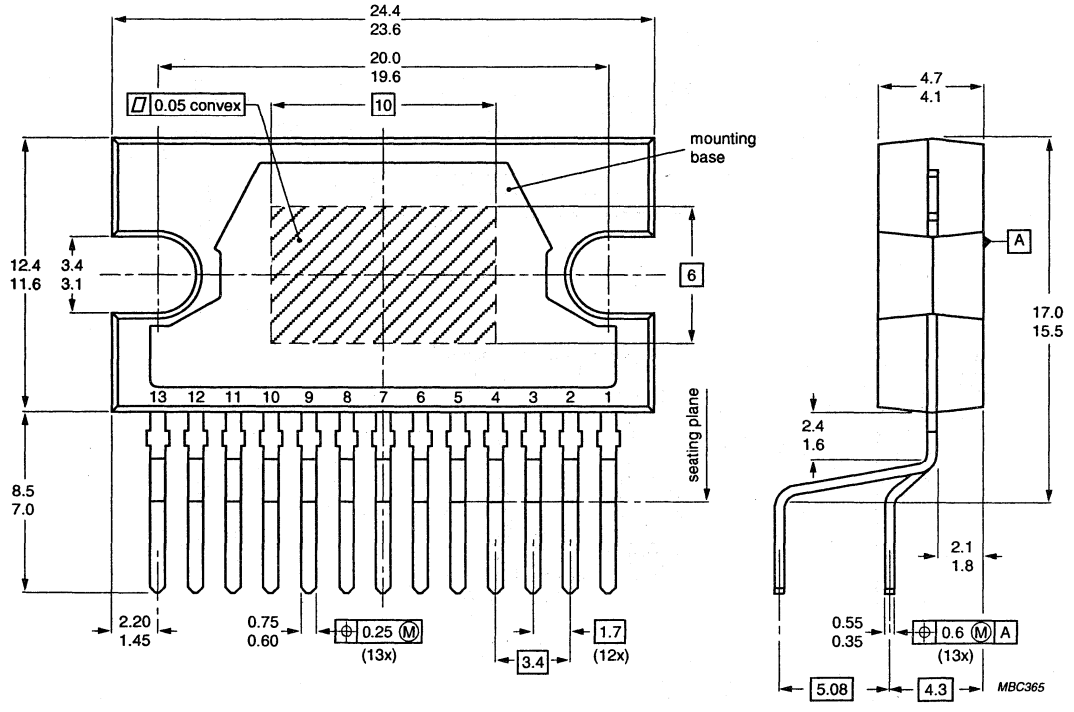
Package outlines



Dimensions in mm.

Fig.35 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAB, RBEB).

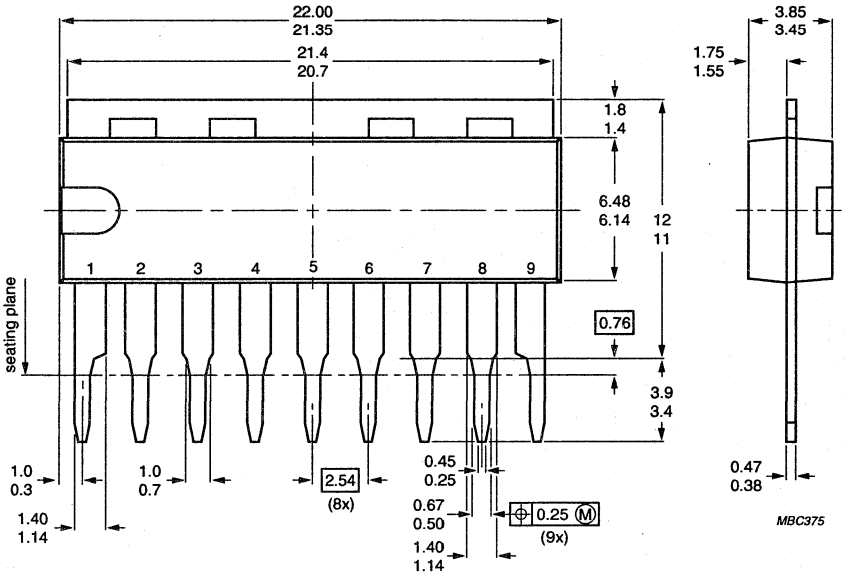
Package outlines



Dimensions in mm.

Fig.36 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAC, RBEC, RDGC, RFGC, RGC).

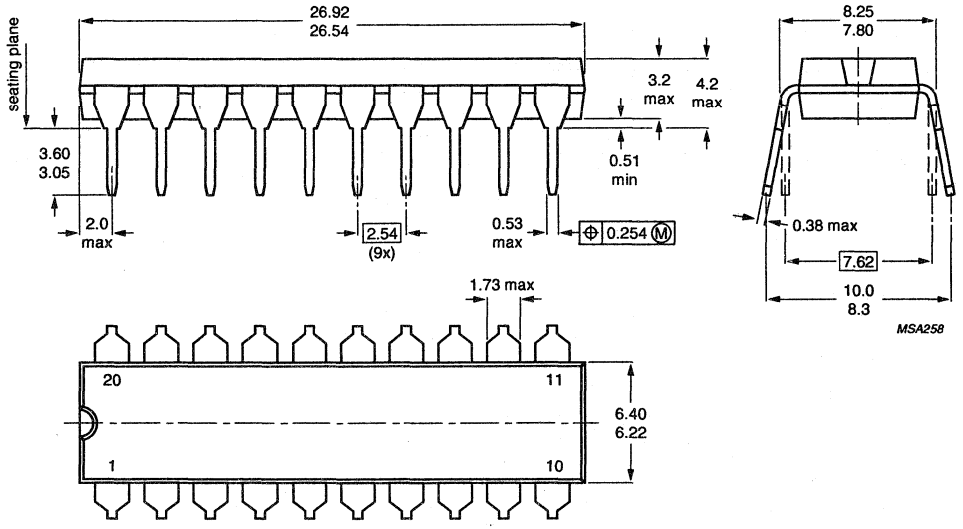
Package outlines



Dimensions in mm.

Fig.37 Single in-line, plastic, medium power, 9-pin (SIL9MP) (SOT142BE).

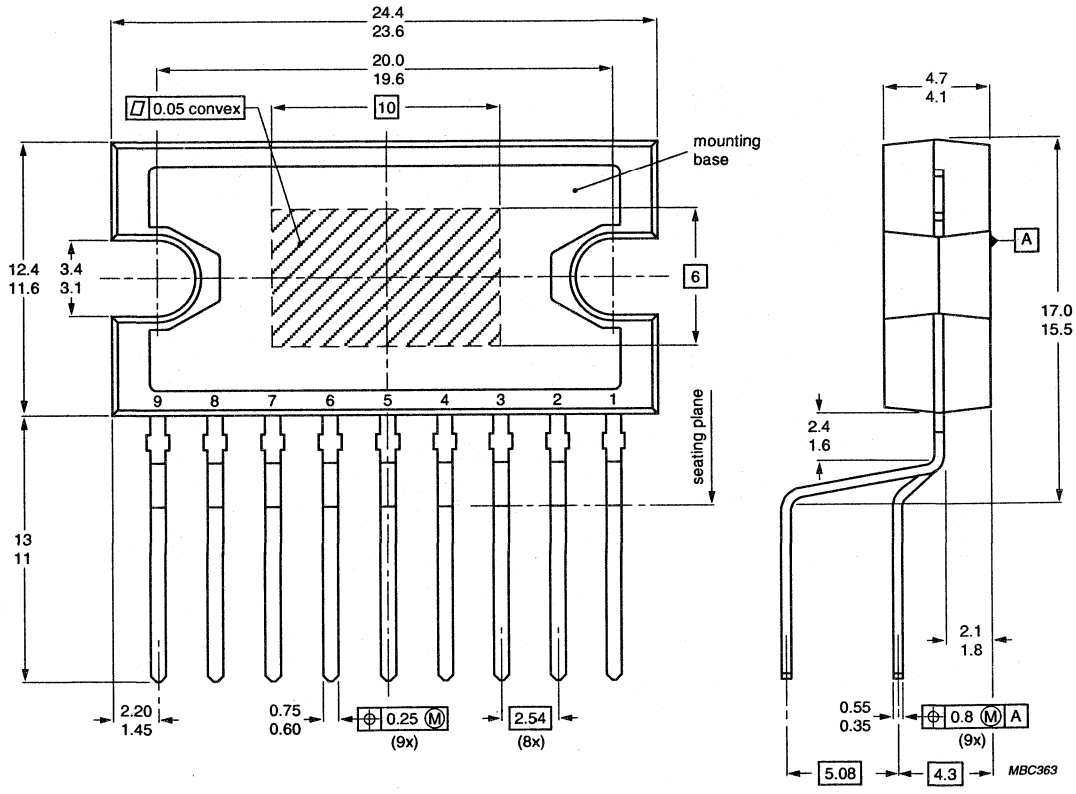
Package outlines



Dimensions in mm.

Fig.38 Dual in-line, plastic, 20-pin (DIL20) (SOT146EF, EG, FE).

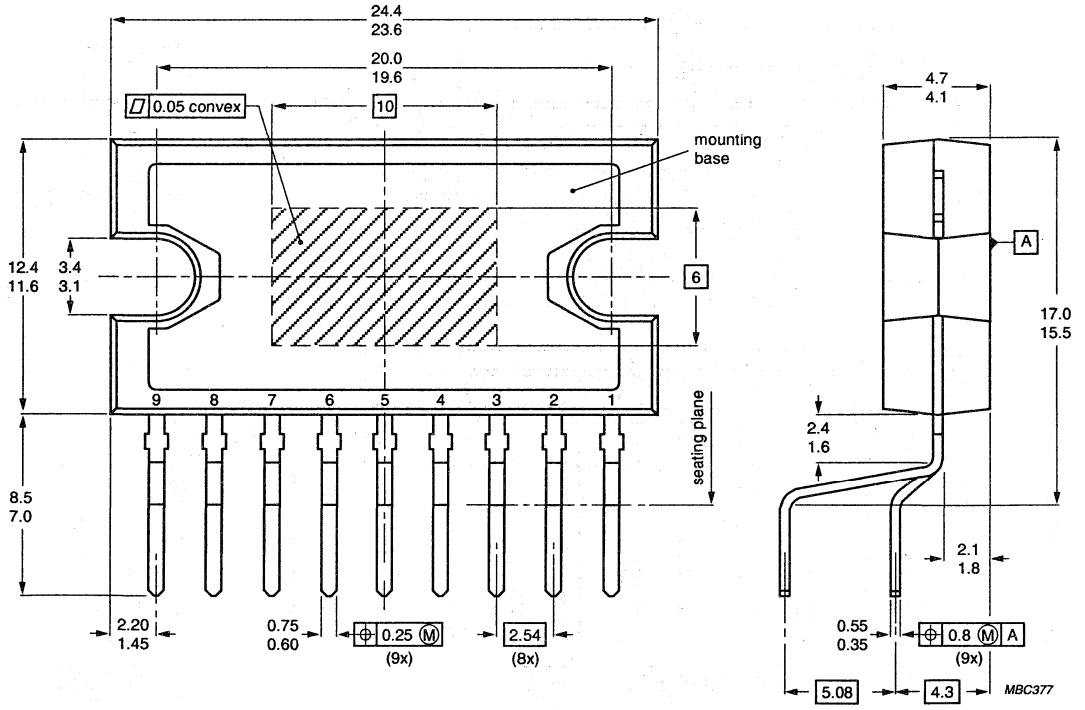
Package outlines



Dimensions in mm.

Fig.39 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157A, BE, CE).

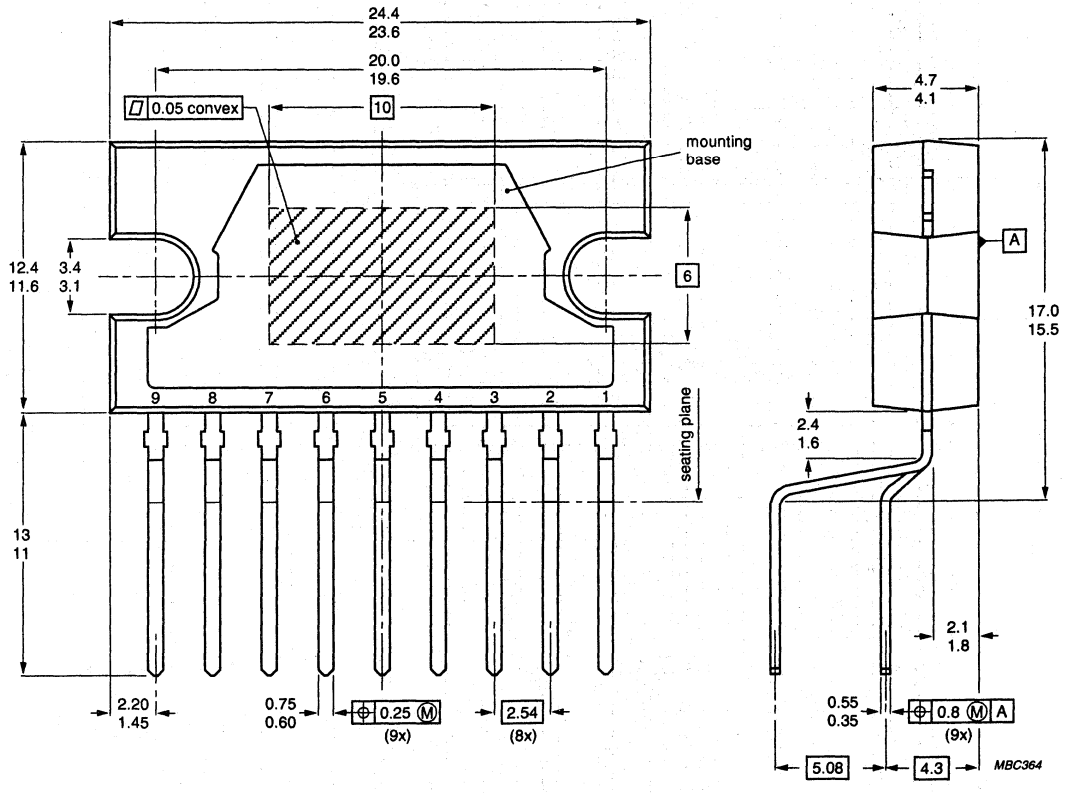
Package outlines



Dimensions in mm.

Fig.40 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157AC, BEC, CEC).

Package outlines



Dimensions in mm.

Fig.41 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157RA, RBE, RCE, RDGA, RDGC, RFGA, RFGC, RGA).

Package outlines

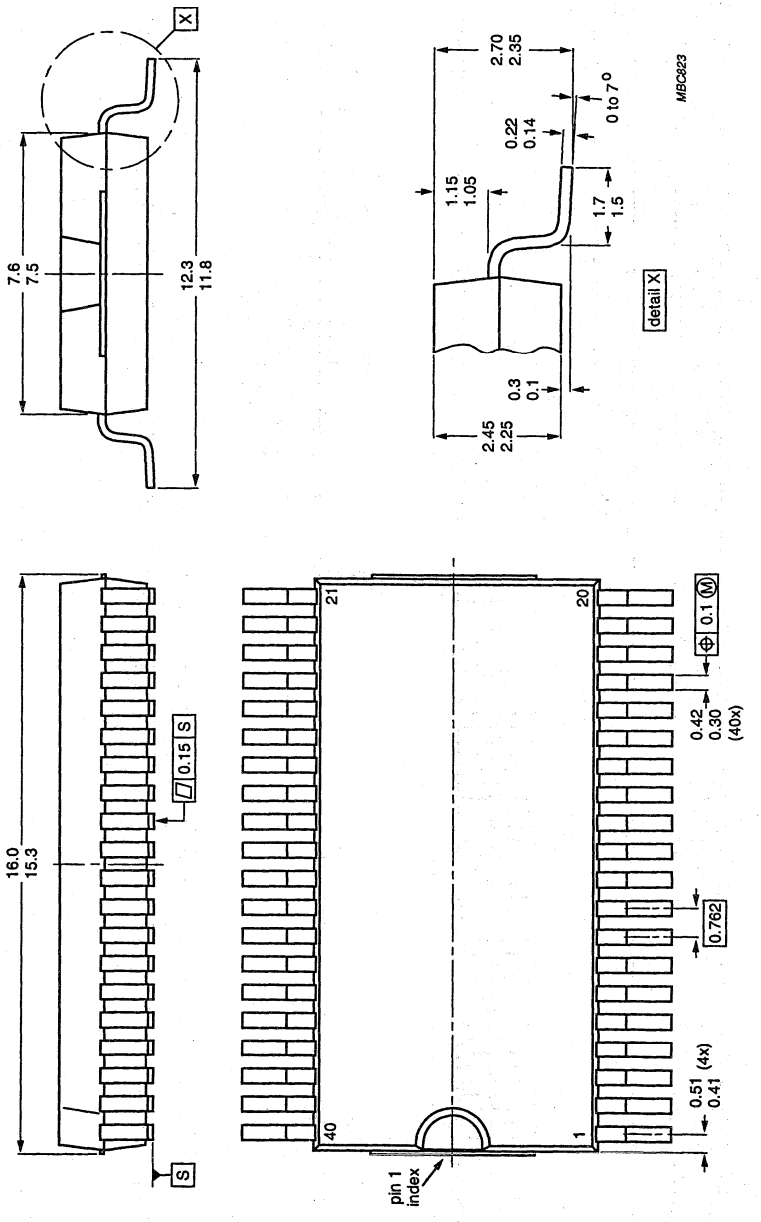
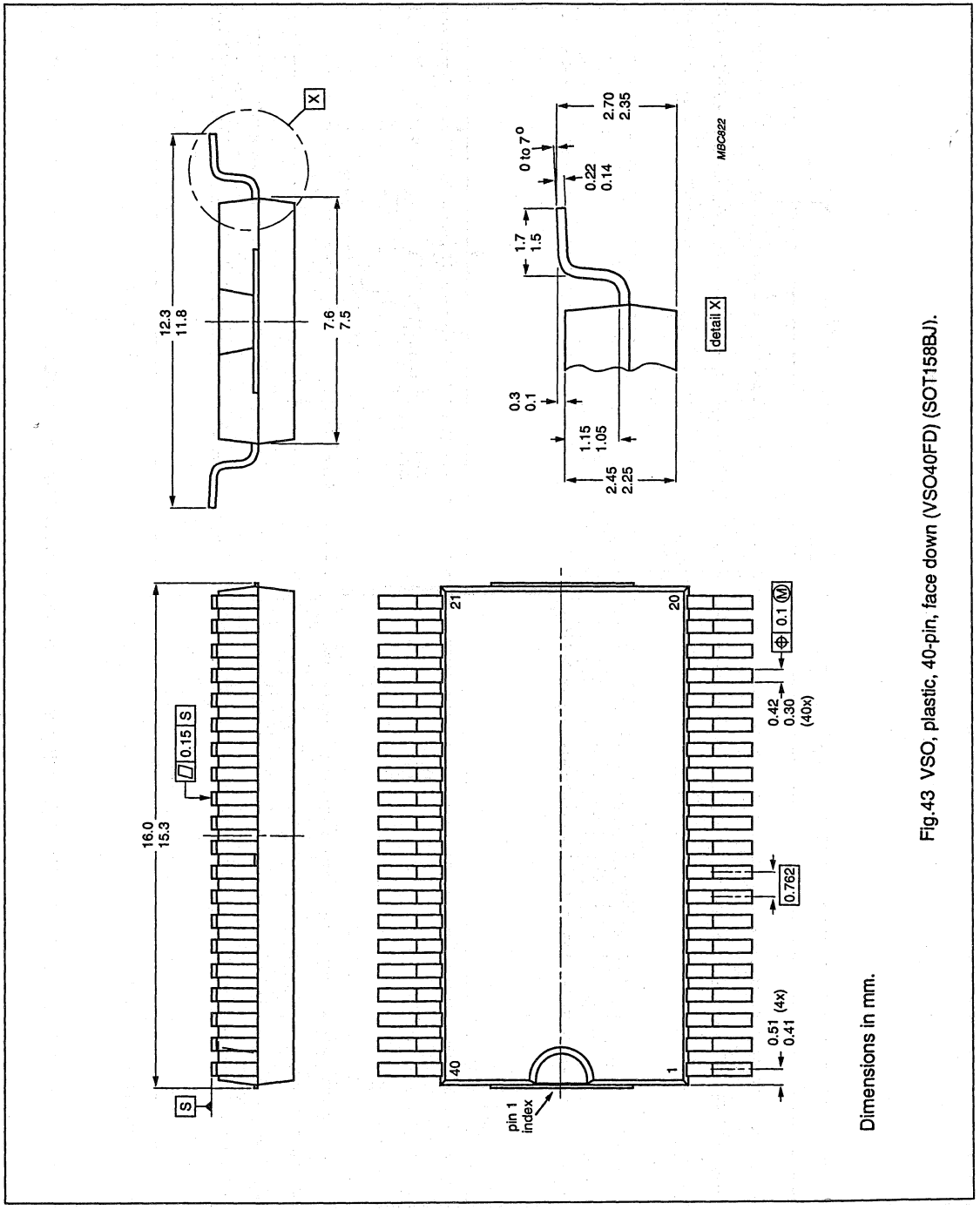


Fig.42 VSO, plastic, 40-pin (VSO40) (SOT158AJ).

Dimensions in mm.

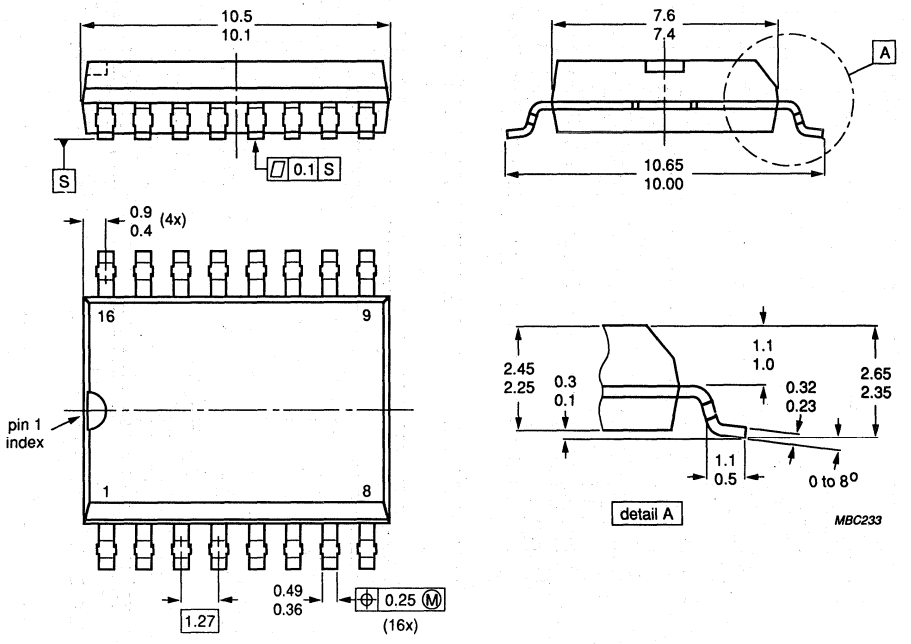
Package outlines



Dimensions in mm.

Fig.43 VSO, plastic, 40-pin, face down (VSO40FD) (SOT158BJ).

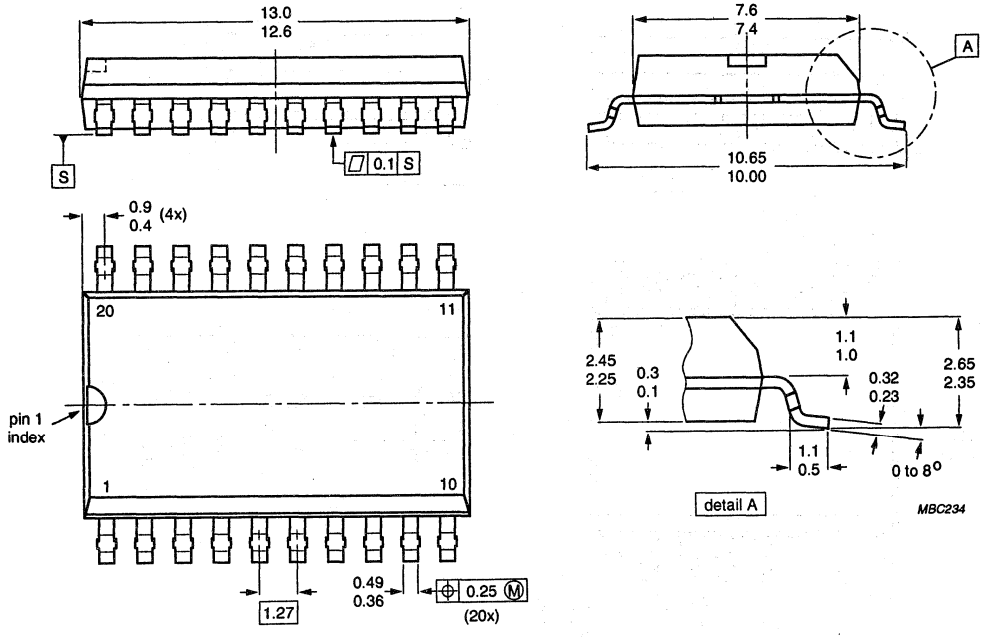
Package outlines



Dimensions in mm.

Fig.44 SOL, plastic, 16-pin (SO16L) (SOT162AG, AH).

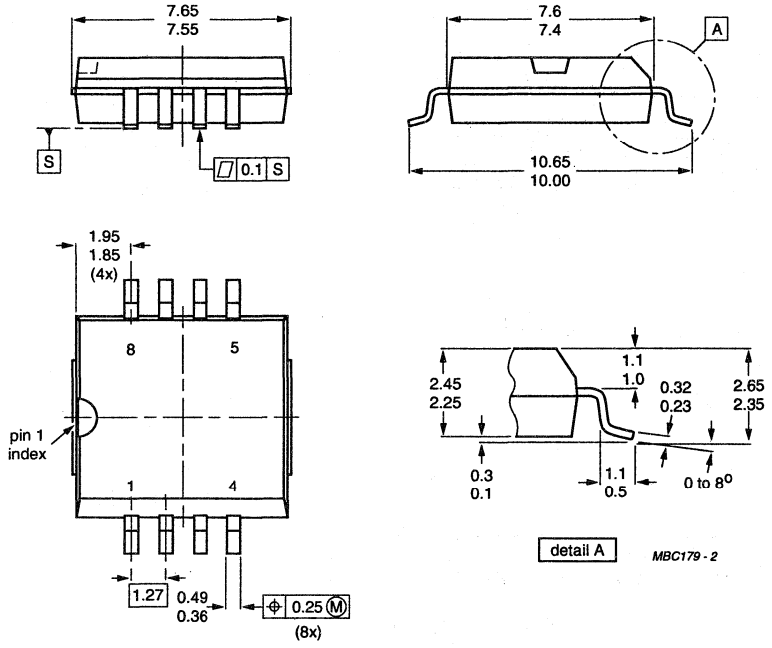
Package outlines



Dimensions in mm.

Fig.45 SOL, plastic, 20-pin (SO20L) (SOT163AG, AH).

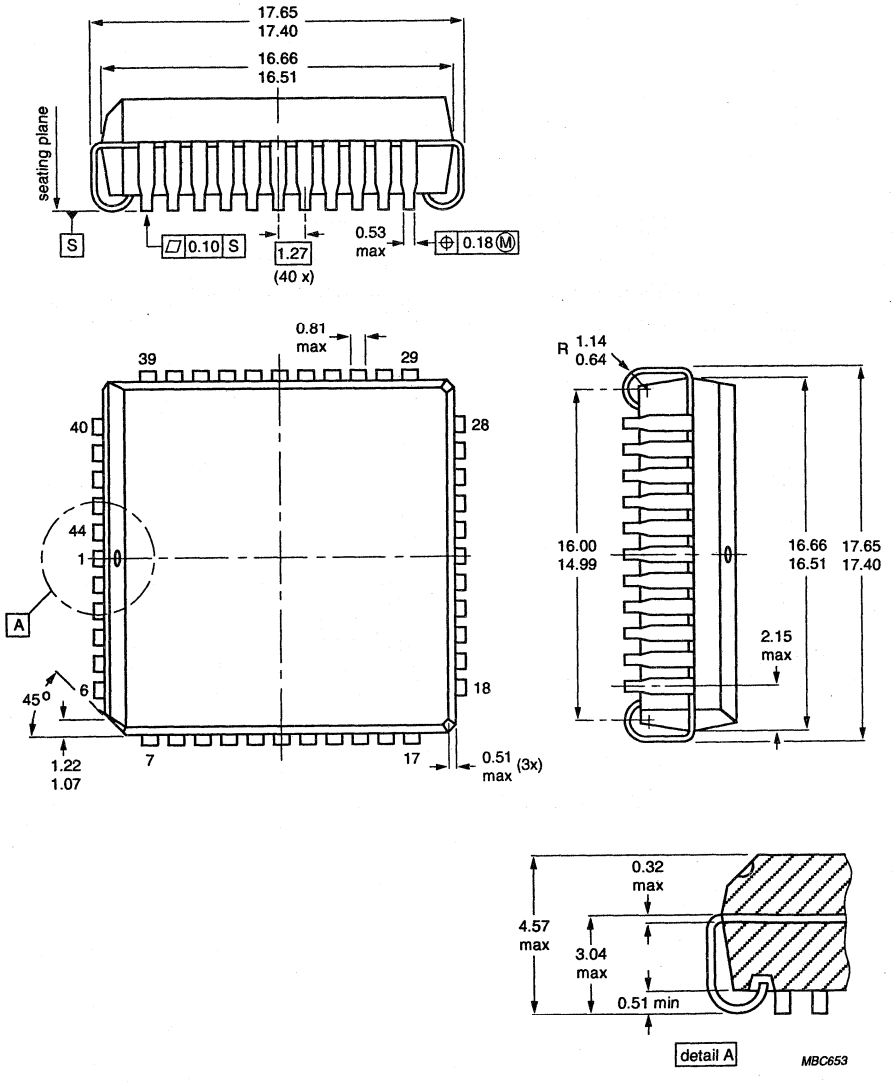
Package outlines



Dimensions in mm.

Fig.46 SOL, plastic, 8-pin (SO8L) (SOT176DG).

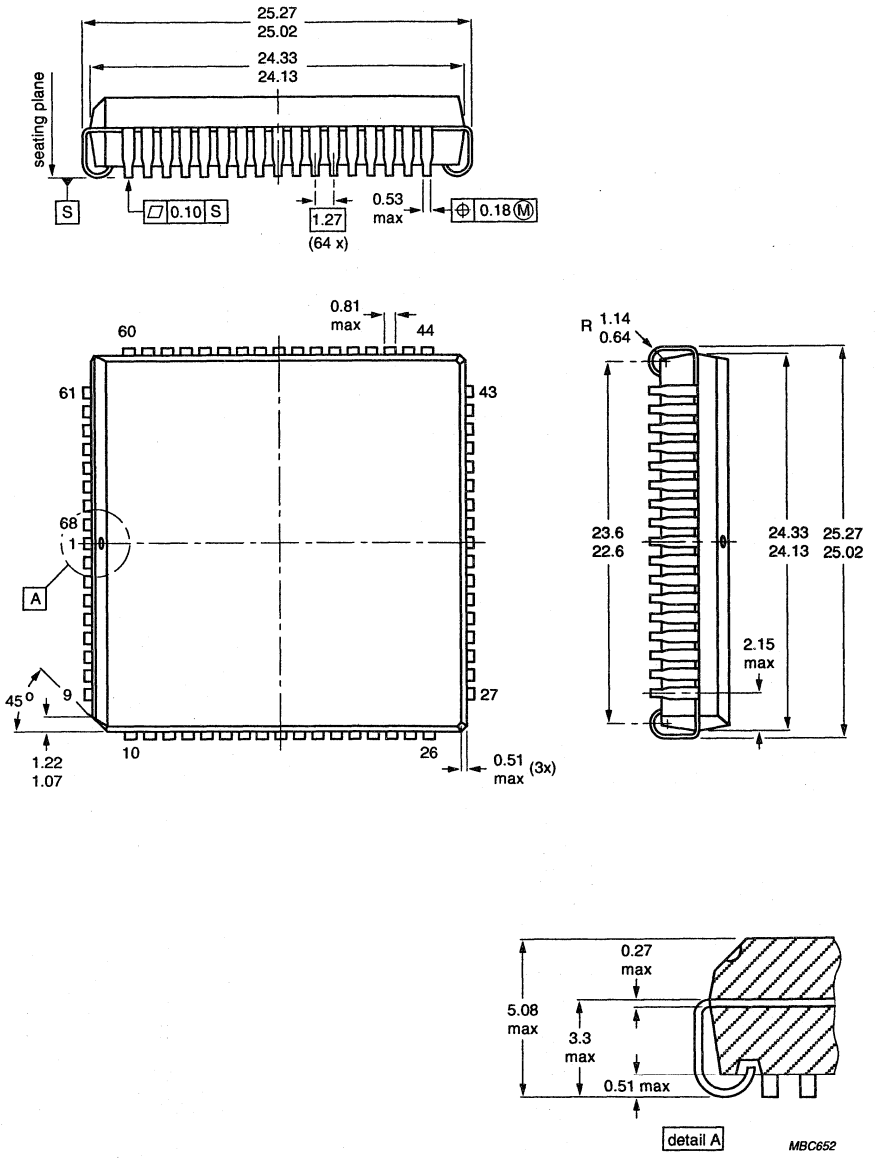
Package outlines



Dimensions in mm.

Fig.47 Plastic headed chip carrier, 44-lead (PLCC44) (SOT187CG).

Package outlines



Dimensions in mm.

Fig.48 Plastic headed chip carrier, 68-lead (PLCC68) (SOT188CG).

Package outlines

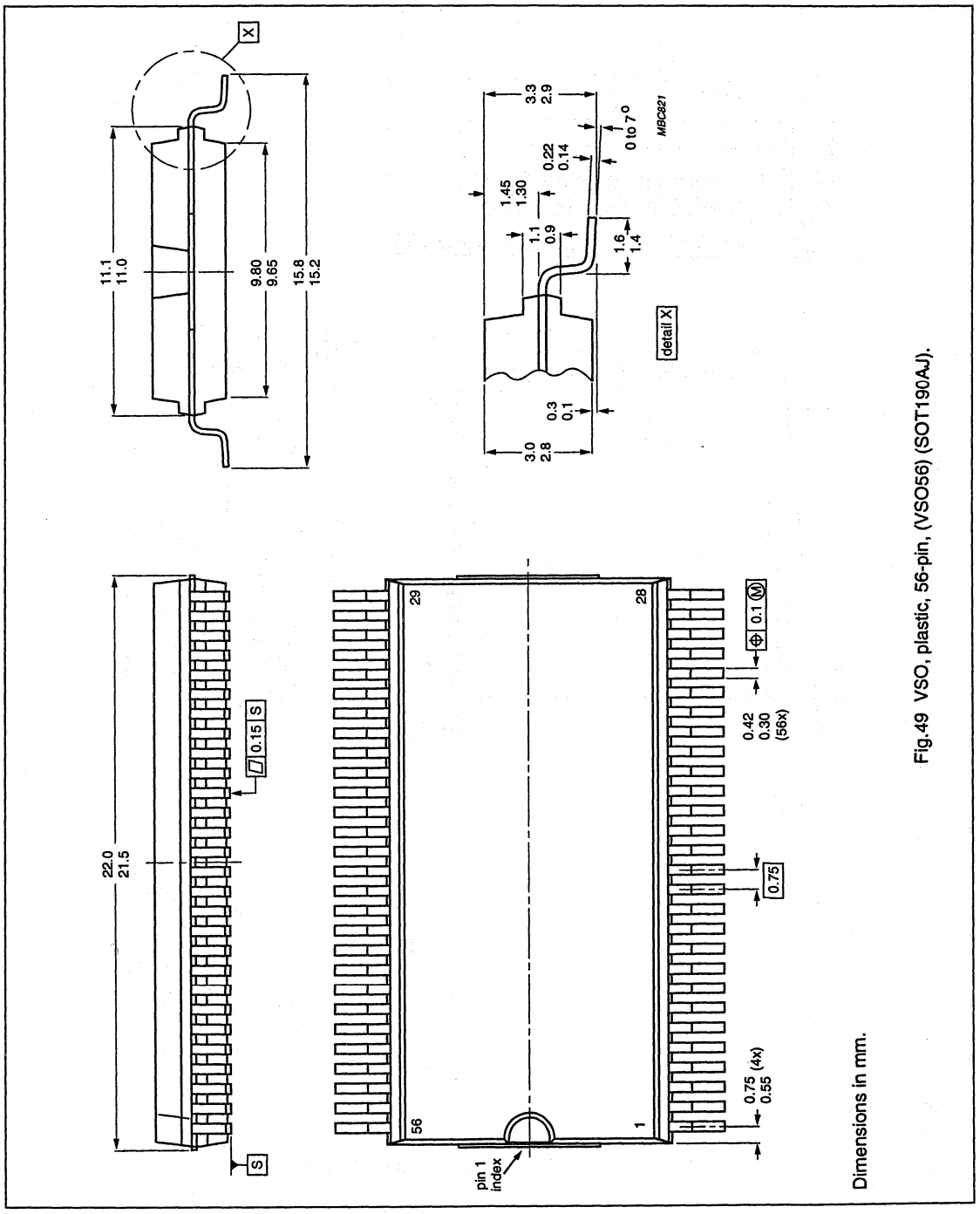


Fig.49 VSO, plastic, 56-pin, (VSO56) (SOT190AJ).

Package outlines

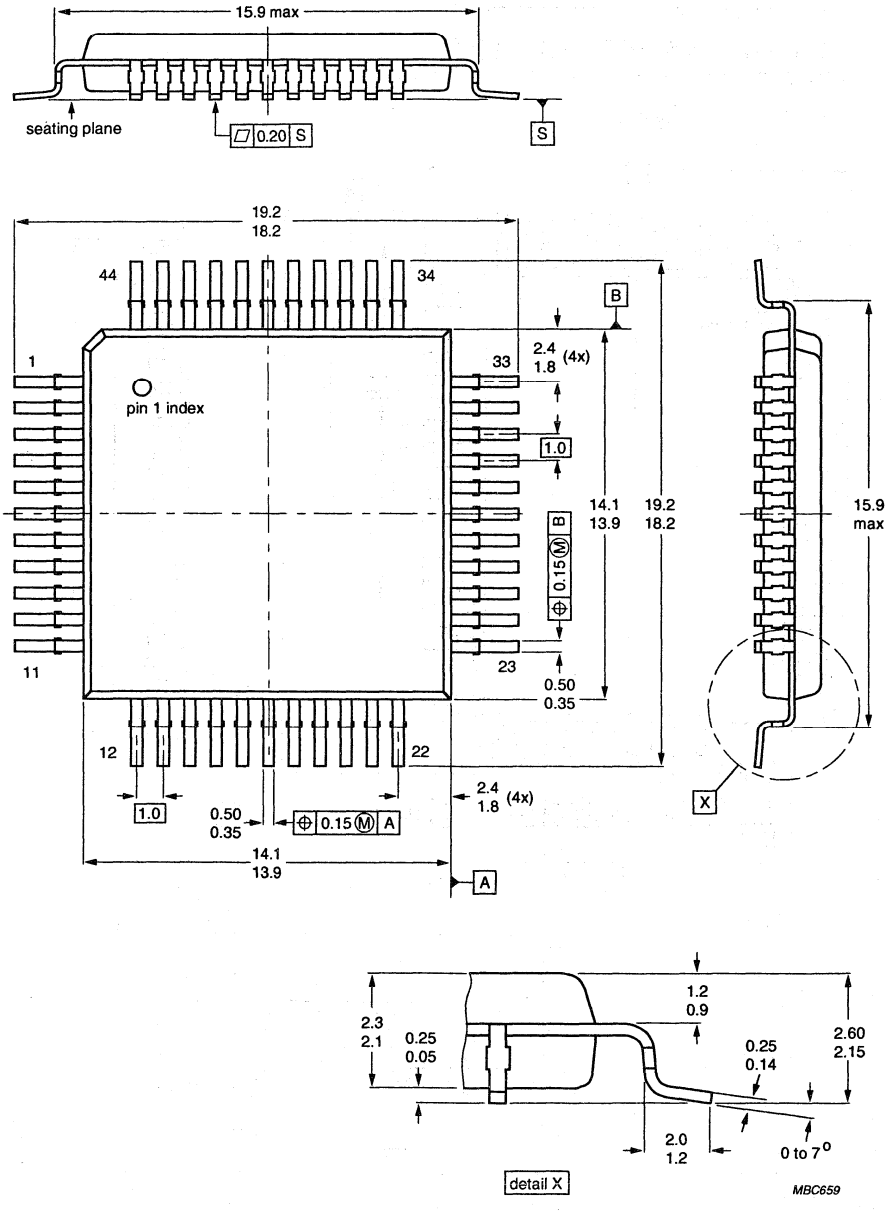
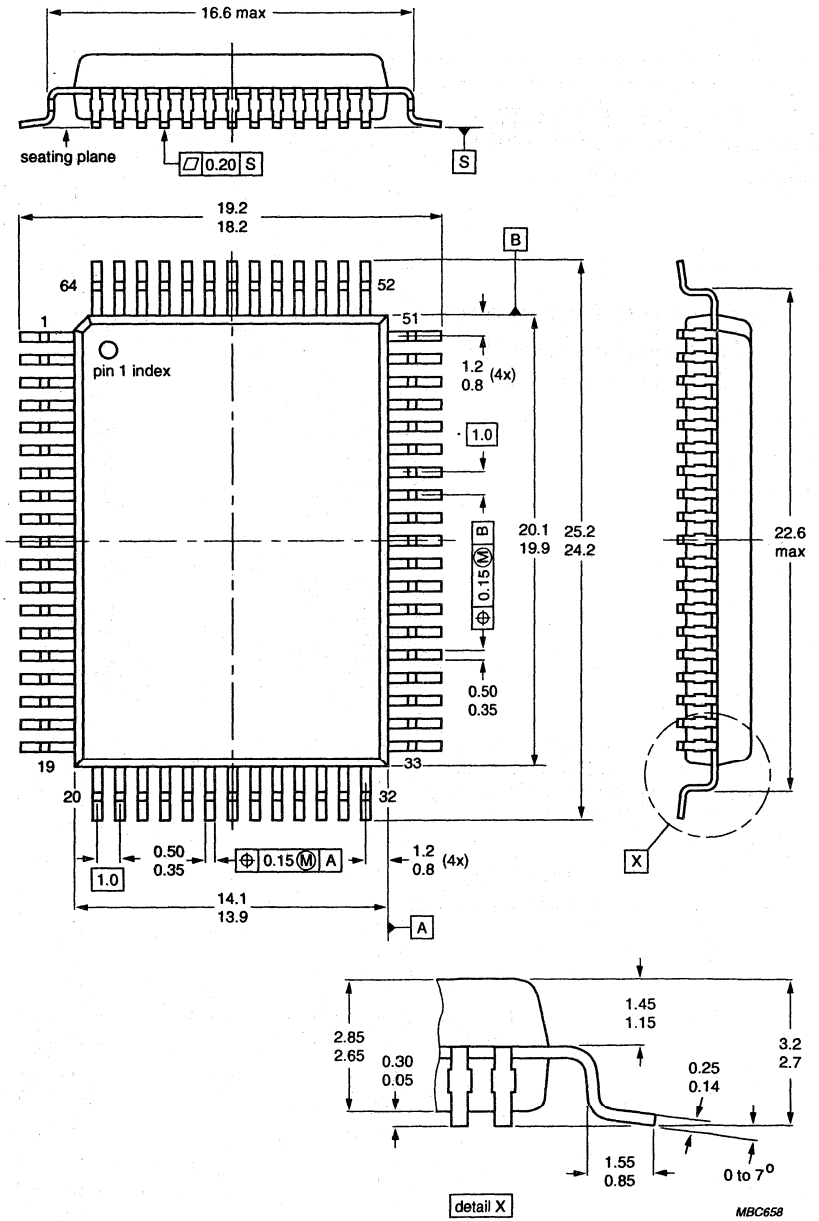


Fig.50 Quad flat-pack, plastic, 44-pin, 14 mm square (QFP44S14) (SOT205AG).

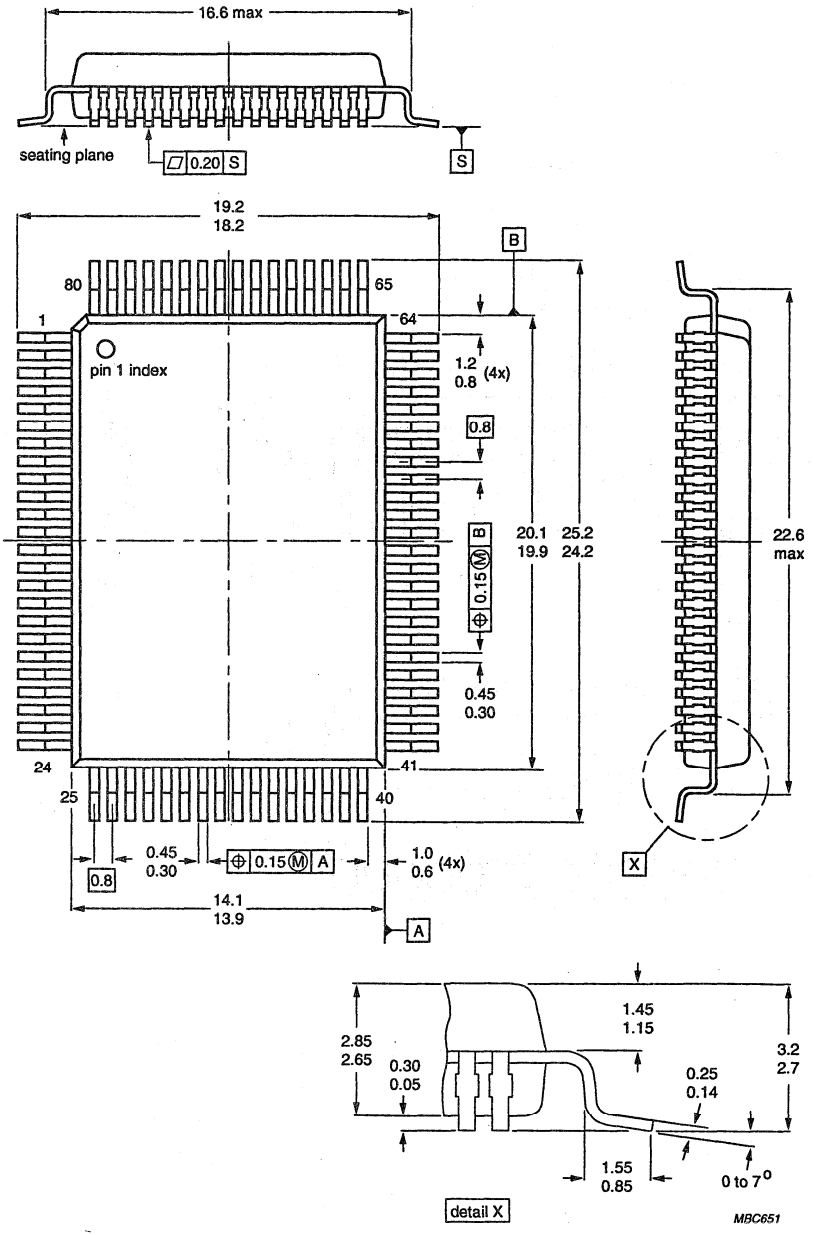
Package outlines



Dimensions in mm.

Fig.51 Quad flat-pack, plastic, 64-pin, rectangular (QFP64REC) (SOT208A).

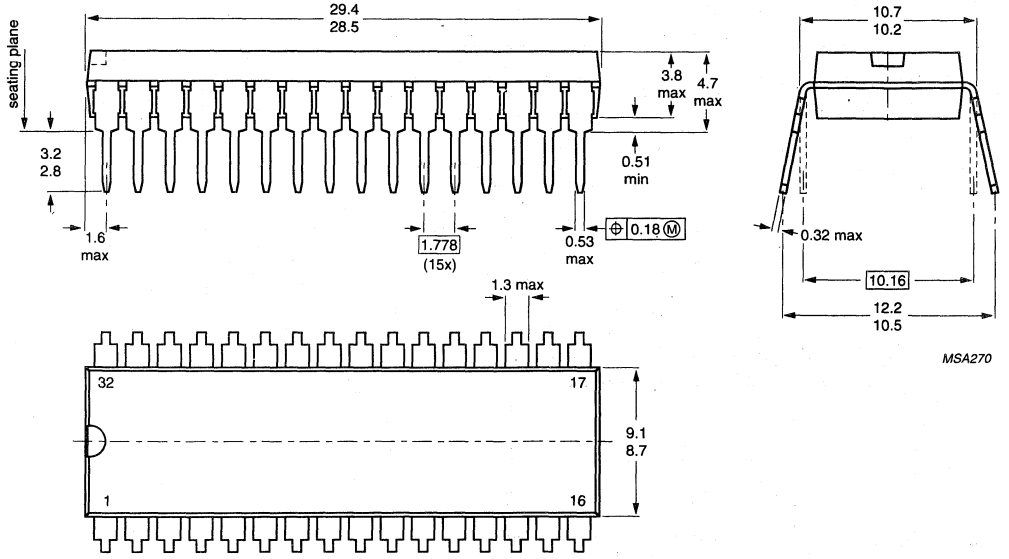
Package outlines



Dimensions in mm.

Fig.52 Quad flat-pack, plastic, 80-pin, rectangular (QFP80REC) (SOT219A).

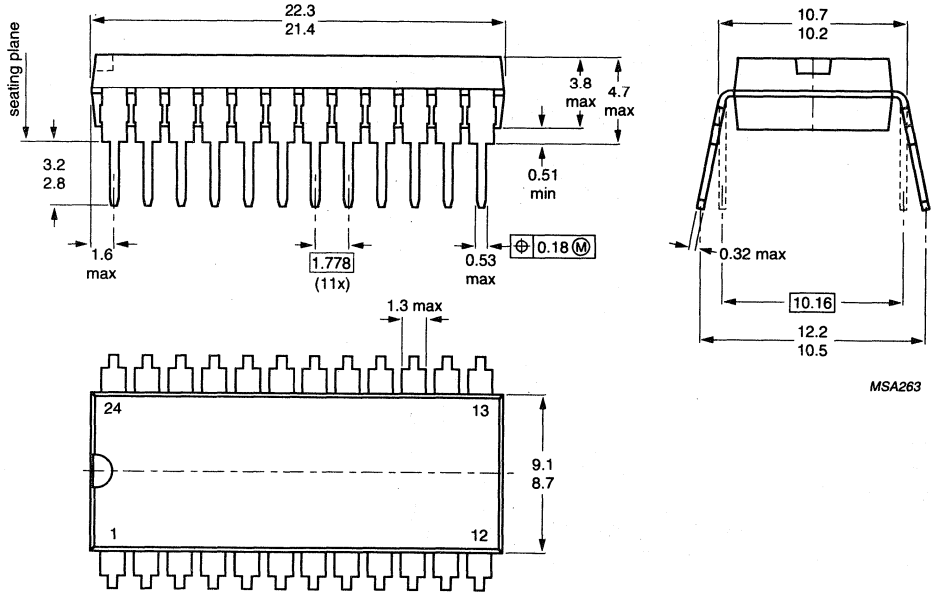
Package outlines



Dimensions in mm.

Fig.53 Shrink dual in-line, plastic, 32-pin (DIL32SHR) (SOT232AG).

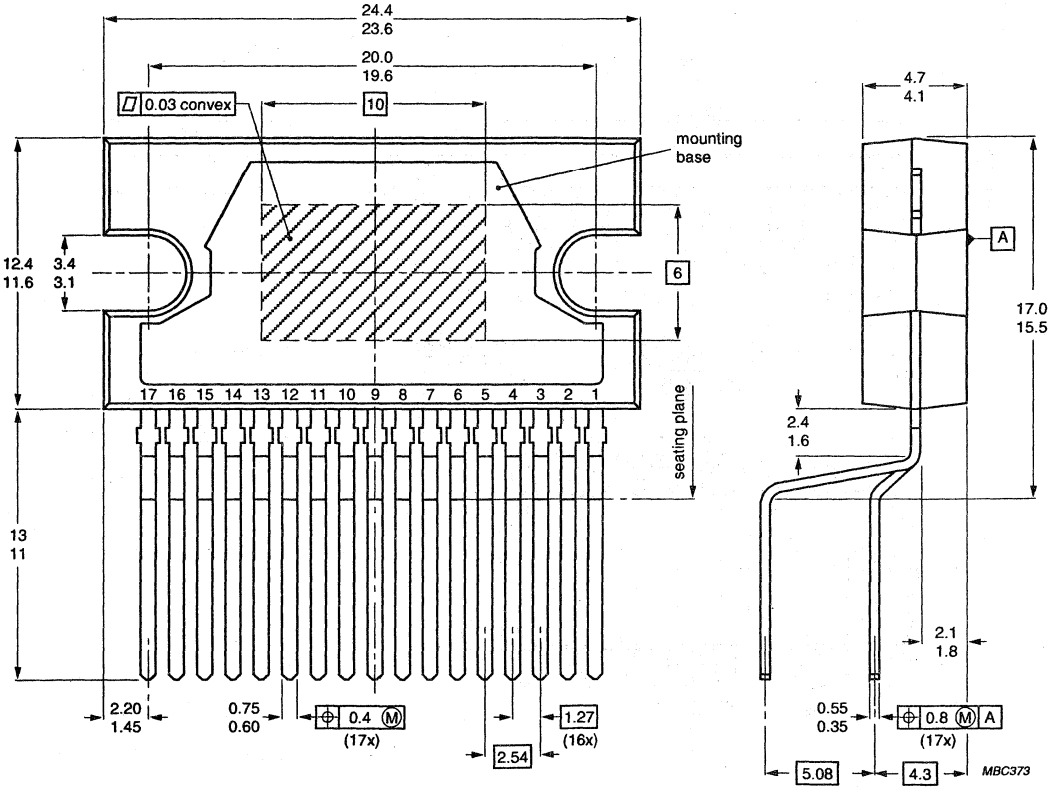
Package outlines



Dimensions in mm.

Fig.54 Shrink dual in-line, plastic, 24-pin (DIL24SHR) (SOT234AG).

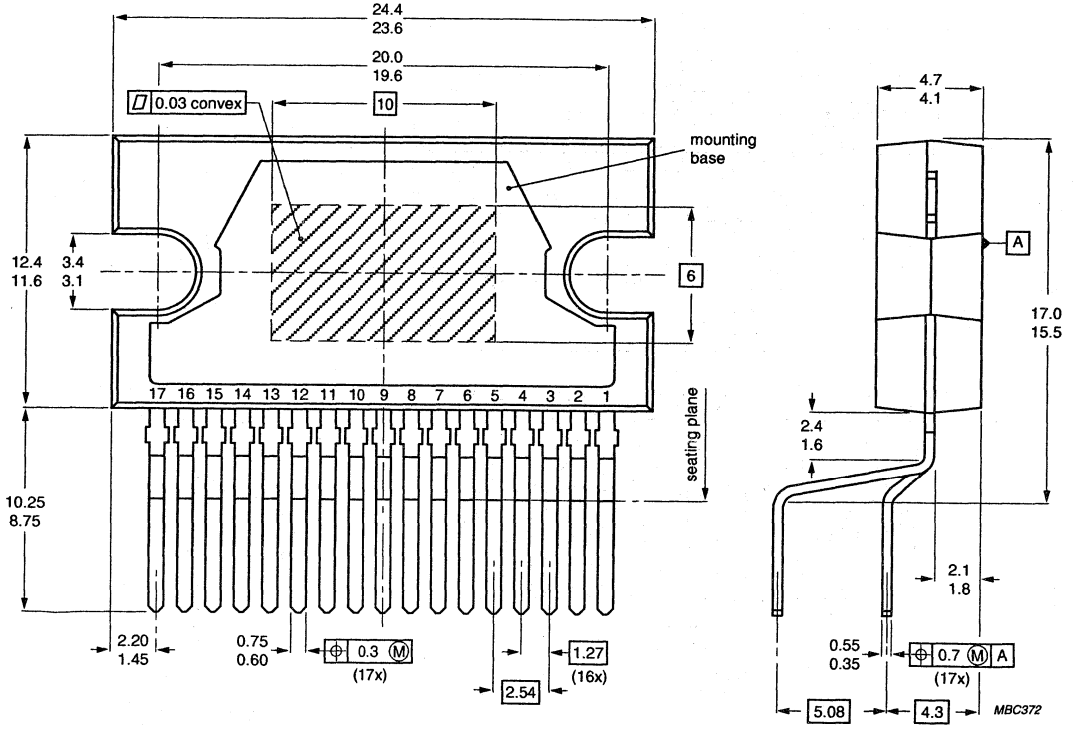
Package outlines



Dimensions in mm.

Fig.55 DIL-bent-SIL, plastic, power, 17-pin (DBS17P) (SOT243RAA, RGA).

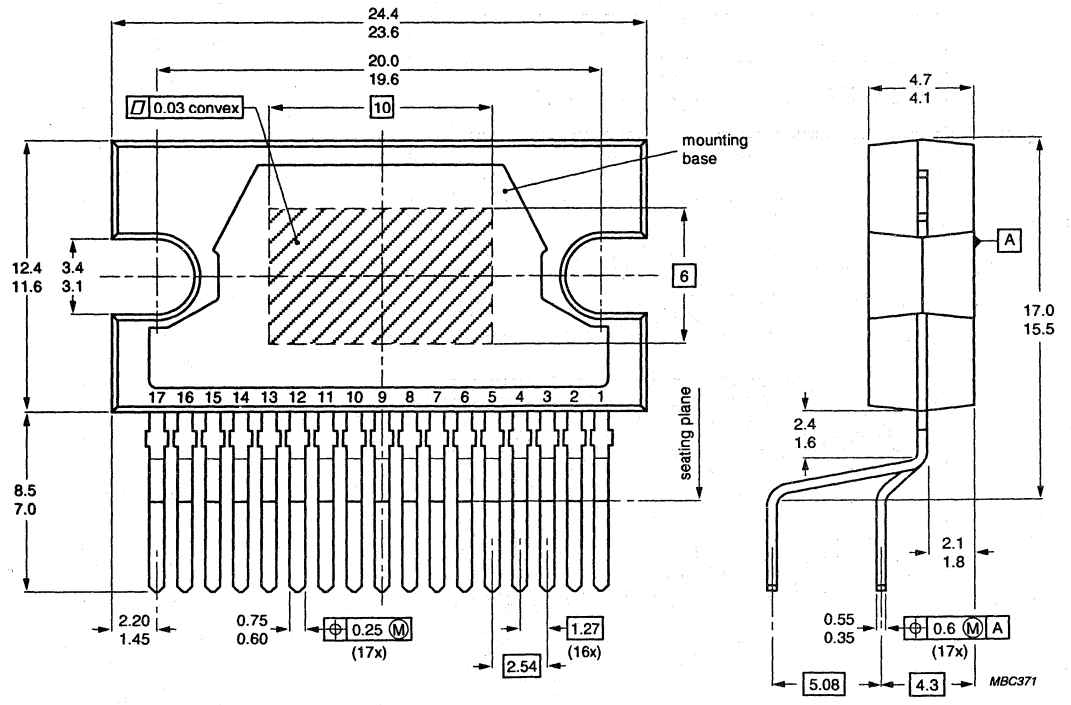
Package outlines



Dimensions in mm.

Fig.56 DIL-bent-SIL, plastic, power, 17-pin (DBS17P) (SOT243RAB, RGB).

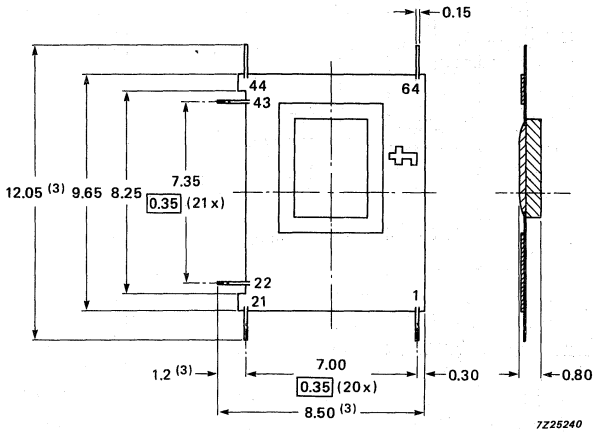
Package outlines



Dimensions in mm.

Fig.57 DIL-bent-SIL, plastic, power, 17-pin (DBS17P) (SOT243RGC).

Package outlines

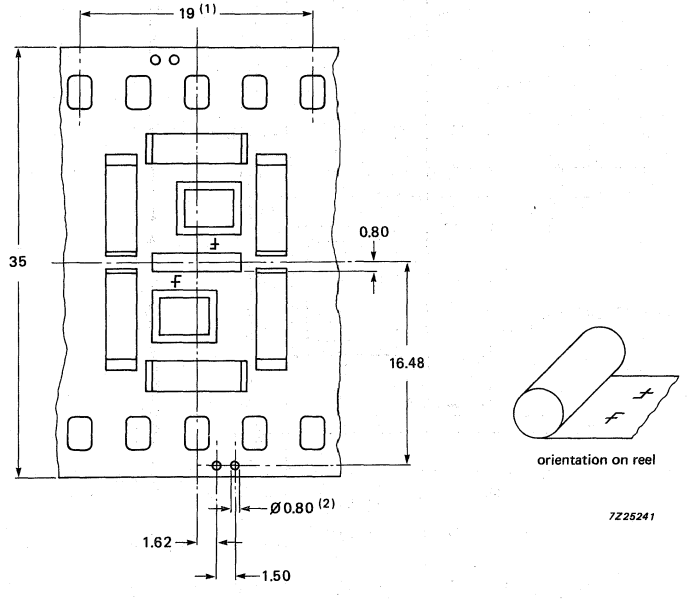


(3) Fixed by the user

Dimensions in mm.

Fig.58 Tape-automated-bonding, tab module, 64-lead (SOT267A, C, D).

Package outlines

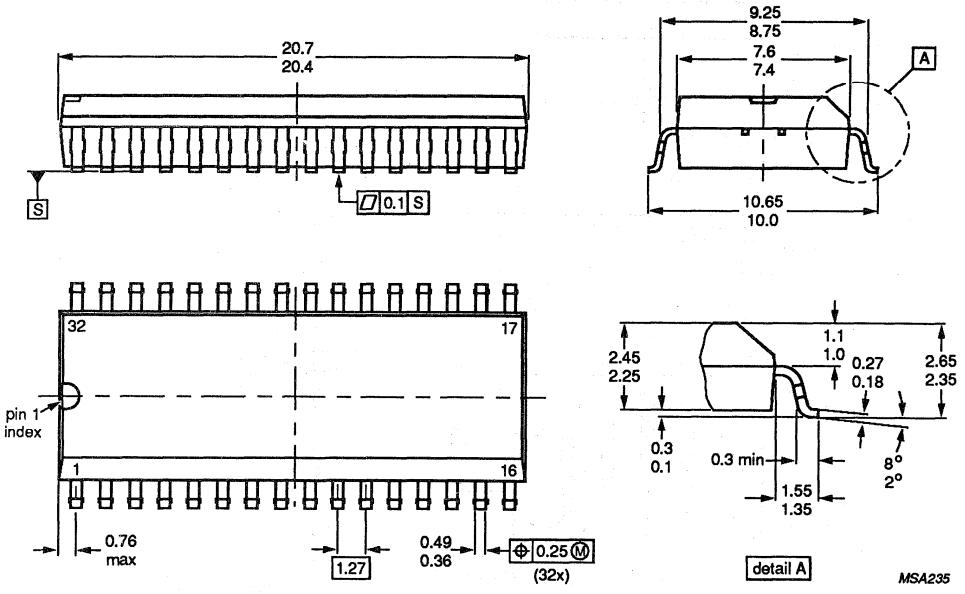


(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes

Dimensions in mm.

Fig.59 Tape-automated-bonding, tab module, 64-lead (SOT267A, C, D).

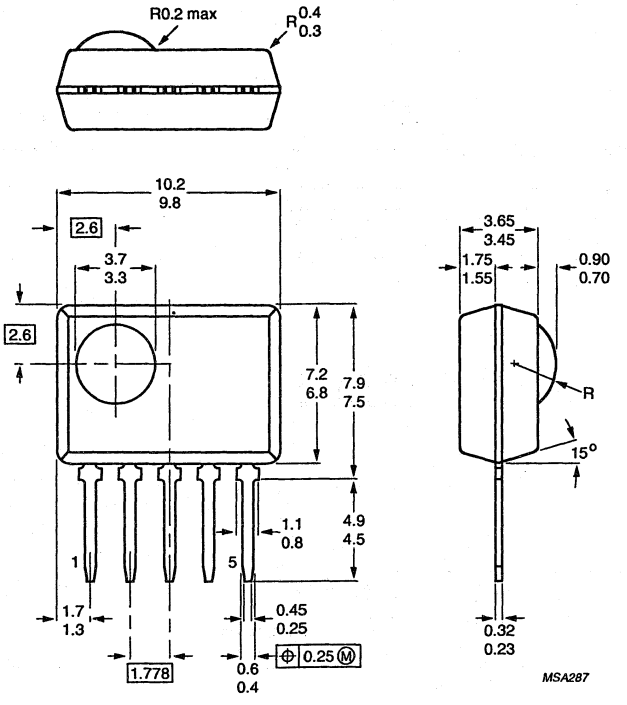
Package outlines



Dimensions in mm.

Fig.60 SOL, plastic, 32-pin (SO32L) (SOT287AH, AJ).

Package outlines



Dimensions in mm.

Fig.61 Single in-line, plastic, 5-pin (SIL5) (SOT294A).

Package outlines

SOLDERING

Plastic mini-packs, PLCC and QFP

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using a pulse-heated tool is usually suitable. Limit the soldering operation to 3 s at 250 °C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do **not** use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do **not** use solvents.

DATA HANDBOOK SYSTEM

Data handbook system

INTRODUCTION

Our data handbook system comprises more than 65 books with subjects including electronic components, subassemblies and magnetic products. The handbooks are classified into seven series:

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DISCRETE SEMICONDUCTORS;

DISPLAY COMPONENTS;

PASSIVE COMPONENTS;

PROFESSIONAL COMPONENTS;

MAGNETIC PRODUCTS;

LIQUID CRYSTAL DISPLAYS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

For more information about data handbooks, catalogues and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and enquiries are answered promptly.

INTEGRATED CIRCUITS

IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	ECL 100K ECL Logic Family
IC10	Memories
IC11	General Purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals

INTEGRATED CIRCUITS (continued)

IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-Car Electronics and General Industrial Applications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-Protocol Controllers and Fibre Optics
IC20	8051-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers
IC22	ICs for Multi-Media Systems
IC23	QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	PowerMOS Transistors
SC14	Wideband Transistors and Wideband Hybrid IC Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

DISPLAY COMPONENTS

DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Loudspeakers
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

PASSIVE COMPONENTS

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

PROFESSIONAL COMPONENTS

PC01	High-power Klystrons and Accessories
PC02	Cathode-ray Tubes
PC03	Geiger-Müller Tubes
PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC06	Circulators and Isolators
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC09	Dry-reed Switches
PC11	Solid-state Image Sensors and Peripheral Integrated Circuits
PC12	Electron Multipliers

MAGNETIC PRODUCTS

MA01	Soft Ferrites
MA02	Permanent Magnets
MA03	Piezoelectric Ceramics

LIQUID CRYSTAL DISPLAYS

LCD01	Liquid Crystal Displays and Driver ICs for LCDs

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